Synchronous Rectification Controller for Boosting Up the Efficiency of a Flyback Converter

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Abstract— In low output voltage power converters, the efficiency is mainly affected due to the voltage drop of a diode. One of the best solution is to replace this diode with a synchronous rectifier. Synchronous rectification (SR) is the technique for boosting up the efficiency of rectification by replacing the diode with actively controlled power MOSFET switch. In this paper, an effective approach for controlling the SR MOSFET of the flyback converter using SR controller is presented. The negative voltage across the output due to overlapping of the primary and secondary switches can be removed by using SR controller. Also SR controller assures reliable turn-on and turn-off of the SR MOSFET and reduces the cross conduction loss between the primary side MOSFET and secondary synchronous rectification MOSFET, thus higher efficiency can be achieved. The response of the SR controller is evaluated by simulating a 50-W flyback converter using MATLAB/ SIMULINK.

Key words: Flyback Converter, Synchronous Rectification

I. INTRODUCTION

Among all the various switched mode power supply converters, flyback converter is considered to be the most favorable one. This is mainly because of its simple topology and low cost. Flyback converter is the most significant converter for low power applications where the output voltage is completely isolated from the input main supply. It requires only one magnetic component and only one output rectifier. The secondary side rectification stage of a switched mode power supply is mostly realized with a diodes. In low power and high switching frequency applications, the conduction loss of this diode rectifier which mainly depends on forward voltage drop and forward current, greatly contributes to the overall power loss in the power supply. The forward voltage drop across a diode rectifier and the output voltage are in series, therefore losses in this rectifier greatly determines the efficiency. Replacing this diode with a more efficient MOSFET is considered as a clear means of drastically improving the efficiency to meet the voluntary energy standard, removing the need for bulky heat sinks and reducing the size and weight of power adapters.

Self-driven method is the most popularly used method to drive a synchronous rectifier. In this method, the voltage across the secondary side of the transformer is used to drive the SR, thereby the complexity in the circuit and cost can be reduced without affecting the efficiency.

Fig.1 shows a flyback converter having a synchronous rectifier MOSFET on the secondary side to reduce the rectification losses. As can be seen in Fig.1, the flyback converter consists of a transformer, a switching device M_1 which controls the conduction between the primary winding of the transformer N_P and an input voltage source V_{IN} and an output capacitor C_0 connected to the secondary winding of the transformer N_S.

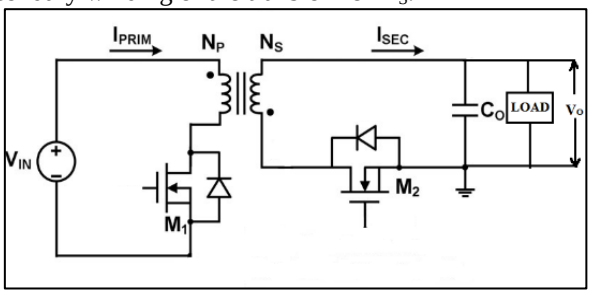


Fig. 1: A Flyback Converter with a Synchronous Rectifier

Basically a flyback converter has two operation states i.e., discontinuous operation state and continuous operation state. In the discontinuous operation state, all the energy stored in the transformer is completely delivered to the load before the next cycle starts. So, induced voltage will not be left in the transformer to resist the output capacitor discharging back to the transformer.

In the first operation mode, the switching device M_1 is switched ON to conduct the input voltage source V_{IN} to the primary winding N_P, and energy is stored to the transformer. In the second operation mode, the connection between the primary winding of the transformer N_P and the input voltage source V_{IN} is no more present and the energy stored in the transformer will be freewheeled to the output capacitor.

As a difference, in the continuous operation state, some amount of energy remains in the transformer i.e., before the current released from the secondary winding N_S falls to zero, the next switching cycle starts. When the synchronous rectifier MOSFET M_2 is switched OFF after the start of the next switching cycle, a reverse charging operation of the output capacitor may takes place.

For proper and effective operation of the converter, the conduction periods of primary switch M_1 and secondary switch M_2 should not overlap which means, primary side and secondary side switching operation must be in synchronization. For that purpose, the on-time duration of the primary side switch must be sensed to produce the synchronized control signal to the secondary side MOSFET.

In this paper, the operation of a low cost SR controller is explained. The way in which the controller prevents the overlapping of the primary and secondary switches is described, finally the response of the controller is analyzed.

II. SYNCHONOUS RECTIFICATION CONTROLLER

Flyback converter with SR controller is shown in Fig. 2. In Fig. 2, the flyback converter consists of a transformer having a primary winding N_P coupled to a primary circuit and a secondary winding N_S which is coupled to a secondary

circuit. In the primary circuit, the primary winding N_P is connected between an input voltage source V_{IN} and a switching device M_1. The secondary circuit has a MOSFET M_2, an output capacitor C_0, and the SR controller. A drain of the MOSFET M_2 is connected to V_{SEN} of the secondary winding N_S. The output capacitor is connected between a terminal of the secondary winding and an output terminal of the secondary circuit. The SR controller is coupled to the MOSFET M_2. The control signal Φ_{SEC} is generated based on the secondary signal voltage V_{SEN} to drive a gate of the MOSFET M_2. In a continuous operation mode, a signal Φ_{PRIM} turns on and off the switching device M_1 in the primary circuit to generate a primary current I_P flowing through the primary winding N_P. Energy will be stored in the transformer. The primary current is in phase with the switching signal Φ_{PRIM}. When the switching device M_1 disconnects the conduction between the input voltage source V_{IN} and the primary winding N_P, the primary current I_P will be ended and the secondary current I_S will flow through the secondary winding N_S to the secondary circuit. As a result, energy stored in the transformer is delivered to the output terminal of the flyback converter and the output capacitor to be the output voltage V_0.

The SR controller is illustrated in Fig. 3. Here, if the primary switch turns OFF, then the voltage level of SR_{SEN} decreases and if the voltage level is smaller than -60mV then the clock signal Φ_{CLK} goes LOW. The falling edge of Φ_{CLK} generates a pulse in Φ_{ON}, which turns ON the secondary switch M_2. A SR latch is used to generate Φ_{CLK},. Similarly, if the primary switch turns ON, the voltage level of SR_{SEN} increases and if the voltage level is is larger than 4.0 V, the clock signal Φ_{CLK} goes HIGH.

A. Secondary Switch off Controller (SSOC):

The secondary switch off controller is employed to turn OFF the secondary switch right before the primary switch turns ON, i.e., right before the Φ_{CLK} goes to high to prevent the cross conduction between the primary and the secondary switches, to prevent a reverse discharge current from the output capacitor and to remove the negative voltage between the synchronous rectifier's gate and source.

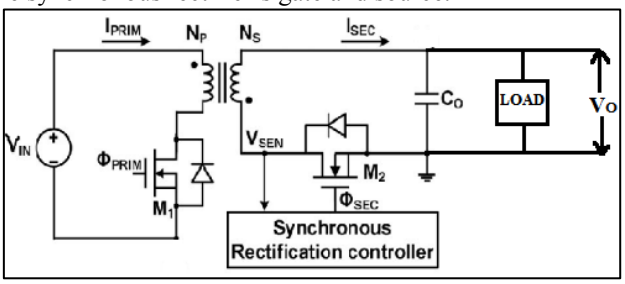


Fig. 2: Flyback Converter with SR Controller

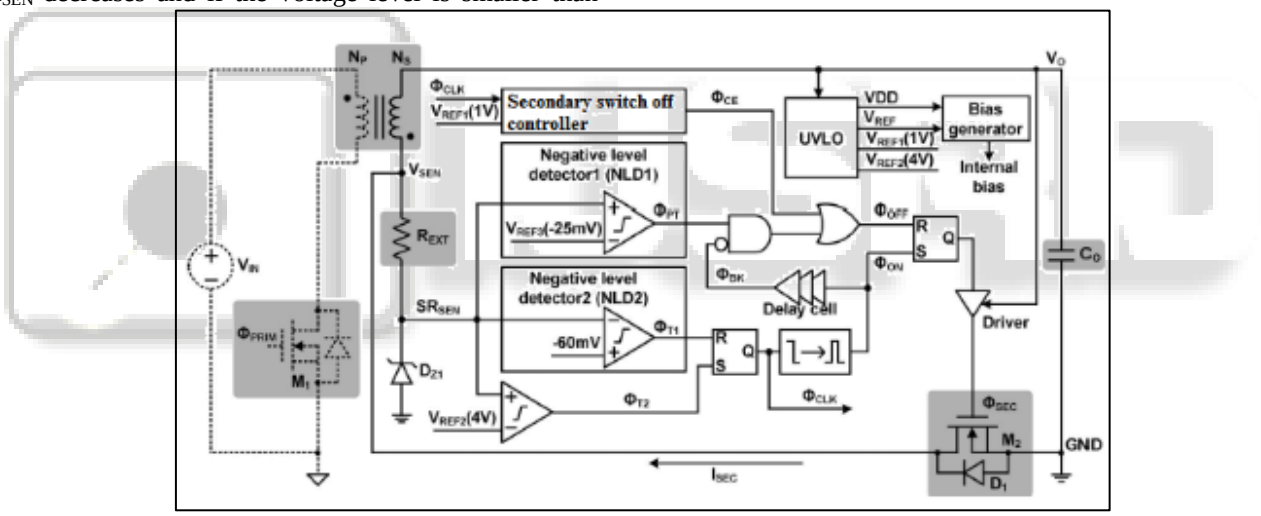


Fig. 3: SR Controller

The SSOC detects the period of the clock pulse Φ_{CLK} to generate a pulse in Φ_{CE} right before clock pulse Φ_{CLK} becomes high, due to which Φ_{OFF} becomes HIGH. The period of Φ_{CLK} varies from cycle to cycle, if the operation mode changes between the CCM and the DCM or if the load current changes. Since the SSOC generates Φ_{CE} depending on the period of Φ_{CLK} which is detected one cycle earlier, Φ_{CE} cannot be adjusted properly to high if the period of Φ_{CLK} changes. This may lead to overlapped conduction of the primary and secondary switches, which greatly affects the converter efficiency. To overcome this, the control signal Φ_{PT} is set to HIGH by detecting the voltage level across the secondary switch M_2.

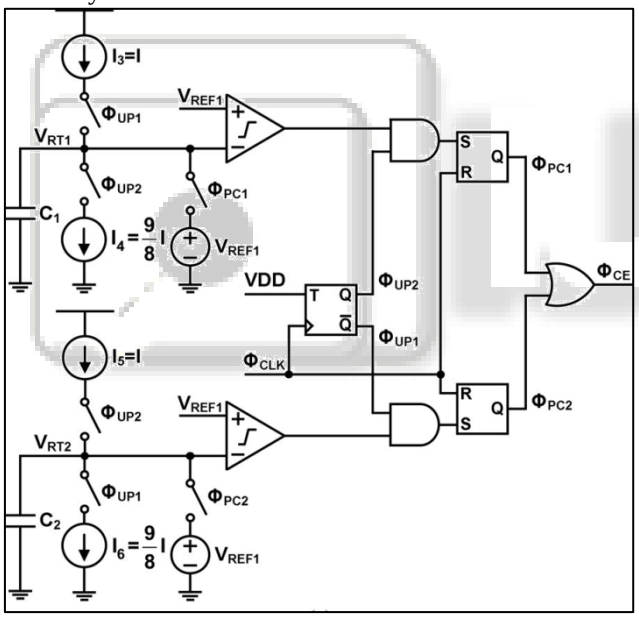
As shown in fig. 4(a), the SSOC includes four current sources, two comparators, a T-type flip-flop, two SR flip-flops, AND gates and a OR gate. The upper comparator has a positive input supplied with a reference voltage V_{REF1}, a negative input supplied with V_{RT1}, and an output connected to the AND gate. The lower comparator has a positive input supplied with a reference voltage V_{REF1}, a negative input supplied with V_{RT2}, and an output connected to the AND gate. The clock input Φ_{CLK} is divided by a toggle flip-flop to generate Φ_{UP1} and Φ_{UP2}. When Φ_{UP1} is HIGH, the capacitor C_1 gets charged by the current source I_3 and V_{RT1} increases linearly. If V_{REF1} is higher than V_{RT1}, the output of the comparator is HIGH and thereby Φ_{PC1} and thus Φ_{CE} becomes HIGH. During the next cycle of Φ_{CLK}, the lower half circuit of the SSOC performs the same operation as explained above. Fig. 4(b) shows the timing diagram of the SSOC.

When the operating mode changes from the CCM to the DCM, the period of clock pulse becomes shorter temporarily, Then, there is no enough time for V_{RT2} to be discharged to reach V_{REF1} and Φ_{CE} cannot be set to HIGH. Then the DMOC cannot produce the turn-off signal Φ_{OFF} of the secondary side switch at a proper time. This may lead to cross conduction of the switches, thereby decreasing the power efficiency. To avoid this problem, Φ_{PT} sets Φ_{OFF} to

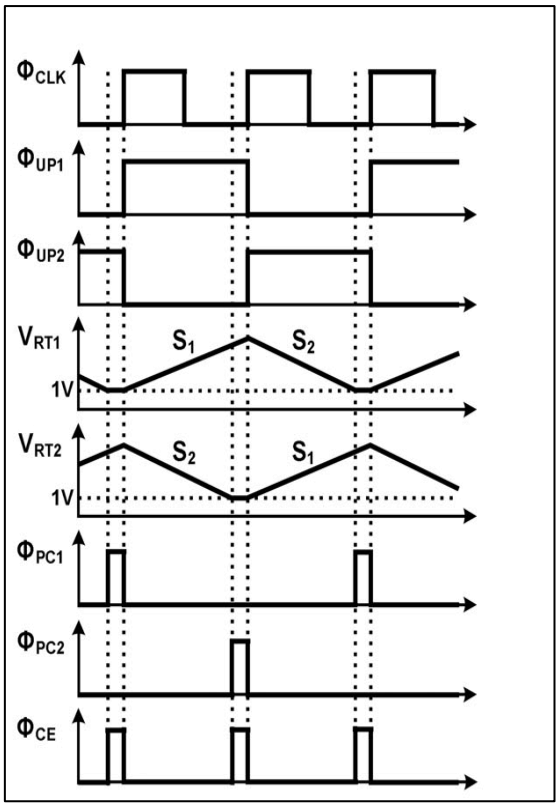
HIGH by detecting the voltage level across the swiching MOSFET. As illustrated in fig. 3, the NLD1 sets Φ_{PT} to HIGH when the voltage level of SR_{SEN} is larger than V_{REF3} (-25mV)

When the operating mode changes from the DCM to the CCM, the period of clock pulse becomes longer temporarily, V_{RT1} cannot be discharged to reach V_{REF1} and Φ_{CE} cannot be set to HIGH. Then, the SSOC cannot produce the turn OFF signal Φ_{OFF} of the secondary side switch at a proper time. This may lead to cross conduction of the switches, thereby decreasing the power efficiency. To prevent this problem, Φ_{PT} sets Φ_{OFF} to HIGH by detecting the voltage level across the switching MOSFET. To prevent this, the NLD1 sets Φ_{PT} to HIGH when the voltage level of SR_{SEN} is larger than V_{REF3} (-25mV) to generate the turn-off signal Φ_{OFF}.

When the transformer operates in the continuous operation mode, the delay time ensures that the MOSFET M_2 is turned off before the next switching cycle starts. This prevents a backward charging to the output capacitor and thus, protects the MOSFET from over-stress switching. Therefore, a proper value of the delay time is very important for the synchronous rectifying. A wider delay is needed for the switching; however, a shorter delay can achieve higher efficiency.



(a)



(b)

Fig. 4: (a) SSOC and (b) Its Timing Diagram

III. SIMULATION RESULTS

The SR controller is applied to a 50-W flyback converter with a switching frequency of 65-kHz, which is supplied by a 220-V input voltage and 13.5-V output voltage. Fig. 5 and Fig. 6 shows the simulation model and timing diagram of SSOC respectively. The response of the flyback converter with the SR controller is shown in Fig. 7.

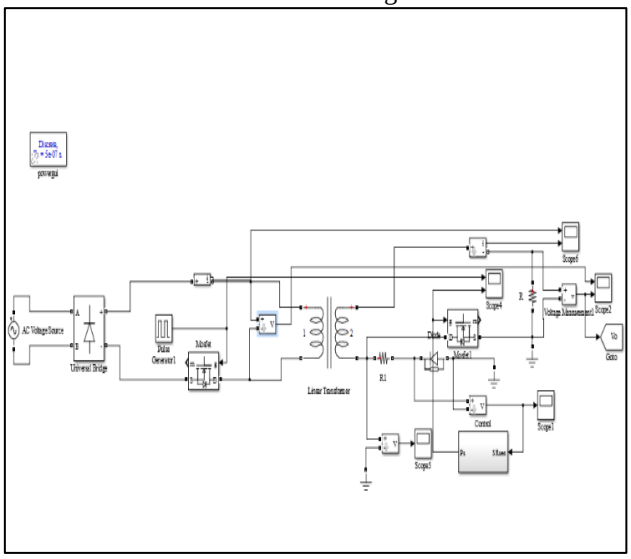


Fig. 5: Simulation Model of A Flyback Converter With SR Controller

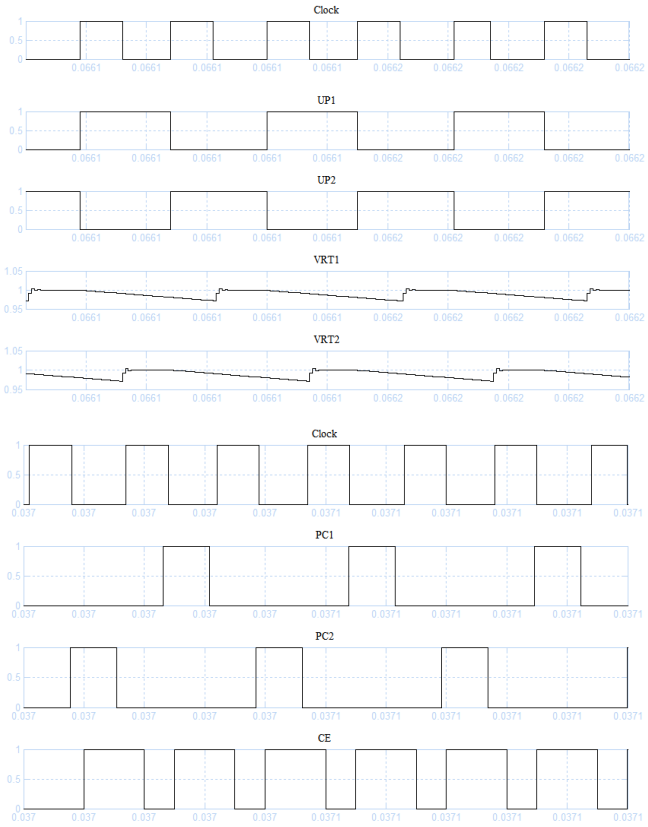
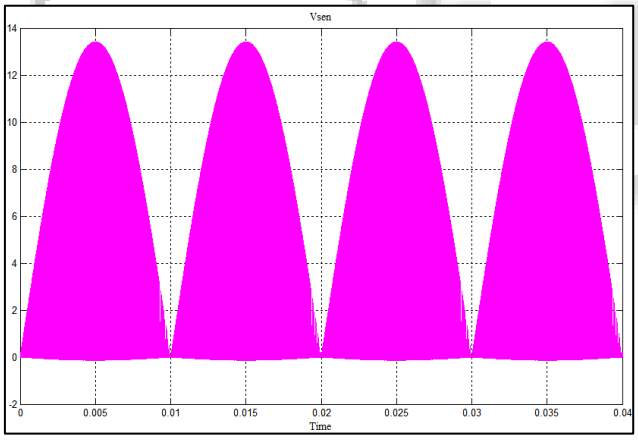
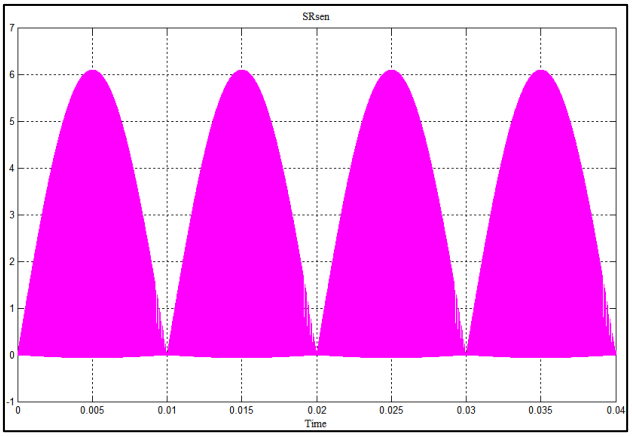


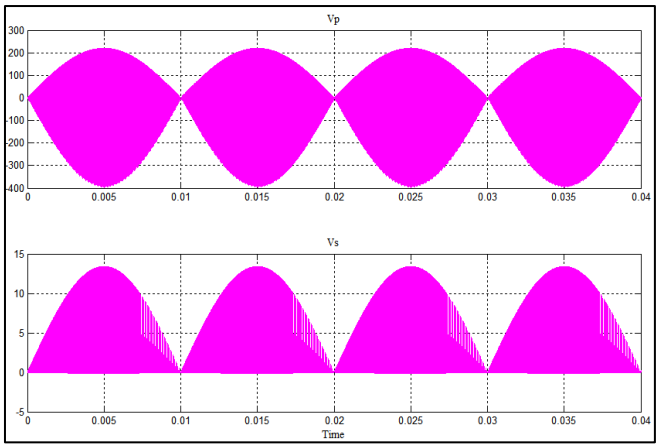
Fig. 6: Timing Diagram of SSOC



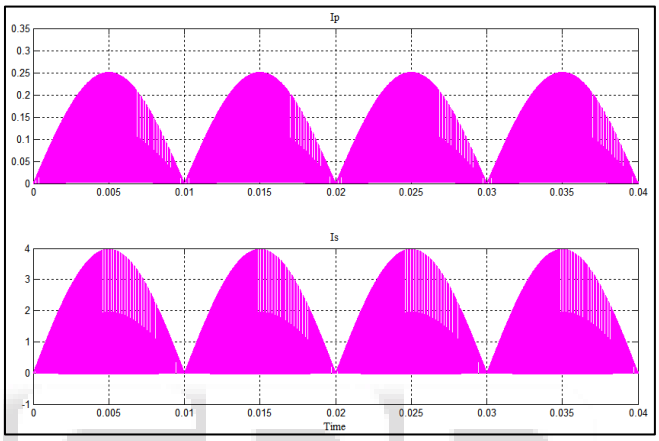
(a) V_{sen}



(b) SR_{sen}



(c) V_p, V_s



(d) I_p, I_s

Fig. 7: Simulation Results

IV. CONCLUSION

The SR approach is a preferred choice in applications where it is required to meet high-power densities, for example, in ac/dc adapters, for portable equipment, In this paper, a synchronous rectification controller applicable to flyback converter is explained and its operation is analyzed and discussed. The control method explained herein has an advantages of reduced conduction losses, removal of negative voltage across the output, prevention of overlapped conduction of primary and secondary side switches. The control scheme is applied to a 50-W flyback converter and the obtained efficiency is 97.45%.

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