Design of Phase Locked Loop as a Frequency Synthesizer

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Abstract— In this paper a PLL is designed and implemented. A PLL is a closed loop frequency system that locks the phase of an output signal to an input reference signal. The term ―lock refers to a constant or zero phase difference between two signals. The signal from the feedback path is compared to the input reference signal, until the two signals are locked. If the phase is unmatched, this is called the unlocked state, and the signal is sent to each component in the loop to correct the phase difference. These components consist of the PFD, CP, LPF, VCO and divide by counter. The application I chose in designing the PLL was a frequency synthesizer. A frequency synthesizer generates a frequency that can have a different frequency from the original reference signal.

Key words: Phase Locked Loop, Phase Frequency Detector, Charge Pump, Low Pass Filter, Voltage Controlled Oscillator

I. INTRODUCTION

PLL is essentially a feedback loop that locks the on-chip clock phase to that of an input clock or signal. High-performance PLLs and clock buffers are widely used within a digital system for two purposes: clock generation, and timing recovery. For clock generation, since off- chip reference frequencies are limited by the maximum frequency of a crystal frequency reference, (Typically in the range of 10 MHz) a PLL receives the reference clock and multiplies the frequency to the multi-gigahertz operating frequency. The high-frequency clock is then driven to all parts of the chip. Timing recovery pertains to the data communication between chips. As data rates increase to satisfy the increase in on-chip processing rate, the phase relationship between the input data and the on-chip clock is not fixed. To reliably receive the high-speed data, a PLL locks the clock phase that samples the data to the phase of the input data. Phase locked loop is closed loop control system that compares the output phase with the input phase.

High-performance digital systems use clocks to sequence operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. Within the digital systems, well-timed clocks are generated with phase-locked loops (PLLs). The rapid increase of the system‘s clock frequency possesses challenges in generating and distributing the clock with low uncertainty

II. PLL BUILDING BLOCKS

Phase-locked loops (PLLs) generate well-timed on-chip clocks for various applications such as clock-and-data recovery, microprocessor clock generation and frequency synthesizer. The basic concept of phase locking has remained the same since its invention in the 1930s. However, design and implementation of PLLs continue to be challenging as design requirements of a PLL such as clock timing uncertainty, power consumption and area become more stringent.

This section briefly discusses the basic concept of phase locking. A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL.

A PLL also multiplies a low-frequency reference clock CK REF clock CK OUT, to produce a high-frequency

A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals. The overall goal of the PLL is to match the reference and feedback signals in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

A basic form of a PLL consists of five main blocks:

1) Phase Frequency Detector (PFD)
2) Charge Pump (CP)
3) Low Pass Filter (LPF)
4) Voltage Controlled Oscillator (VCO)
5) Divide by N Counter

The phase frequency detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error. If there is a phase difference between the two signals, it generates up or down synchronized signals to the charge pump/ low pass filter. If the error signal from the PFD is an up signal, then the charge pump pumps charge onto. the LPF capacitor which increases the control voltage $V_{control}$ On the contrary, if the error signal from the PFD is a down signal, the charge pump removes charge from the LPF capacitor, which decreases $V_{control}$. $V_{control}$ is the input to the VCO. Thus, the LPF is necessary to only allow DC signals into the VCO and is also necessary to store the charge from the CP. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. If the PFD generates an up signal, the VCO speeds up. On the contrary, if a down signal is generated, the VCO slows down. The frequency of oscillation is divided down to the feedback clock by a frequency divider. The phase is locked when the feedback clock has a constant phase error and the same frequency as the reference clock. Because the feedback clock is a divided version of the oscillator‘s clock frequency, the frequency of oscillation is N times the

reference clock.

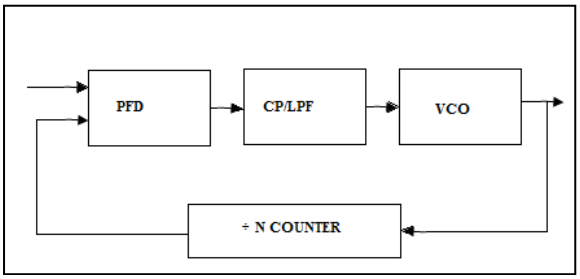

Fig. 1: Block diagram of the proposed PLL.

A. Phase Frequency Detector (PFD):

The PFD, measures the difference between the reference and feedback signals. If there is a phase difference it generates synchronized up or down signal to the LPF or charge pump. If he PFD is an up error signal, then the charge pump pumps charge on to the LPF capacitor this rises the control voltage *V*control. and if the PFD error signal is a down signal, charge pump reduses charge from the LPF capacitor, this reduses *V*control.

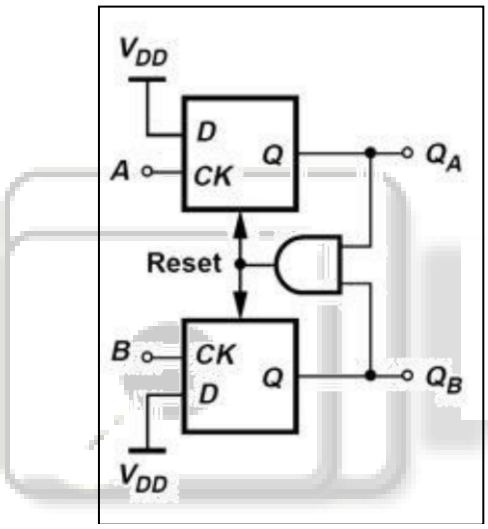

Fig. 2: PFD Schematic Circuit

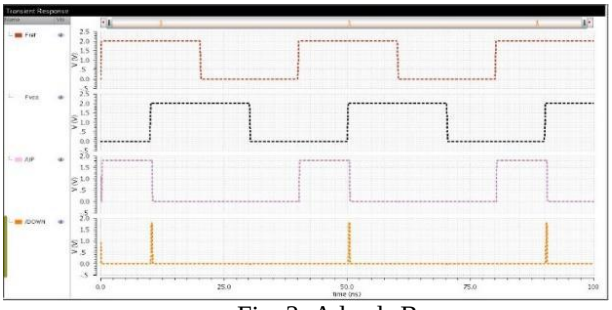

Fig. 3: A leads B

The above shown PFD circuit can be analyzed in two different ways. One way where A is greater than B and the other where B greater than A.

Fig. 4: B leads A

The two clock signals phase difference signal is QA pulse. This QA pulse indicates to the remaining whole circuit that the feedback signal requires to catch up or speed up with the reference signal. In the second case B is greater than A. In this case the phase of two clock signals is QB pulse. Figure 4 represents B is greater than A simulation results

B. Charge Pump (CP)

The action of pumping charge into or out of the loop filter which depended by two logical input signalsis completed by the two switched current sources. The circuit is consist of three states. If QA=0, QB=0, then output voltage remains constant because both switches are off. If QA=1, QB=0, then capacitor charged through the current of PMOS branch. Like that if QA=0, QB=1, then the capacitor discharged by current in the PMOS branch. If for example, QA continues to produce pulses and output rises steadily only when A is greater than B, then. Like that B is greater than A, then QB continues to produce pulses and output falls steadily. The currents through the both PMOS and NMOS branches are nominally equal.

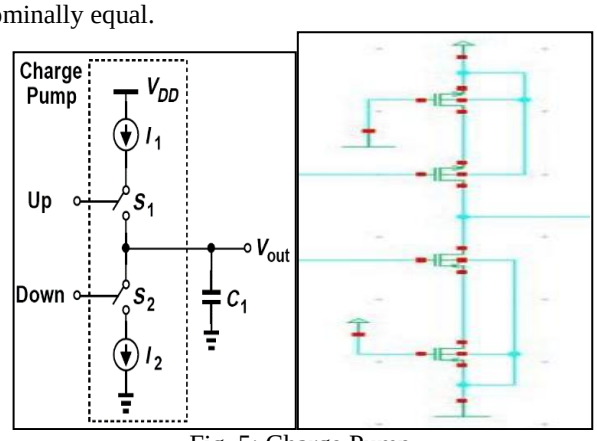

Fig. 5: Charge Pump

C. Loop Filter

The loop filter is the main circuit of PLL. If the loop filter values are not selected correctly, it may take the loop too long to lock, or once locked small variations in the input data may cause the loop to unlock. The PFD/CP/LP combination contains a pole at the origin and VCO also contains a pole at the origin. So the instability arises because the loop gain has two poles at the origin. In order to stabilize the system, we must modify the phase characteristics by adding a resistor in series with the loop filter capacitor. The

compensated PLL also suffers from a critical drawback. Since the charge pump drives the series combination of R1 and C1, each time a current is injected into the loop filter, the control voltage experiences a large jump. To relax this issue, a second capacitor is usually added in parallel with R1 and C1.

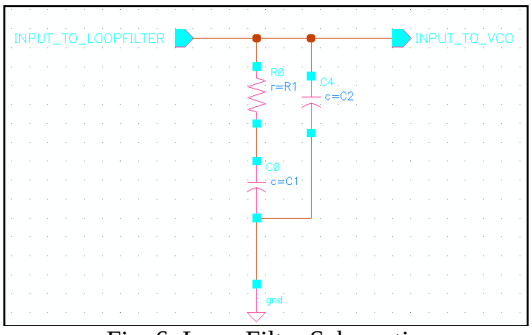

Fig. 6: Loop Filter Schematic

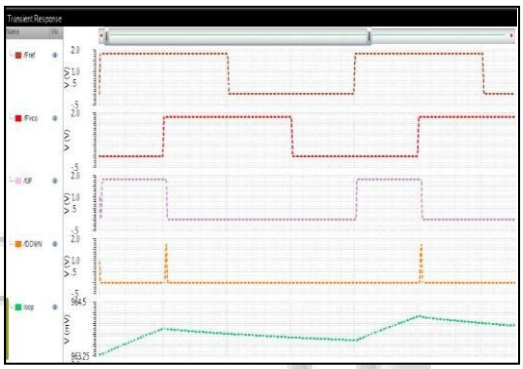

Fig. 7: When PMOS On

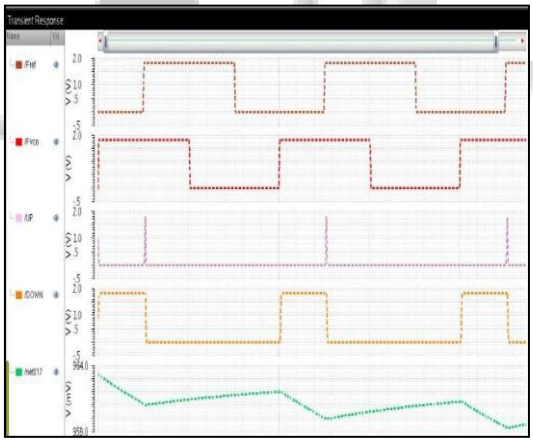

Fig. 8: When NMOS ON

D. Voltage Controlled Oscillator (VCO):

An oscillator is an autonomous system that generates a periodic output without any input. Most applications require that oscillators be ―tunable. i.e., their output frequency be a function of a control input, usually a voltage. An ideal voltage-controlled oscillator is a circuit whose output frequency is a linear function of its control voltage. There are different types of voltage controlled oscillators used in PLL. Here I am discussing about 2 types of VCOs. Source coupled VCO and Current starved VCO. The source coupled VCO can be designed to dissipate less power than the current starved VCO. The major disadvantage of this configuration is the need of a capacitor. However this configuration is useful when the VCO center frequency is set by an external capacitor. The operation of current starved VCO is similar to the ring oscillator. Middle PMOS and NMOS operate as inverter, while upper PMOS and lower NMOS operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter/current source stage. Since the propagation delay of the inverters is proportional to the current each inverter supplies to the output, we can effectively control the frequency.

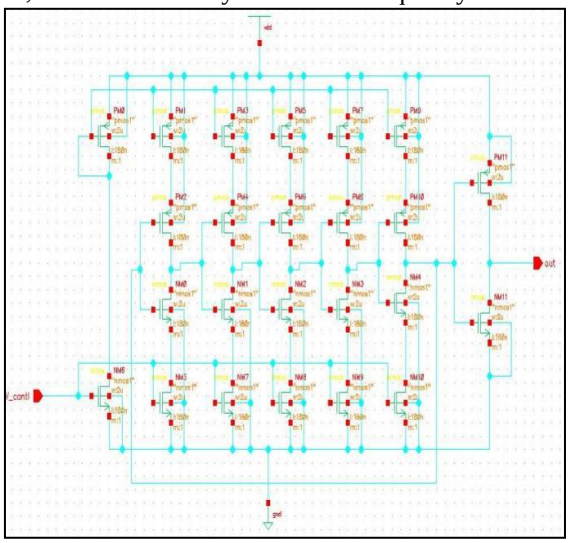

Fig. 9: Current Starved VCO

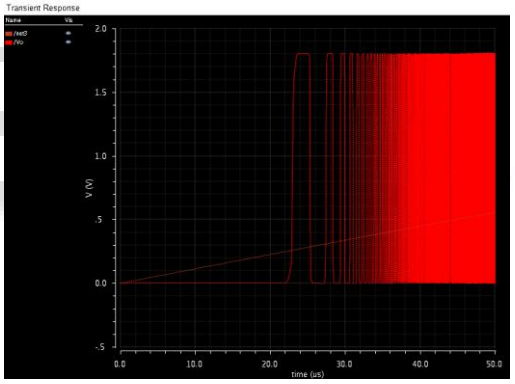

Fig.10: VCO Output

Two different VCO outputs, the above output shows the frequency starts at a particular point. The below output shows the change of frequency depending upon high and low voltage.

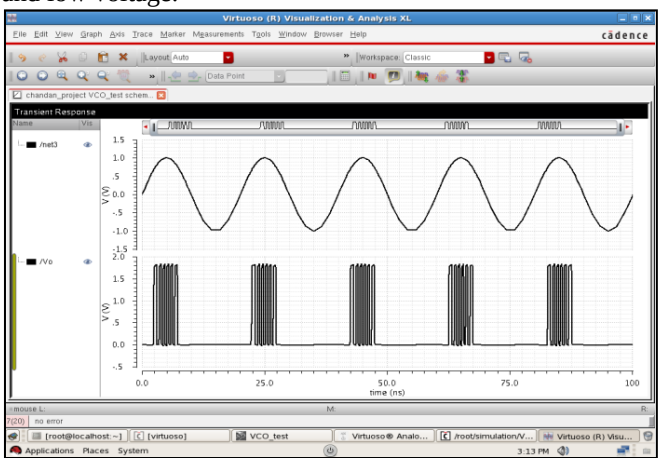

Fig. 11: VCO output

E. Divide By Counter

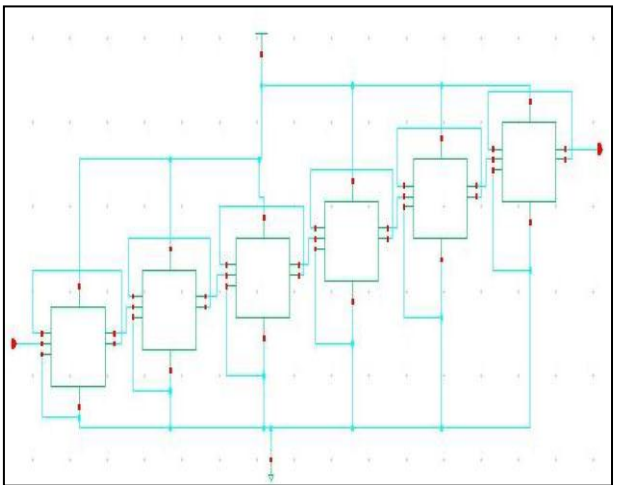

Fig.12: Divide by 64 Counter

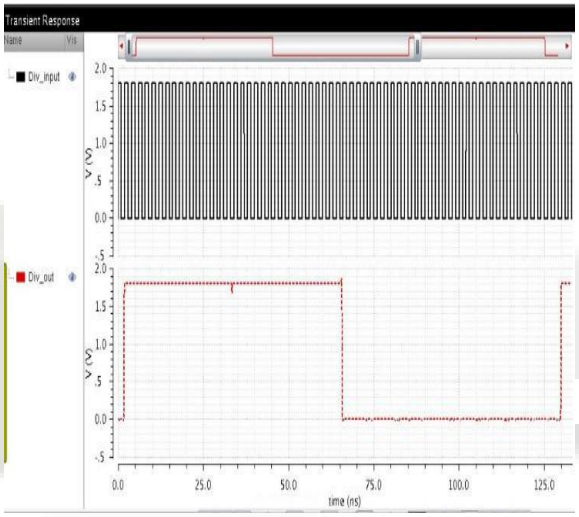

Fig. 13: Output of Divide by 64 Counters

III. PHASE LOCKED LOOP

The frequency of oscillation is divided down to the feedback clock by a frequency divider. The Phase is locked when the feedback clock has a constant phase error and the same frequency as the reference clock, because the feedback clock is a divided version of the oscillator's clock frequency, the frequency of oscillation is N times the reference clock.

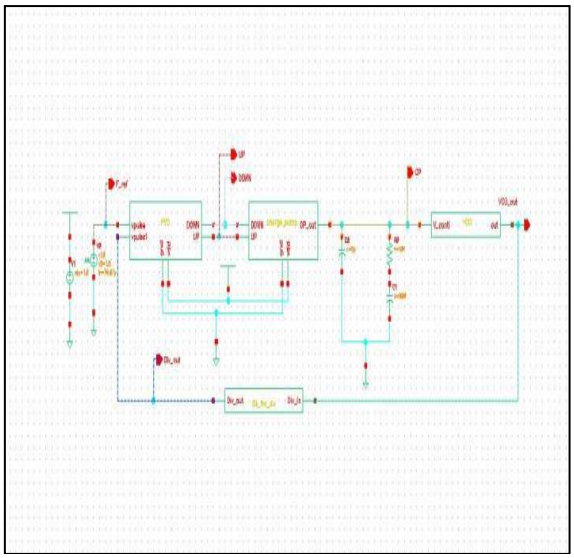

Fig. 14: Complete PLL circuit

The below output is the complete output of PLL, you can clearly see the output of VCO varying depending on the charge pump output.

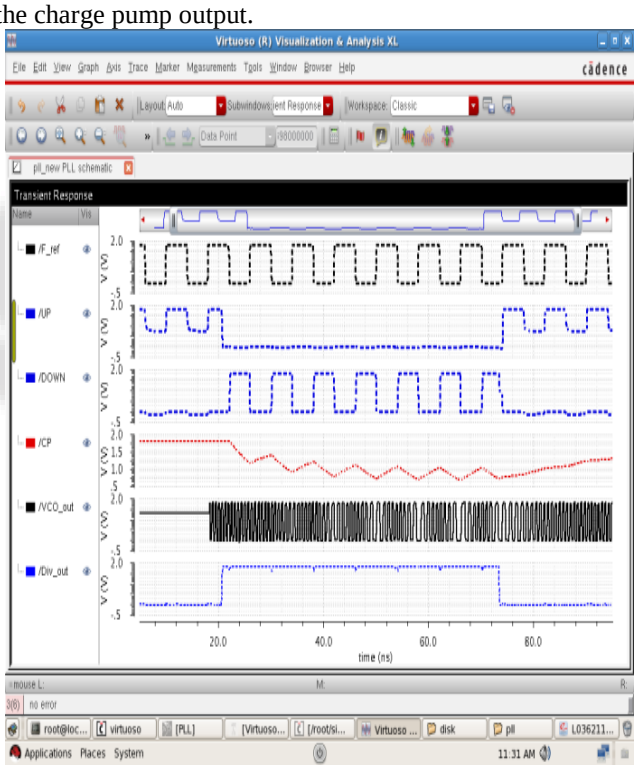

Fig. 15: PLL Output

IV. PLL SPECIFICATION

$F_{ref} = 10M$

$F_{out} = 640M$

Take Lock range as 1MHz. That is

$2\xi\omega_n = 1M$

Take $\xi = 0.7$

$\omega_n = 714.285K$

Lock Time = $T_L = \frac{2\Pi}{\omega_n}$

$\omega_n = \sqrt{\frac{K_{PDI}K_{VCO}}{NC_1}}$

$K_{PDI} = \frac{100}{2\Pi}\mu A/rad$

$K_{VCO} = 2\Pi\frac{f_{max} - f_{min}}{V_{max} - V_{min}}$

$= 2\Pi * 4179.3MHz$

$C_1 = 12.79nf$

[N=64]

$\xi = \frac{\omega_n}{2}RC_1$

R=153.2 Ω

Loop Bandwidth = 2.06 ω_n

=.359Mrad/s

Charge Pump Current = 100μA

Fig. 16

V. APPLICATIONS OF PLL & CONCLUNSIOS

Phase-locked loops are widely used for synchronization purposes; in space communications for coherent carrier tracking and threshold extension, bi synchronization, and symbol synchronization. Phase-locked loops can also be used to demodulate frequency-modulated signals. In radio transmitters, a PLL is used to synthesize new frequencies which are a multiple of a reference frequency, with the same stability as the reference frequency.

A. Clock Recovery:

Some data streams, especially high-speed serial data streams (such as the raw stream of data from the magnetic head of a disk drive), are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery. In order for this scheme to work, the data stream must have a transition frequently enough to correct any drift in the PLL's oscillator.

B. Clock Generation:

Many electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertz and the reference crystal is just tens or hundreds of megahertz.

C. Frequency Synthesis

A frequency synthesizer is an electronic system for generating a range of frequencies from a single fixed time base or oscillator. Frequency Synthesizer manufacturers include Analog Devices, National Semiconductor and Texas Instruments. VCO manufacturers include Sirenza, Z-Communications.

VI. CONCLUSIONS

1) Phase Locked Loop is designed for a frequency multiplying factor of 64 and verified.
2) A new high speed low glitch CMOS PFD is proposed. In the charge pump configuration, a new current source is replaced.
3) In order to achieve the stability in the loop filter, a resister is added in series with the loop filter capacitor. Since the charge pump drives the series combination of R1 and C1, each time a current is injected into the loop filter, the control voltage experience a large jump. To relax this issue, a second capacitor is added in parallel with R1 and C1.
4) Current starved VCO is selected as the voltage controlled oscillator in the design of PLL.
5) A divide by 64 counters is used for the synchronization with the input frequency.
6) 640 MHz is used in CMOS continuous-time sigma delta ADC, which can be achieved with this PLL design.

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