Study on various GDI Techniques for Low Power, High Speed Full Adder Design

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Abstract— This paper is an outcome of a survey on different full adders design methodologies using gate diffusion input technique. Gate diffusion input is a technique of low power digital combination design. This technique as compared to other currently used logic design styles, allows less power consumption and reduced propagation delay for low power design of combinational digital circuits with minimum number of transistor. A comparison is also made on the basis of power, delay and area to find out the best possible design technique. This paper presents a detail performance of GDI Based 1-bit Full Adder Circuit for Low Power Applications. Different techniques like GDI, PTL-GDI and GDI-MUX for the designing of full adder is reviewed.

Key words: Full Adder, GDI, MGDI

I. INTRODUCTION

Full adder is the most common and highly used element in the designing of every basic arithmetic circuit like Subtractor, Multipliers, and Dividers etc. It is the heart of Arithmetic Logic Unit. Even the minute change in the designing of adder cell will degrade the overall performance of the designed circuit. So care must be taken while designing these adder cells. One of the basic operations in most arithmetic components is the binary addition due to which adder is also known as fundamental arithmetic component of the processor. The design criterion of a full adder cell is usually multi fold.

The main concern while designing is the number of transistor count as it will largely affects the design complexity of many other functional unit such as multipliers and ALU. As the capability of power supply is limited, present battery technology has made power consumption an important figure in portable devices. Speed, power dissipation and wiring complexity of the circuit are highly influenced by the logic style used in logic gates. The propagation delay of circuit is determined by the number of transistors in series, the number of inversion levels, size of the transistor and the intra cell wiring capacitances.

The complementary CMOS full adder [1,2,3] is robust structure against voltage scaling and transistor sizing. As this circuit provides full swing which is extremely important when utilized in a more complex structure. The use of substantial number of transistors results in high input load, more power consumption and large silicon area.

A complementary Pass Transistor Logic (CPL) is one of the important conventional adder [1,2,3] which provides high speed, full-swing operation, as well as good driving capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors. The main issue with CPL is large power dissipation due to the presence of lot of internal nodes in whole circuit.

TFA [3,4,5] uses both NMOS and PMOS transistors. As there is no voltage drop problem in TFA but it requires double the number of transistors to design the function. The power consumption of TFA is very low due to which they are consider good for designing XOR and XNOR gates. Lack driving capability is the main disadvantage in this logic style as well as more number of transistors will be needed.

Transmission gate [5] one of the most commonly used and important CMOS which is highly used for the designing of full adder. As there is no voltage drop in transmission gate but it requires double the number of transistors to design a similar function. The main disadvantage of these logic styles is that there lack driving capability. When TGA are cascaded, their performance degrades significantly. To overcome its weak driving capability additional buffers are needed. By adding these buffers, area of the chip increases and power consumption will also increases simultaneously [3].

II. FULL ADDER CIRCUIT DESIGN TECHNIQUES

A. GDI Full Adder

GDI [9,10,11] is a technique of designing low power digital circuit which allows minimum power consumption, delay, and area of the whole chip. GDI method is based on the use of a simple cell as shown in Figure 1. The Truth Table is shown in Table 1. GDI approach allows implementation of complex logic functions using only two transistors over a wide range. The basic cell is similar to the standard CMOS inverter is connected to the terminal N or P, so it can be randomly biased at contrast with CMOS inverter. The major difference between GDI and CMOS is the designing of circuit as in GDI the source of the PMOS is not connected to VDD as compared to conventional CMOS as well as the source of the NMOS is not grounded.. Due to this important change in the design, GDI based circuit have two extra input pins for the use.

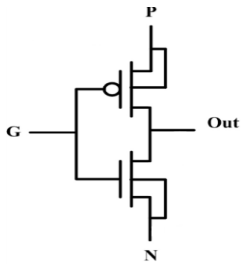

Fig 1: Basic GDI Structure

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	NOT
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX

Table 1: Truth table of the basic GDI cell

This modification makes GDI design more flexible as compared to the CMOS design. GDI cell have three inputs. The first input is G (common gate input of NMOS and PMOS), second one is P (input to the source/drain of PMOS) and the last one is N (input to the source/drain of NMOS). Bulk of both NMOS and PMOS are connected to N and P respectively. The main issue with GDI is due to the requirement of the twin-well CMOS or silicon on insulator (SOI) process to realize. Due to this major issue it will be more expensive to realize a GDI chip. Another factor with GDI that it will face the problem of lacking driving capability due to the use of standard p-well CMOS process which makes it more expensive and difficult to realize as a feasible chip.

In the Figure 2, the SUM and CARRY cell is designed using GDI technique. In total it required minimum eight transistor to implement SUM and two transistors to implement CARRY cell. Part 1 of the design (XOR) is implemented using GDI technique and Part 2 is designed for SUM and CARRY using 'H' as input.

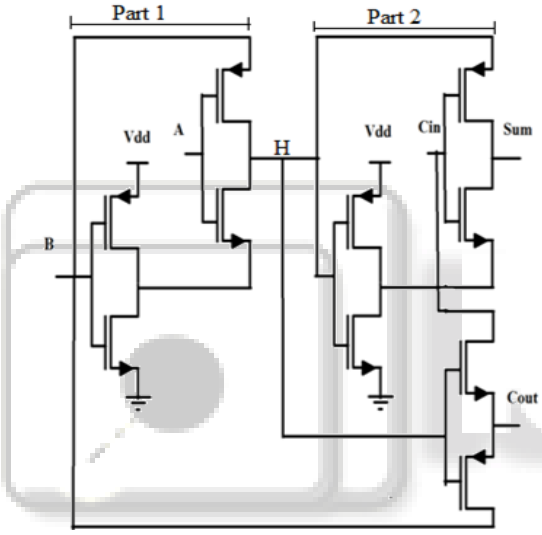

Fig. 2: Design of GDI full adder circuit

B. PTL-GDI Full Adder

The main difference in the designing of full adder using PTL-GDI [12] compared to others lies in the designing of SUM and CARRY. The SUM cell is designed using pass transistor logic (PTL) whereas the CARRY cell is designed using gate diffusion technique (GDI).

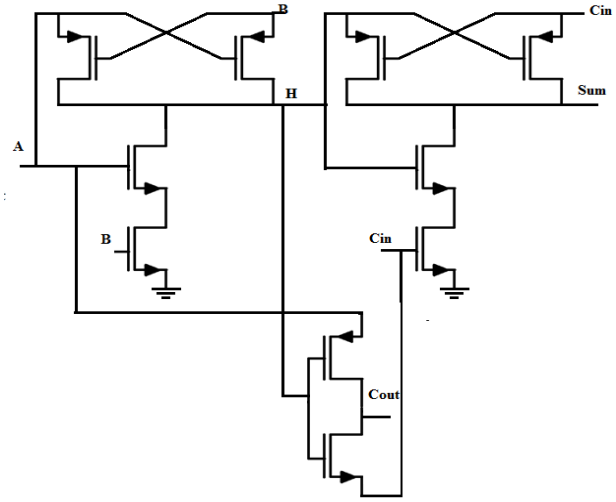

Fig. 3: PTL-GDI Full Adder

As shown in Figure 3, signal H is generated by the combination of two PMOS and two NMOS transistor whereas the SUM is obtained by using signal H which was generated earlier and C_{in}. To obtain SUM total eight transistors are used. CARRY cell is designed by using GDI technique as shown in Figure 3. For the calculation of carry signal, signal H is used as input to the gate and signal A and C_{in} variables are connected to the source of PMOS and NMOS respectively.

C. GDI-MUX Full Adder

To eliminate the need of complex XOR-XNOR gates, a GDI-MUX [14] approach with new methodology is reviewed. From the GDI based technique , C_{OUT} will be equal to A ANDING B when C_{IN} is equal to the '0' and C_{OUT} will be equal to A ORING B when C_{IN} is equal to the '1'. Thus a multiplexer can be used to obtain C_{OUT}. Also SUM is equal to A ORING B ORING C_{IN} when C_{OUT} is equal to '0' whereas SUM is equal to A ANDIND B ANDING C_{IN} when C_{OUT} is equal to '1'.

Hence, an alternative logic scheme to design a full adder cell can be formed by AND, OR and MUX logic blocks as shown in Figure 4. The GDI-MUX full adder provides low power high speed with full voltage swing.

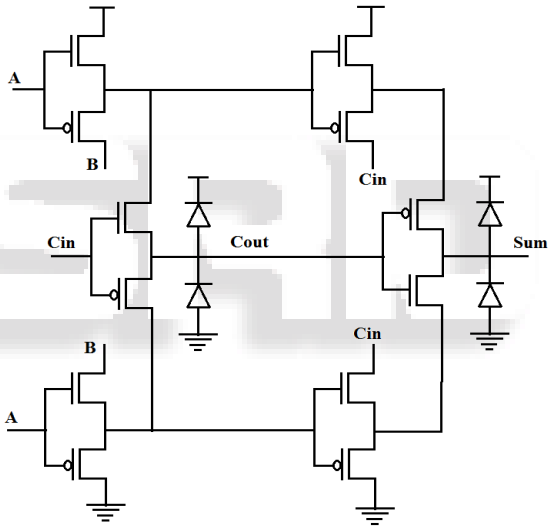

Fig. 4: GDI-MUX Full Adder

D. MGDI Full Adder

The main difference between GDI and modified- GDI [15,16] is that the bulk node of PMOS transistor is connected to V_{DD} and the bulk of NMOS transistor is connected to the ground in modified- GDI. Due to this MGDI is completely compatible for implementation in standard CMOS process of fabrication where bulk of all PMOS and NMOS are connected to V_{DD} and GND respectively. As shown in Figure 5, MGDI cell uses standard four terminal NMOS and PMOS transistors. They are implemented effortlessly in all type of standard CMOS technology. MGDI is quite suitable for the designing of high- speed, low power circuits and a broad range of other logic circuits as it offers less number of transistors, even as improving swing degradation and static power characteristics and allowing easy top-down design by using a small cell library.

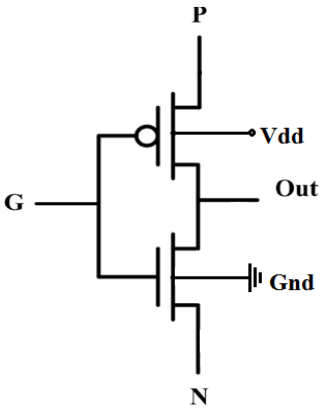

Fig. 5: MGDI Cell

Design of MGDI based full adder using 3T XOR gate is shown in Figure 6. The SUM is obtained by cascading 3T XOR gates and CARRY can be obtained by 2T MUX. The main advantage of MGDI based full adder is its high speed with the minimum number of transistor, delay and power dissipation.

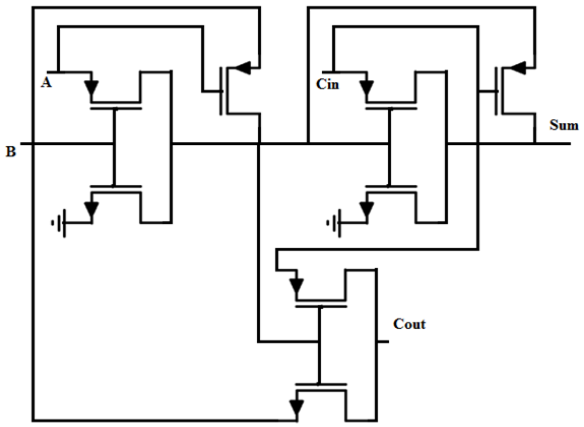

Fig. 6: Full adder based on MGDI

III. RESULTS

The comparison table of designing full adder using different techniques and different CMOS technology has been shown in Table 2.

Technique	Technology	Input Voltage	Number of Transistor	Power	Delay	Power Delay Product
GDI	180 nm	1.8V	10	1.054 µw	13.8 ps	0.020 fJ
PTL- GDI	180 nm	1.8V	10	1.053 µw	23.26 ps	0.026 fJ
GDI-MUX	130 nm	1.2 V	20	1.039 µw	36.72 ps	0.038fJ
M-GDI	45 nm	1.2 V	8	0.409 µw	1.651 ps	0.675aJ
CMOS	180 nm	1.2 V	28	2.12 µw	0.531 ps	1.126 fJ
CPL	180 nm	1.2 V	32	2.64 µw	0.321 ps	0.847 fJ
TFA	180 nm	1.2 V	16	3.60 µw	0.511 ns	1.840 fJ
TGA	180 nm	1.2 V	20	3.30 µw	0.497 ns	1.640 fJ

Table 2: Comparison Table

From the table 2 it can be concluded that the minimum number of transistor to design a full adder is using M-GDI technique. Also in terms of power M-GDI have minimum power and also minimum power delay product which is high in demand in today's scenario.

IV. CONCLUSION

From comparative analysis and review study it is concluded that M-GDI is the best known technique for the designing of full adder as compared to other techniques reviewed in this research activity. It succeeds in targeting the goal of power minimization. To add further using M-GDI technique other full adder designs can also be implemented to achieve power minimization.

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