A Review on Designing of Two Stage, Three Stage and Multistage Operational Amplifiers using Nanometer Scaling for CMOS

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Abstract— This paper deals with the review for design of a 2 stage and 3 stage CMOS operational amplifier, also a pad frame and analyze the effect of various parameters on the characteristics of operational amplifier, which operates at 5V power supply using 50 nm, C5 process CMOS technology. Here parameters are computed and response curves are computed between all characteristics such as Gain, PM, GBW, Slew Rate etc using AC, DC and transient characteristics of it. The operational amplifier, design is a two-stage, three-stage, multi-stage CMOS operational amplifier. The operational amplifier is designed to exhibit properties a unity gain frequency of 75-100 MHz and exhibits a gain of 77.25dB with a 60° or more phase margin. There is numerous numbers of configurations for operational amplifier exists in literature. The classification of the namely existing topologies includes single stage, two stage, three stage and multistage amplifiers. By results and reasons two stage and three stage topologies are suitable choices for low voltage and high performance applications. A pad frame design is also reviewed for all possible configurations of operational amplifier.

Key words: CMOS Analog Circuit, C5 Process, 2 stage CMOS Operational Amplifier, 3 stage CMOS Operational Amplifier, Stability, UGB, Device Design, CMRR, Differential Amplifier

I. INTRODUCTION

Designing high-performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in an analog circuit is the operational amplifier [1]. While digital circuits can take full advantage of shorter device lengths in modern CMOS processes, low noise analog circuits are generally constrained by short channel effects [2]. An operational amplifier is a fundamental building block in analog integrated circuit design and is used to realize functions ranging from DC bias generation to high speed amplification or filtering. There is numerous numbers of configurations for Operational amplifiers exist in literature. The classification of the namely existing topologies includes single stage, two stage, three stage and multistage amplifiers.

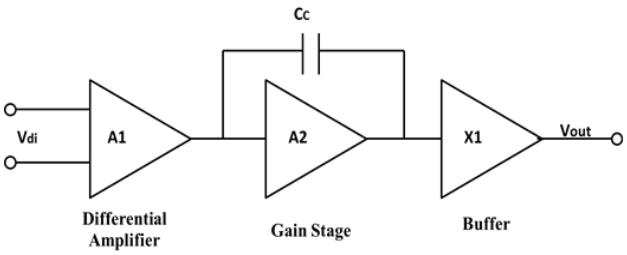

Fig. 1: Block Diagram of two stage operational Amplifier with output buffer [3]

II. DIFFERENTIAL AMPLIFIER

The basic building block in an Op-amp circuit is the differential amplifier or an Op-amp can be said to be made of a series of differential amplifiers similar to shown in the below figure. A differential amplifier will only amplify a differential signal between its inputs while it will suppress common mode signals. Before jumping to Operational Amplifiers, a brief section explaining various features of an operational amplifier is as follows. Current Iss/2 will flow through MOS transistors M1 and M2 respectively satisfying Idd= Iss/2.

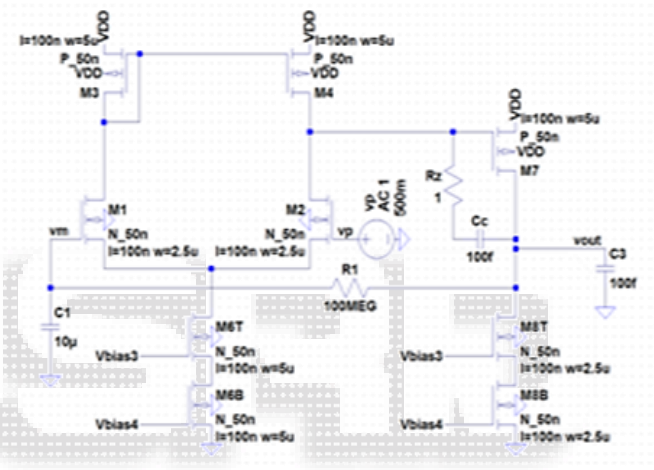

Fig. 2: Differential Amplifier [3]

To understand the functionality of the differential amplifier, let us assume that voltage v can vary from Vin1-Vin2 can vary from VDD to Vss. If Vin1 is much more negative than Vin2, M1 is off with zero Id1current, M2 has a current Id2=Iss. Voltage Vout1 is equal to VDD while Vout2 is equal to (VDD –Iss *Rd). If Vin1 is bought closer to Vin2 then M1 turns on having a non zero current Id1, again satisfying Iss= Id1+Id2 . If Vin1 is much more positive than Vin2, then all the current Iss will flow through transistor M1 while transistor M2 will be off.

DC Transfer characteristic function, output currents will be a function of voltage. The above simulation was performed using LTSpice using C5 model. The currents Id (M1) and Id (M2) will plotted against a suitable range of voltage.

III. TECHNOLOGY USED

This non-silicided CMOS process has 3 metal layers and 2 poly layers, and a high resistance layer. Stacked contacts are supported. The process is for 5 volt applications [4].

A. *Features*

- 2 or 3 metal layers
- Poly to poly capacitors
- EEPROM

– Schottky diodes
– High voltage I/O – 12/20 V
– High-resistance poly
– Low-voltage modules

S.NO	CHARACTERISTIC	VALUE
1.	Operating Voltage	5, 12 V
2.	Substrate Material	p-type, bulk or EPI
3.	Drawn Transistor Length	0.6 µm
4.	Gate Oxide Thickness	13.5 nm
5.	Contact/Via Size	0.5 µm
6.	Contacted Gate Pitch	3.9 µm
7.	Top Metal Thickness	675 nm
8.	Contacted Metal pitch	
	Metal 1	1.5µm
	Metal 2,3	1.6µm
9.	Metal composition	TiN/AlCu/TiN

Table 1. Process Characteristics [4]

IV. DESIGN PROCEDURE

To design a high performance and low power Operational amplifier this must meet the following minimum performance applications while driving a specific capacitive load of certain value

1) A unity gain frequency (ft) of _75- 100Mhz_ frequency of greater.
2) A low frequency gain of __ dB or greater
3) A phase margin of at least 60'
4) An input common mode range and output common mode range of +1 with no visible distortion of signals between these values.
5) A pad frame that fits layouts of all individual circuits with a certain load capacitor
6) Using 300nm, 3 metal process for design.
7) Circuits will be judged on the basis of AC and transient responses.

Overall methodology can be summarized as follows

1) Choosing the basic structure of the OpAmp.
2) Selection of the d.c currents and transistor sizes.
3) Measurement and Optimization of Design parameters
4) Physical implementation of the design, layout of transistors.
5) Pad frame / Fabrication

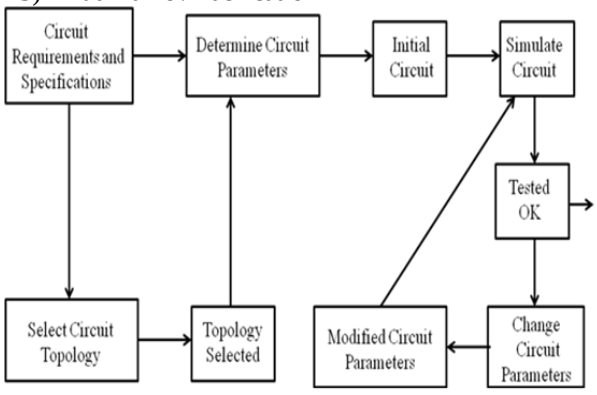

Fig. 3: Design Flow[3]

A. Design Technology For CMOS VLSI Design

As the manufacturing technology moves forward the ability to reap the full potential of available transistors and interconnect is increasingly important Design technology is concerned with the automated or semi automated conception, synthesis and verification and eventually testing of microelectronic systems. The design technology faces fundamental limitation in the computational intractability of the design optimizations.

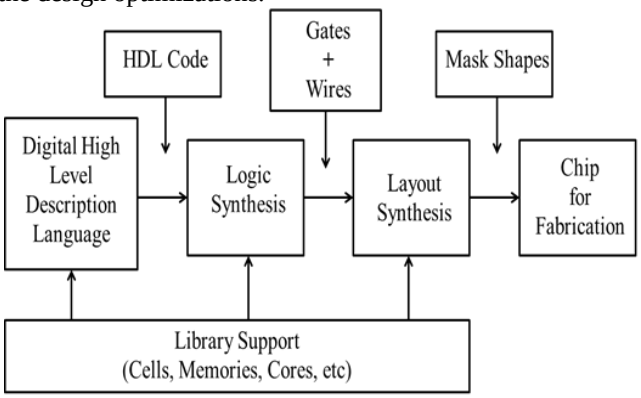

Fig. 4: Co-evolution of tools and methodology

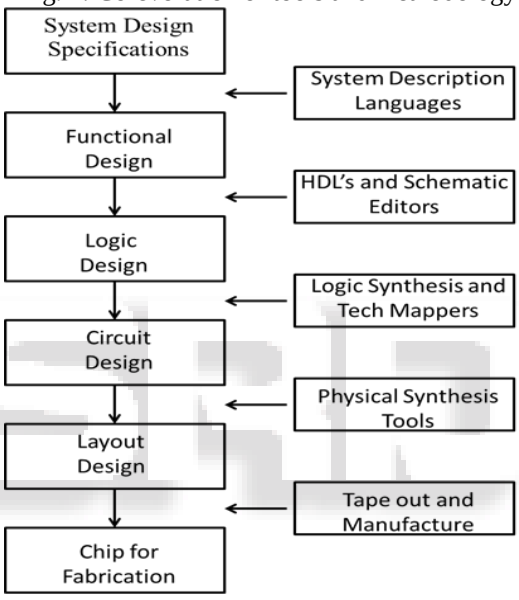

Fig. 5: Traditional VLSI Design Flow [16]

V. EXPECTED OUTCOME OF PROPOSED DESIGN

The Operational Amplifiers are designed to exhibit properties with unity gain frequency of approximately 25 MHz, gain of 77.25dB and a phase margin of 60o or more. The design and simulations carried out to achieve these values are also approximated. Two stage and three stage configurations are suitable choices for low voltage and high performance applications. X. Limitations and Challenges to be overcome in CAD tools [3]

In this section, various established and emerging design quality metrics and the main challenges of CAD tools to effectively predict, analyze their interactions, and optimize them in the CMOS technology were discussed. In the last few years, the research developers have witnessed increasing levels of interactions between physical, logical, and functional realms in the synthesis of VLSI circuit and systems. Various approaches with varying levels of interactions between the synthesis and layout phases have been proposed. These techniques are classified into several classes:

A. Gain-Based Synthesis

It is based on logical effort theory, which performs the gate sizing based on logical effort, electrical effort and timing constraints. The succeeding layout phase, is then performed with additional timing and capacitance constraints to meet the initial gate sizing decision. Appropriate circuit libraries are must.

B. Layout-Friendly Synthesis

Here, Synthesis of layout implications is given more importance. The wire planning is a best example for this type of synthesis. The research developers use the placement of I/O pins to achieve a layout-friendly logic factorization.
C. Layout-Driven Synthesis: In this synthesis depends on companion, layout/placement of various parts of the logic. After synthesis nodes may get created or deleted, and the companion layout may need to be updated to reflect these changes. The benefit of having a companion layout view is access to a more realistic estimates about the interconnect parasitics. This would allow the synthesis phase to make better decisions, while optimizing the logic.

C. Integrated Synthesis And Layout

The ultimate integration of the synthesis and layout phases were carried out by this class.

D. Synthesis-Driven Layout

This category consists of those techniques which perform layout optimization moves either within the synthesis phase or in a post-layout phase where synthesis and layout optimizations are applied to improve the design or meet the performance constraints.

E. Synthesis-Friendly Layout

This type of synthesis consists of layout synthesis algorithms and environments which is capable of withstanding functional and logic changes, with minimal disruption to the layout.

VI. CONCLUSIONS

Keeping in view different applications the Op-amp design has been proposed. For this first a selection is made for the active device used. The development of a design procedure provides a quick, well integrated and effective mechanism for estimation and calculation of various parameters. The steps highlighted make it easy to redesign the circuit for various set of specifications. The responses are simulated using LTSpice and Electric VLSI CAD design tool. The simulated results of the Op-amp will be in compliance with the theoretical values

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