High Fault Coverage for On Chip Network Using Priority Based Routing Algorithm

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Abstract— Network on chip is an interconnection between several processing elements and routers. There are several possibilities for the occurrence of faults within the network. These faults degrade the performance of the network. In order to increase the performance several fault tolerant methods has been used. They involve themselves in rerouting and hence take longer paths. To make the path shorter, the router architecture has to be modified. For this efficient routers are needed to take place communication between these devices. This project, proposes a priority based solution for a bufferless network-on-chip, including an on-line fault-diagnosis mechanism to detect both transient and permanent faults, a hybrid automatic repeat request and forward error correction link-level error control scheme to handle transient faults.

Key words: Chip network, Bufferless Network

I. INTRODUCTION

Network-on-Chip (NoC) has already become a promising solution for integrating a large number of cores on a chip to achieve high performance. However, as the CMOS technology scales down to the nanometer domain, smaller feature size, lower voltages and higher frequencies increase the number of occurrence of intermittent and transient faults besides manufacturing defects and wear out. NoC approach has emerged as a promising solution for on-chip communications to enable integrating various processors and on-chip memories into a single chip.

The recent technology in VLSI has made the chip to be much smaller in size. To make it possible, the inner modules and their interconnections are brought into small size. Networks-on-Chip (NoC) has emerged as a promising solution for on-chip interconnection in Multi Core NoCs due to its scalability, reusability, flexibility, and parallelism. NoC consists of Network Interfaces, Routers, set of links interconnecting the Routers and a defined communication protocol for IP core interaction. NoC architecture design follows the computation architecture design, which partitions a behaviour model and maps it onto an computation architecture model. The first step is communication modelling and analysis. The second step is topology and protocol design based on the communication.

Faults refer to the failure of the system. Transient and permanent faults are two different types of faults that can occur in on-chip networks.Transient faults are temporary and unpredictable. They are often difficult to be detected and corrected. Permanent faults are caused by physical damages such as manufacturing defects and device wear-out. These faults should be recovered or tolerated in a way that the network continues functioning. A deterministic routing algorithm uses a fixed path for each pair of nodes resulting in increased packet latency especially in congested networks.

In order to avoid transient and permanent faults a fault-tolerant solution, including an on-line fault diagnosis mechanism, a link-level error control scheme, and a fault tolerant routing algorithm is proposed for the bufferless NoC.

There are mainly three techniques to handle transient faults in NoC and they are Automatic repeat request (ARQ), Forward error correction (FEC), and Hybrid ARQ (HARQ). Also transient faults can be handled at both link-level and transport level. In ARQ-based error control the packet is retransmitted if it is found to have errors. Such packets are retransmitted until it is received error free. The error detection is usually implemented through a cyclic redundancy check (CRC). A simple errordetecting code is applied to the packet before transmitting, and at the receiver side a checksum will be calculated to ensure that no error has occurred. If the checksum does not add up to the right value, the packet is retransmitted.

The Efficient Rank Based fault-tolerant solution guarantees zero lost packets as long as the fault pattern does not cut the network into two or more disconnected parts. Simulation results demonstrate that under synthetic workloads, in the presence of permanent link faults, the throughput of an 8 × 8 network with Priority-based routing algorithm is 14% higher on average.

II. MINIMAL ROUTING ALGORITHM

The introduction of minimal routing algorithm for faults in the network increases the overall performance of the network. When we use the algorithm, it takes shortest path regardless of the presence of faults. The proposed algorithm is much simpler than the previous existing algorithm. It provides link among the surviving routers in the network. It proves to be more efficient even in the presence of multiple faults. It has the ability to connect the routers both horizontally and orthogonally even in the presence of faults. The fault tolerant algorithm is used to tolerate the number of faults present in the entire network. It supports the faulty router by taking non minimal paths. Due to the characteristics of adaptiveness, the data chooses different path by bypassing the faulty router to reach the destination router from the source router

III. FAULT-TOLERANT DEFLECTION ROUTING (FTDR) ALGORITHM

In order to have a high throughput system one must have system which should handle both transient faults and permanent faults. In our existing work we have methods like hybrid ARQ scheme to avoid transient faults. But we must also incorporate algorithms which can handle permanent faults. It has reduced delay over the network. It has proved to be more reliable of 99.5% when multiple faults are found in the network. It also helps to estimate the various

parameters such as reliability, latency, speed, area and power. FTDR algorithm makes routing decision based on the packet priority and routing table. First, the algorithm always gives the highest priority to the oldest packet. Given a network size and different fault patterns, the length of the hop count must be enough to guarantee the priority can not saturate. Second, it can be proved that the routing table entry will converge to the minimum hops to each destination.

IV. CONCLUSION

In this project, I provided a Efficient Rank Based fault-tolerant solution for a bufferless NoC to protect it from faults and achieved low latency. It provide the required communications at a low cost and system will be scalable

V. RESULTS

Without Fault

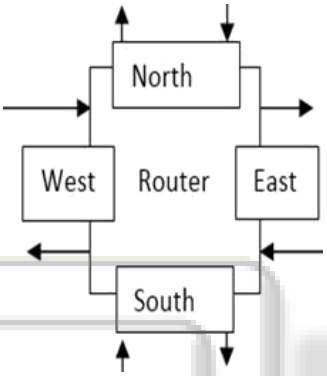

Fig. 1: Priority Based Routing

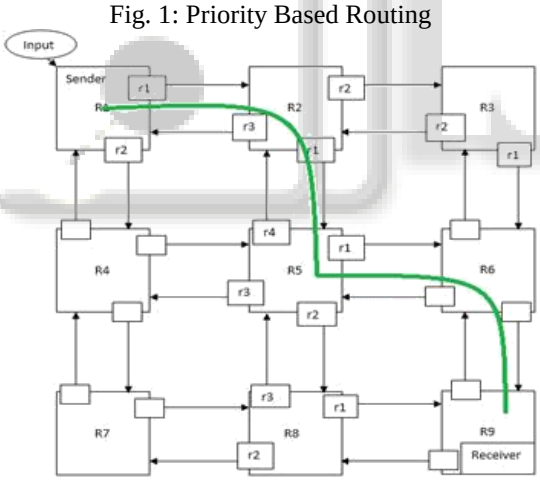

Fig. 2: Priority Based Routing Without Fault

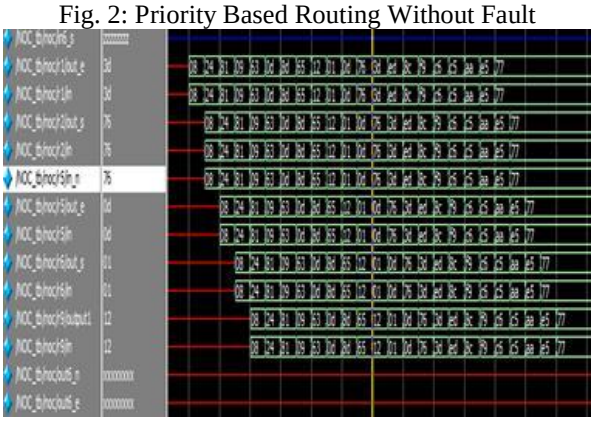

Fig. 3: Output Waveforms for without fault routing

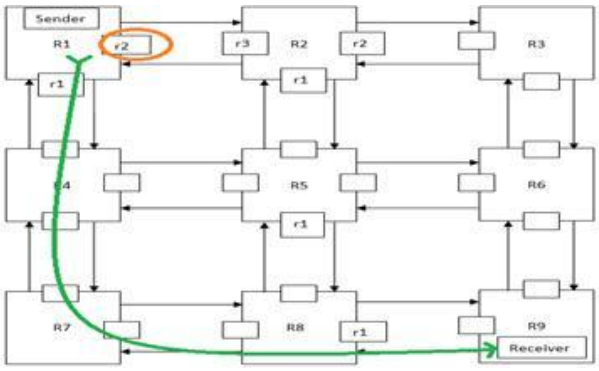

Fig. 4: Priority Based Routing with fault on Router1 at EAST

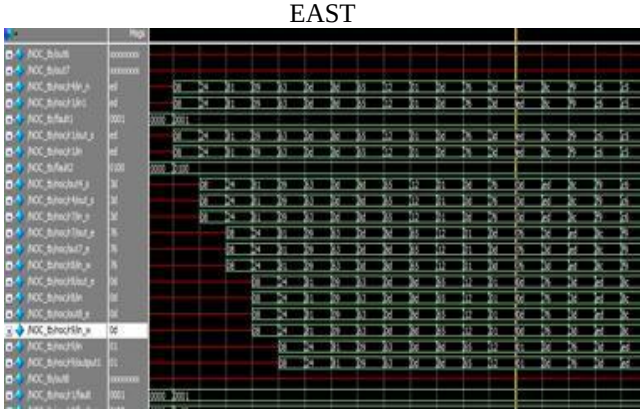

Fig. 5: Output Waveforms with fault on Router1 at EAST

ACKNOWLEDGEMENT

I would like to thank" Ms.Channpreet Kaur Toor" under whose guidance I completed my review paper. This review would not have been possible without the support and guidance given by her.

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