A high accuracy, Low power, Reproducible temperature telemetry System

Ankur Sharma[1] Gaurav Soni[2]
[1,2]Electronics and Communication
[1.2]Poornima College of Engineering

Abstract— Sense amplifiers are extensively used in memory. Sense amplifiers are one of the most vital circuits in the periphery of CMOS memories. We know that memory is the heart of all digital systems. Today all worlds are demanding high speed and low power dissipation as well as small area. We know that speed and power dissipation of memory is overall depends upon the sense amplifier we used and their performance strongly affects both memory access time, and overall memory power dissipation. So it is important to design a good sense amplifier which performs well in both speed and power dissipation. In this dissertation, an implementation of a most efficient sense amplifier is done by comparing the best known sense amplifier in today. The dissertation focuses on design, simulation and performance analysis of sense amplifiers. In this thesis, current latch sense amplifier and body bias controlled current latch sense amplifier are designed and results compared. The result shows that the body bias controlled current latch sense amplifier is performing best. The result also shows a novel sense amplifier which consumes small power at same time its speed is faster than other sense amplifiers.

Keywords: CMOS, memory access time, SRAMs

I. INTRODUCTION

Digital system design in an amazing and emerging field now days. Each and every digital system has adequate memories. In memory today the CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuit. SRAMs are used as large caches in microprocessor cores and serve as storage in various inputs on a system-on-chip like graphics, audio, video and image processors. SRAMs also used in high performance microprocessors and graphics chips so for each generation to bridge the increasing divergence in the speeds of the processor and the main memory we need high speed requirements. At the same time, SRAMs used in application processors which go into mobile, handheld and consumer devices have very low power requirements. So power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances. As with other integrated circuits today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation.

To read the contents of this memory a sense amplifier is used. The sense amplifier converts the arbitrary logic levels of bitlines to the digital logic levels which required running the peripheral Boolean circuits of outside world of memory. In the SRAM data path, switching of the bitlines, I/O lines and biasing the sense amplifiers consume a significant fraction of the total power. Mainly performance of memory depends on the performance of SA such as delay and power dissipation.

So the sense amplifier is one of the most circuits in the periphery of CMOS memories. Speed and power dissipation of the memory is mainly depends on types of sense amplifier used. So performance of SA strongly affects both memory access time, and overall memory power dissipation.

II. SENSE AMPLIFIER

A sense amplifier is an active analog circuit that reduces the time of signal propagation from an accessed memory cell to the logic circuit located at the periphery of the memory cell array, and used to detect small variation on bitlines of memory and produce full voltage swing it means that converts the arbitrary logic levels occurring on a bitline to the digital logic levels of the peripheral Boolean circuits. The sense amplifier circuit has to operate within the conditions which are set by the operation margins. Operation margins in a digital circuit are those domains of voltages, current and charges. These domains unambiguously represent data throughout the entire operation range of the circuit. Operation margin depends on the circuit design, processing technology and environmental conditions. Sense amplifiers, used with memory cells, are key elements in defining the performance and environmental tolerance of CMOS memories. Because of their great importance in memory designs, sense amplifiers became a very large circuit-class. CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuits, and appear in an amazing variety of circuit organizations.

$$A_{\downarrow}d = -g_{\downarrow}m\,(r_{\downarrow}(d\,)\,\|R_{\downarrow}L)$$
$$A_{\downarrow}C = (-\mathbf{g_{\downarrow}(m\,)}\,(r_{\downarrow}d\,\|\mathbf{R_{\downarrow}L}))/(\mathbf{1} + \mathbf{2g_{\downarrow}}m\,R_{\downarrow}S\,)$$
$$\Delta v_O = -2(r_d \,\|\, R_L)[(V_{PR} - v_S) - V_T(V_{BS})]\Delta v_i$$

III. IPLEMENTATION AND SIMULATION OF SENSE AMPLIFIERS

As previously discussed in chapters about various sense amplifiers, it is found that some sense amplifier consume less power but with more delay than other consume slightly more power but speed (with less delay) is relatively large. In this dissertation I propose a new sensing scheme which has less delay, more sensitivity than previously discussed with less power consumption. This chapter divided into four parts.

- Current latch sense amplifier
- Latch operation
- The Sizing Consideration
- Body-biased controlled Current latch sense amplifier

All rights reserved by *www.ijsrd.com*

These sense amplifiers made using with the help of Tanner tool V13.1.

IV. CIRCUIT CONFIGURATION

It consists of 5 nMOS and 4pMOS transistors namely MN1, MN2, MN3, MN4, and MN5.

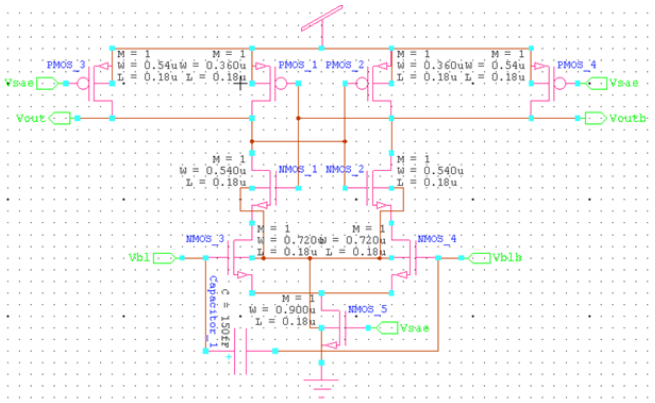

Fig. 1:. Current Latch Sense Amplifier (CLSA)

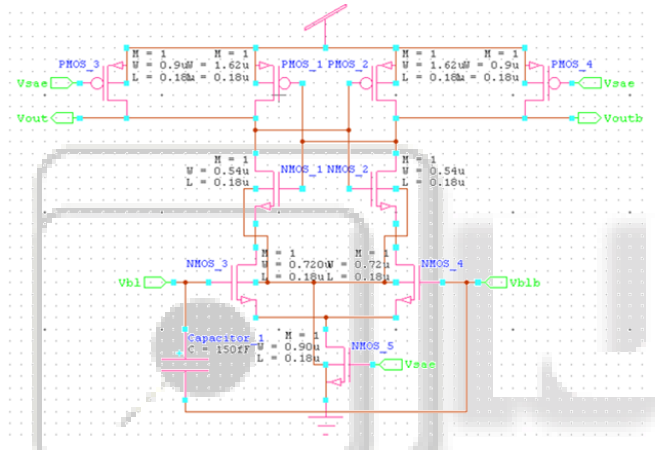

Fig. 2: Current Latch Sense Amplifier (CLSA) with different W/L ratio

V. SIMULATION RESULTS

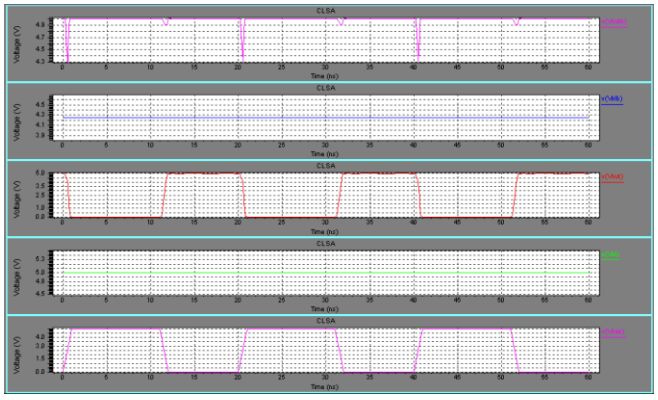

Fig. 3: Simulation waveforms of the Current Latch Sense Amplifier (CLSA) (a) for Bit Voltage (b) For Constant Voltage Difference

Vsae	Vbl	Vblb	Vout	Voutb	Remark
5V	5V	4.5 V	0V	5V	In sense mode
0V	5V	4.5 V	5V	5V	In pre-charge mode
5V	4.5V	5 V	5V	0V	In sense mode
0V	4.5V	5 V	5V	5V	In pre-charge mode

Table 1: CLSA operation

VI. CONCLUSION AND FUTURE SCOPE

In this chapter I summarize the conclusion for the proposed design and also explained about future scope.

A. Conclusion

In this dissertation Body Bias Controlled Current Latch Sense Amplifier has been designed and simulated using 180nm CMOS technology of tanner tool at a various supply voltage from1.0V to 5.0V. A Sense Amplifier is specially proposed in this dissertation as it is the heart of the Memory. Especially I proposed a BB-CLSA for low power and high speed operations in SRAM. This proposed Sense amplifier is compared with nearest basic Current Latch Sense amplifier as

- The power consumption of proposed BB-CLSA has been reduced from 47% to 87% compared to conventional CLSA.
- Speed of proposed Sense amplifier is increased by 10% as compared to conventional CLSA.
- Noise Margin and Sensitivity of proposed sense amplifier is improved considerably.
- Body Bias method is used for high speed at low power dissipation operation.
- Only 44% more transistors are used to reduce about 87% power dissipation and to get 10% more high speed operation.

B. Future Scope

However some aspects of the goal have been achieved using this design, but still a better Sense Amplifier can be build by some improvement in the circuit design. The SA can be further extended and modified by the following points.

- Delay can be further reduced by improving circuit design.
- Affect of process variations and corner variations on the performance of the proposed sense amplifiers are not included. So effects of these variations are removed by proper design of circuits and accurate simulations.
- Yield measurements can be done
- The layout can also be designed using L-Edit of tanner tool by which area can be calculated for chip fabrication.
- Body Bias Voltage Latch Sense amplifier is designed for high speed operation.
- In this design we use 180 nm technologies but latest technology 28nm and more can be used for batter design and analysis.
- The layout can also be designed using L-Edit of tanner tool by which area can be calculated for chip fabrication
- The delay and power dissipation can also reduced by using low power and high speed techniques like VTCMOS, DTCMOS, and Adaptive CMOS and Adiabatic logic technology.

All rights reserved by *www.ijsrd.com*

REFERENCES

[1] Yen-Huei Chen, Shao-Yu Chou, Quincy Li, Wei-Min Chan, Dar Sun, Hung-Jen Liao, Ping Wang, Meng-Fan Chang, and Hiroyuki Yamauchi, "Compact measurement Schemes for Bit-Line Swing, Sense Amplifier Offset Voltage, and Word-Line Pulse Width to Characterize Sensing Tolerance Margin in a 40 nm Fully Functional Embedded SRAM" , *IEEE Journal Of Solid-State Circuits*, Vol. 47,pp.1-12, No. 4, April 2012.

[2] Ravi Dutt and Abhijeet. "Current Mode Sense Amplifier for SRAM Memory", *International Journal of Engineering Research & Technology (IJERT)* Vol. 1 Issue 3, pp.1-4, May – 2012.

[3] Maurice Meijer and José Pineda de Gyvez, "Body-Bias-Driven Design Strategy for Area- and Performance-Efficient CMOS Circuits", *IEEE Transactions On Very Large Scale Integration (VLSI) Systems*, Vol. 20, No. 1, pp. 42-51, January 2012.

[4] Vibhu Sharma, Stefan Cosemans, Maryam Ashouei, Jos Huisken, Francky Catthoor, and Wim Dehaene, "8T SRAM with Mimicked Negative Bit-Lines and Charge Limited Sequential Sense Amplifier for Wireless Sensor Nodes", *IEEE Journal Of Solid-State Circuits*, 978-1-4577-0704-9/10pp. 531-534, 2012.

[5] Sampath Kumar Sanjay Kr Singh, Arti Noor, D. S. Chauhan and B.K. Kaushik, "Comparative Study of Different Sense Amplifiers In Submicron CMOS Technology", *International Journal of Advances in Engineering & Technology*, Vol. 1, Issue 5, pp. 342-350, Nov 2011.

[6] Myoung Jin Lee, "A Sensing Noise Compensation Bit Line Sense Amplifier for Low Voltage Applications", *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 3, pp. 690-694, March 2011.

[7] Anh-Tuan Do, Zhi-Hui Kong, Kiat-Seng Yeo, and Jeremy Yung Shern, "Design and Sensitivity Analysis of a New Current-Mode Sense Amplifier for Low-Power SRAM", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 2, pp. 196-204, February 2011.

[8] Mohammad Sharifkhani, Ehsan Rahiminejad, Shah M. Jahinuzzaman and Manoj Sachdev, "A Compact Hybrid Current/Voltage Sense Amplifier with Offset Cancellation for High-Speed SRAMs", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 5, pp. 883-894, May 2011.

[9] MasoodQazi, Kevin Stawiasz, Leland Chang and Anantha P. Chandrakasan, "A 512kb 8T SRAM Macro Operating Down to 0.57V With an AC-Coupled Sense Amplifier and Embedded Data-Retention-Voltage Sensor in 45 nm SOI CMOS", *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 1, pp. 85-96, January 2011.

[10] Myoung Jin Lee, "A Sensing Noise Compensation Bit Line Sense Amplifier for Low Voltage Applications", *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 3, pp. 690-694, March 2011.

[11] Michael Wieckowski, Gregory K. Chen, Daeyeon Kim, David Blaauw and Dennis Sylvester, "A 128kb High Density Portless SRAM Using Hierarchical Bitlines and Thyristor Sense Amplifiers", *IEEE 12th Int'l Symposium on Quality Electronic Design*, pp. 87-90, 2011.

[12] Takashi Ohsawa, Kosuke Hatsuda, Katsuyuki Fujita, Fumiyoshi Matsuoka, and Tomoki Higashi, "Generation of Accurate Reference Current for Data Sensing in High-Density Memories by Averaging Multiple Pairs of Dummy Cells", *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 9, pp. 2148-2157, September 2011.

[13] Vibhu Sharma, Stefan Cosemans, Maryam Ashouei, JosHuisken and Wim Dehaene, "A 4.4 pJ/Access 80 MHz, 128 kbit Variability Resilient SRAM With Multi-Sized Sense Amplifier Redundancy", *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 10, pp. 2416-2430, October 2011.

[14] Joseph F. Ryan, Sudhanshu Khanna and Benton H, "An Analytical Model for Performance Yield of Nano Scale SRAM Accounting for the Sense Amplifier Strobe Signal", *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 297-302, August 2011.

[15] Yusuke Niki, Atsushi Kawasumi, Azuma Suzuki, Yasuhisa Takeyama, Osamu Hirabayashi, Keiichi Kushida, Fumihiko Tachibana and Tomoaki Yabe, "A Digitized Replica Bitline Delay Technique for Random-Variation-Tolerant Timing Generation of SRAM Sense Amplifiers", *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 11, pp. 2545-2551,November 2011.

[16] Vandana Niranjan, Ashwni Kumar and Shail Bala Jain, "Subthreshold Logic using Body-bias technique for Digital VLSI neural Applications", *IEEE 2013 International Conference on Machine Intelligence Research and Advancement*, pp. 316-320, December, 2013.

[17] Mohamed H. Abu-Rahma, Ying Chen, Wing Sy, Wee Ling Ong, Leon Yeow Ting, Sei Seung Yoon, Michael Han and Esin Terzioglu, "Characterization of SRAM Sense Amplifier Input Offset for Yield Prediction in 28nm CMOS", *IEEE Custom Integrated Circuits Conference (CICC)*, September 2011.

[18] Labonnah F. Rahman, Md. Syedul Amin M. B. I. Reaz and M. A. M. Ali, "Circuit of an EEPROM Sense Amplifier in 0.18 μm CMOS Technology", *IEEE TENCON* 978-1-4577-0255-6/11, pp. 642-645, 2011.

[19] LI Xi, CHEN Hou-Peng and SONG Zhi-Tang, "Design and analysis of a high-performance sense amplifier for Phase-Change Memory", *Computer Research and Development (ICCRD)*, Vol, 3, pp. 318-321, March 2011.

[20] Oghenekarho Okobiah, Saraju P. Mohanty, Elias Kougianos and Mahesh Poolakkaparambil, "Towards Robust Nano-CMOS Sense Amplifier Design: A Dual-Threshold versus Dual-Oxide Perspective", *GLSVLSI'11, May 2–4, 2011*, Lausanne, Switzerland.

[21] V.Mohana Vidya, R.Thilagavathy and M.Bhaskar, "Low Power, High Performance Current mode Transceiver for Network-on-Chip Communication", *IEEE Proceedings of 2011 International Conference on Signal Processing, Communication, Computing*

All rights reserved by *www.ijsrd.com*

and Networking Technologies(ICSCCN), pp. 223-227, July 2011.

[22] Anh-Tuan Do, Zhi-Hui Kong, and Kiat-Seng Yeo, "Criterion to Evaluate Input-Offset Voltage of a Latch-Type Sense Amplifier*", IEEE Transactions on Circuits and Systems-I: Regular Papers*, Vol. 57, No. 1, pp. 83-92, January 2010.

[23] Chua-Chin Wang, Chia-Hao Hsu, Chi-Chun Huang and Jun-Han Wu, "A Self-Disabled Sensing Technique for Content-Addressable Memories", *IEEE Transactions on Circuits and Systems—II: Express Briefs*, Vol. 57, No. 1, pp. 31-35, January 2010.

[24] Shien-Chun Luo and Lih-Yih Chiou, "A Sub-200-mV Voltage-Scalable SRAM with Tolerance of Access Failure by Self-Activated Bitline Sensing", *IEEE Transactions on Circuits and Systems—II: Express Briefs*, Vol. 57, No. 6, pp. 440-445, June 2010.

[25] Mohamed N. Elzeftawi, C. Patrick Yue, and Luke, "Design Challenges for Sense Amplifier and Wireless Link in High-Density Neural Recording Implants*", IEEE International Symposium on VLSI Design Automation and Test (VLSI-DAT)*, pp. 61-64, April 2010.

[26] Chia-Tsung Cheng, Yu-Chang Tsai and Kuo-Hsing Cheng, "A High-Speed Current Mode Sense Amplifier for Spin-Torque Transfer Magnetic Random Access Memory", *53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 181-184, August 2010.

[27] Taejoong Song, Sang Min Lee, Jaehyouk Choi, Stephen Kim, Gyuhong Kim, Kyutae Lim and Joy Laskar, "A Robust Latch-Type Sense Amplifier Using Adaptive Latch Resistance", *IEEE International Conference on IC Design and Technology (ICICDT)*, pp. 182-185, June 2010.

[28] Atsushi Kawasumi, Yasuhisa Takeyama, Osamu Hirabayashi, Keiichi Kushida, Yuki Fujimura, and Tomoaki Yabe, "A Low-Supply-Voltage-Operation SRAM With HCI Trimmed Sense Amplifiers", *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 11, pp. 2341-2347, November 2010.

[29] S.-H. Woo H. Kang K. Park S.-O. Jung, "Offset voltage estimation model for latch-type sense amplifiers", *IET Circuits Devices Syst*, Vol. 4, Iss. 6, pp. 503–513, 2010.

[30] Akira Kotabe, Yoshimitsu Yanagawa, Riichiro Takemura, Tomonori Sekiguchi and Kiyoo Itoh, "Asymmetric Cross-Coupled Sense Amplifier for Small-Sized 0.5-V Gigabit-DRAM Arrays", *IEEE Asian Solid-State Circuits Conference* November 8-10, 2010 / Beijing, China.

[31] Yinhui Chen, Zhiyuan Yu, Haiqing Nan, and Ken Choi, "Ultralow Power SRAM Design in Near Threshold Region using 45nm CMOS Technology ", *IEEE International Conference on Electro/Information Technology (EIT)*, May 2011.

[32] Syed Iftekhar Ali, M. S. Islam, "A High-Speed and Low-Power Ternary CAM Design Using Match-Line Segmentation and Feedback in Sense Amplifiers", *IEEE 13th International Conference on Computer and Information Technology*, pp. 221-226, 23-25 December, 2010, Dhaka, Bangladesh.

[33] Joseph F. Ryan and Benton H. Calhoun, "Minimizing Offset for Latching Voltage-Mode Sense Amplifiers for Sub-threshold Operation", *IEEE, 9th International Symposium on Quality Electronic Design*, pp. 127-132, 2008.

[34] Haitao Fu, Anh-Tuan Do, Kiat-Seng Yeo and Zhi-Hui Kong, "Design and Performance Evaluation of a Low-power Data-line SRAM Sense Amplifier", *IEEE Proceedings of the 2009 12th International Symposium on Integrated Circuits, ISIC*, December 2009.

[35] Stanley E. Schuster and Richard E. Matick, "Fast Low Power eDRAM Hierarchical Differential Sense Amplifier", *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 2, pp. 631-641 February 2009.

[36] Atsushi Kawasumi, Yasuhisa Takeyama, Osamu Hirabayashi, Keiichi Kushida, Yuki Fujimura and Tomoaki Yabe, "A Low Supply Voltage Operation SRAM with HCI trimmed Sense Amplifiers", *IEEE Asian Solid-State Circuits Conference November*, pp. 221-224, *16-18*, 2009 / Taipei, Taiwan.

[37] Tao Jiang, Patrick Y. Chiang, "Sense Amplifier Power and Delay Characterization for Operation under Low-Vdd and Low-Voltage Clock Swing", *IEEE International Symposium on Circuits and Systems*, pp. 181-184, May 2009.

[38] Mudit Bhargava, Mark P. McCartney, Alexander Hoefler, and Ken Mai, "Low-Overhead, Digital Offset Compensated, SRAM Sense Amplifiers", *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 705-708, 2009.

[39] Zhao Huizhuo and Xu Bingshi, "Design Ofthree Important Peripheral Circuits of SRAM Based on 9T Cell", *IEEE, Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics*, pp. 337-340, PrimeAsia 2009, January 2009.

[40] Ya-Chun Lai and Shi-Yu Huang, "A Resilient and Power-Efficient Automatic-Power- Down Sense Amplifier for SRAM Design", *IEEE Transactions on Circuits and Systems—II: Express Briefs*, Vol. 55, No. 10, pp. 1031-1035, October 2008.

[41] Anh-Tuan Do, Jeremy Low Yung Shern, Zhi-Hui Kong, Kiat-Seng Yeo, and Joshua Low Yung Lih, "A Full Current-mode Sense Amplifier for Low-power SRAM Applications", *IEEE Asia Pacific Conference on Circuits and Systems, APCCAS 2008* , pp. 1402-1405, Novomber-December,2008.

[42] Do Anh-Tuan, Kong Zhi-Hui, and Yeo Kiat-Seng, "Hybrid-Mode SRAM Sense Amplifiers: New Approach on Transistor Sizing", *IEEE Transactions on Circuits and Systems—II*: Express Briefs, Vol. 55, No. 10, pp. 986-990, October 2008.

[43] Daniël Schinkel, Eisse Mensink, Eric Klumperink, Ed van Tuijl and Bram Nauta, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time", *IEEE International Solid-State Circuits Conference* February, pp. 89-94, 2007.

[44] Hee-Bok Kang, Suk-Kyoung Hong, Heon-Yong Chang, Hae-Chan Park, Nam-Kyun Park, Man Young

All rights reserved by *www.ijsrd.com*

Sung, Jin-Hong Ahn, and Sung-Joo Hong, "A Sense Amplifier Scheme with Offset Cancellation for Giga-bit DRAM", *Journal Of Semiconductor Technology and Science*, Vol.7, No.2, pp. 67-75, June, 2007.

[45] Chun-Lung HSU, Mean-HomHO and Chin-Feng LIN, "New Current-Mirror Sense Amplifier Design for High-Speed SRAM Applications", *IEICE Trans. Fundamentals*, Vol.E89–A, No.2, pp. 377-384, February 2006.

[46] Manoj Sinha, Steven Hsu, Atila Alvandpour, Wayne Burleson, Ram Krishnamurthy, Shekhar Borkar, "High-Performance and Low-Voltage Sense-Amplifier Techniques for sub-90nm SRAM", *Proceedings. IEEE International [Systems-on-Chip] SOC Conference*, September 2003.

[47] Tsuguo Kobayashi, KazutakaNogami, Tsukasa Shirotori, and Yukihiro Fujimoto, "A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low -Power Architecture", *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 4, pp. 523-527, April 1993.

Books

[48] Jan M. Rabaey,Anantha P, Chandrakasan, Borivoje Nikolic, "digitan Intigrated circuits: a design perspective", *ISBN 978-81-317-0914-6*, Pearson Eduction,Inc,2009.

[49] Neil H.E.Weste, David Haris, Ayan Banerjee, "CMOS VLSI Design-A Circuits and Systems Perspective", Pearson Education, Inc, 2006.

[50] Sumo-Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", *ISBN 0-07-053077-7*, Tata McGraw-Hill Publishing Company Limited, 2003.

[51] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", *ISBN 0-07-052903-5*, Tata McGraw-Hill Publishing Company Limited, 2008.

[52] [52] Tegze P. Haraszti, "CMOS Memory Circuits", *ISBN 0-792-37950-0*, Kluwer Academic Publishers, 2002.

[53] Ben G. Streetman, "Solid State Electronic Devices", *ISBN 81-203-0692-9*, Prentice Hall of India Private Limited, 1994.

Paper Published

[54] Ratan Lal Regar, Kumkum Verma, Sanjay Kumar Jaiswal and Dheeraj Jain, "Design and Analysis of high Speed Body bias control and CLSA Sense Amplifier", *IEEE, 2013 International Conference on Machine Intelligence Research and Advancement*, pp. 383–386,December,2013,SMVDU, Katra, Jammu, India.

All rights reserved by *www.ijsrd.com*