Five level hybrid Cascaded multilevel inverter Harmonic reduced in PWM switching scheme

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Abstract— The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as a inverter. This paper describes a harmonics reduced in a hybrid cascaded multilevel inverter circuit with pulse width modulation (PWM) scheme. These scheme pulse width modulations in modified method are uses reduce switching device. These methods are a conventional inverter and hybrid inverter combine form. This topology used the combined form of a new five level hybrid cascaded multilevel inverter. The multilevel carrier based pulse width modulation methods are used in this topology five level output voltage wave forms is shown in FFT window MATLABE/SIMULINK is used to simulate the inverter circuit operation and control signals.

Key words: Multilevel Inverter (MLT), Hybrid Cascaded Multilevel Inverter, Pulse width modulation (PWM)

I. INTRODUCTION

The multilevel inverter [MLI] is a bright inverter topology for high voltage and high power applications. These inverter synthesizes several different levels of DC voltage to get a staircase (stepped) that access the pure sine waveform. It has high power superior waveforms, lour voltage ratings of devices, lour harmonic distortion, lour switching frequency and switching losses, higher efficiency and reduction of dv/dt stresses. Its gives a possibility of working with low speed semiconductors if its comparison with the two-level inverter. Numerous of MLI topologies and modulation techniques have been introduced and studied extensively. But most popular MLI topologies are Diode Clamp inverter, Flying Capacitor inverter and Cascaded Multilevel Inverter (CMLI). In this thesis we use a CMLI that consist of some H-Bridge inverters and with un-equal DC named as Asymmetric Cascaded Multilevel Inverter (ACMLI). It is implemented because these inverters are more modular and simple in construction and have other advantages than Diode clamp and flying capacitor.

II. MULTILEVEL INVERTER

Multilevel inverter is very versatile and is uses for power electronics topology for high power application. The multilevel inverter has a very low electromagnetic interference (EMI) and it efficiency is high compare to conventional inverter. Multilevel inverter is a latest alternative to implement low frequency based inverters with low output voltage distortion. Basic multilevel topologies are of three types. Figure 1.1 shown in bellow:-

All three topologies of a multilevel inverter can be used in reactive power compensation without having the voltage unbalance problem. Diode clamping is not needed in flying capacitor and cascaded inverter configuration and balancing capacitors are not needed in diode clamped and cascaded inverter configuration in cascaded inverter configuration requires the least number of components.

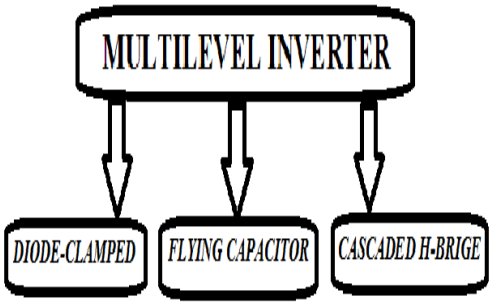

Fig. 1.1: Multilevel inverter topologies

A. *Diode-Clamped Multilevel*

The diode clamped topology is shown in fig 2.1 this inverter is also called as a neutral point converter. This figure shows a five level neutral point converter. It was the first widely popular multilevel inverter topology. It is extensively used in industrial application this three levels neutral point converter uses capacitor to generate intermediate voltage level and voltages across the switches are only half cycle in dc input. These inverters most commonly used in high power and medium power voltages. in these inverter topology diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus the main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each switch and each capacitor is Vdc.

1) Disadvantages

(1) Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.

(2) The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

B. *Flying Capacitor Inverter*

A similar topology to the Neutral-Point Clamped Multilevel Inverter topology is the Capacitor Clamped (CC), or Flying Capacitor, multilevel inverter topology, the Neutral-Point Clamped Multilevel Inverter (m-1) number of capacitors on a shared DC-bus, where m is the level number of the inverter, and 2(m-1) switch-diode valve pairs are used the flying capacitor topologies shown in figure 2.2. Flying capacitor inverter is a good alternative to overcome some of the neutral point clamped inverter topology. Drawbacks of this inverter topologies can be overcome by additional levels and voltage clamping. these topologies doesn't require additional clamped diode, and it provides a reduce switching states. That can be used to control the capacitor charge even under load with DC source.

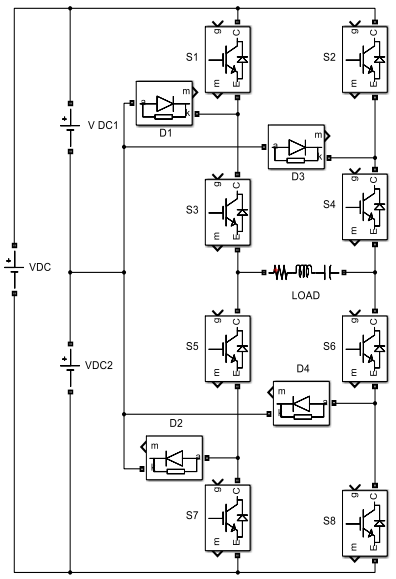

Fig. 2.1: Three level diode clamped MLI

1) Disadvantages

(1) Converter initialization i.e., before the converter can be modulated by any modulation scheme the capacitors must be set up with the required voltage level as the initial charge. This complicates the modulation process and becomes a hindrance to the operation of the converter.
(2) Control is complicated to track the voltage levels for all of the capacitors.
(3) Pre charging all of the capacitors to the same voltage level and startup are complex.
(4) Switching utilization and efficiency are poor for real power transmission.

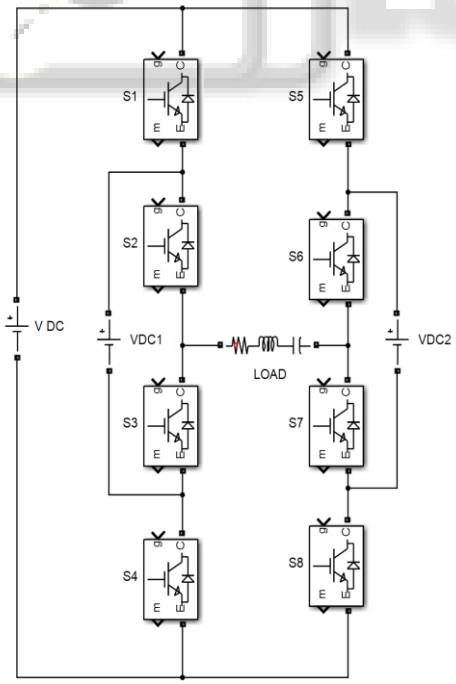

Fig. 2.2: flying capacitor multilevel inverter.

C. Cascaded H- Bridge Multilevel Inverter

The cascaded multilevel inverter topology consist of number of H bridge inverter unit with a separate DC source of each topology and are connected in cascaded or series circuit. Each H-bridge can produces different voltage levels. In figure 2.3 shown H-bridge multilevel inverter topologies which produces seven level output voltages, such as $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$. This topology uses 12 switches and 3 voltage sources as shown in figure 1.4.

1) Disadvantages

(1) Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.
(2) Needs separate dc sources for real power conversions, and thus its applications are somewhat limited

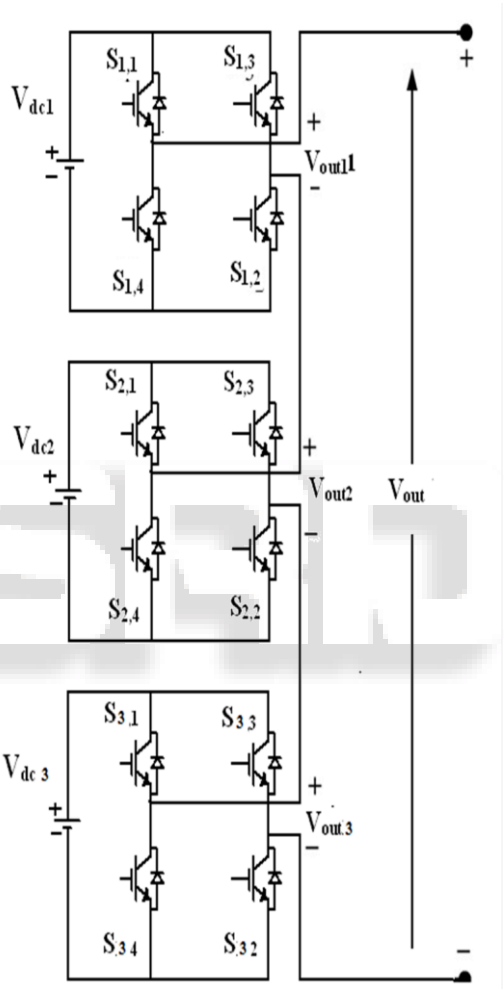

Fig. 2.3: cascaded H-bridge multilevel inverter

III. PROPOSED H-BRIDGE SYSTEM

A. Block Diagram Of Propesed Circuit.

This modified method shown in figure 3.1 Five level hybrid cascaded multilevel inverter with a pulse width modulation method is designed by reducing a number of switches hence reduces switching losses. These inverter topologies are used only six switches, two capacitors and two asymmetrical voltage sources.

This method is a combination of two inverter circuit first is a H-bridge inverter and another use conventional inverter, To form a new proposed five level cascaded H-bridge multilevel inverter. This topology uses a multi carrier based new PWM method, used to produced a

five level output voltage. This inverter circuit is used in a hybrid electric vehicles and electrical vehicles.

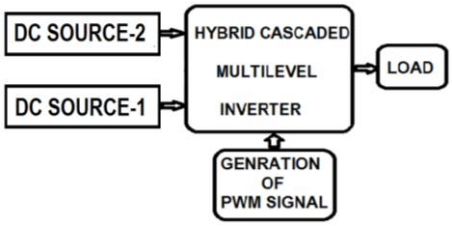

Fig. 3.1: Proposed block diagram.

B. Simulation Work

1) Simulation diagram

A simulation diagram are shown in a figure 3.2 using MATLAB/SIMULINK.

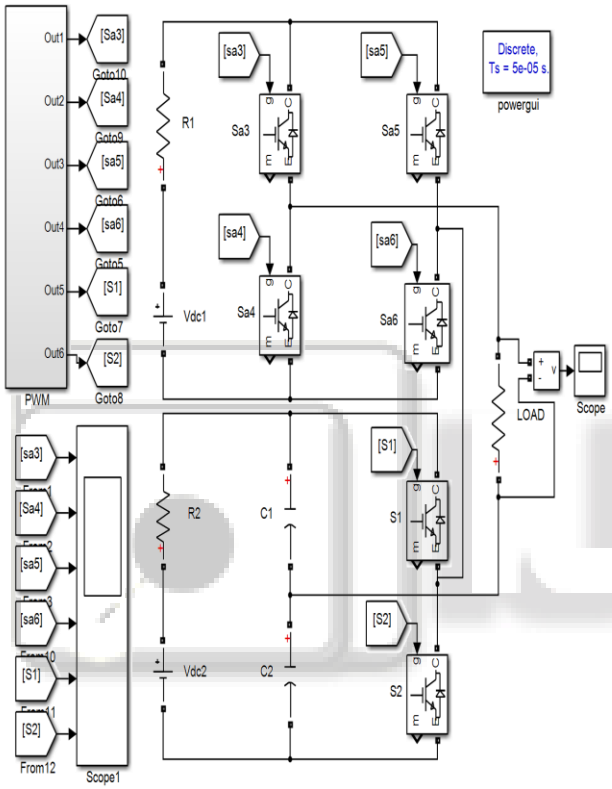

Fig. 3.2: five-level HMLI simulation diagram.

The simulation block diagram has five level hybrid multilevel inverter. This topology is H-bridge inverter and normal conventional inverters are combined to form a new hybrid multilevel inverters. The two inverter circuit are connected in cascaded manner .as shown in figure-3.2

2) Proposed PWM signal for hybrid multilevel inverter

Generation of pulse width modulation signal formula shown in tabel-1

S_n	Hybrid PWM mixing operator
S_{A1}	$A1$
S_{A2}	$\overline{A1}$
S_{A3}	$PWM \bullet ((A2 \bullet A1) + (\overline{A2} \bullet \overline{A1}))$
S_{A4}	$\overline{PWM} + ((A2 \bullet A1) + (\overline{A2} \bullet \overline{A1}))$
S_{A5}	$PWM \bullet ((A2 \bullet A1) + (\overline{A2} \bullet \overline{A1}))$
S_{A6}	$\overline{PWM} + ((A2 \bullet A1) + (\overline{A2} \bullet \overline{A1}))$

Table 1: Pulse Generation Formula

These pulses are given for six switches. one conventional inverter has a S_1, S_2, and H-bridge inverter has four pulse Sa_3, Sa_4, Sa_5, Sa_6. The figure 3.3 shows output of pulse width modulation. These are a new carrier based pulse width modulation output wave. This PWM signal generate a new proposed signals with a combination of logical operation as shown in table-1

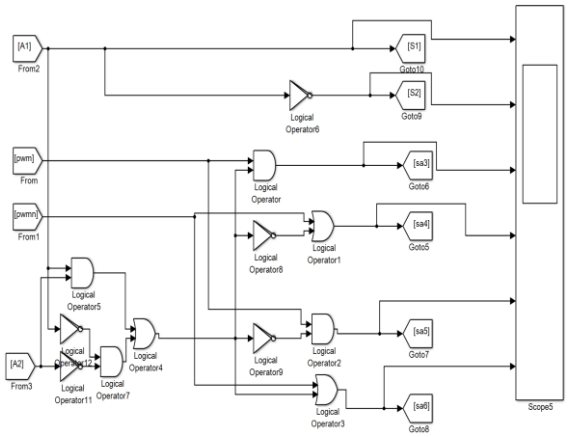

Fig. 3.3: Logic Diagram for five-level HMLI

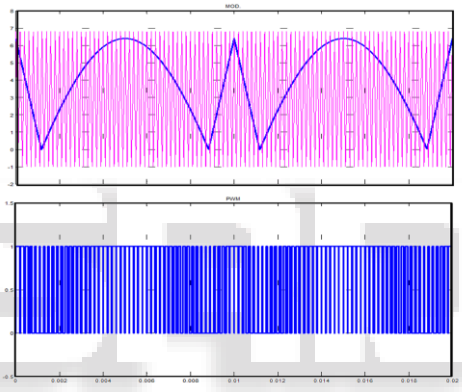

Fig. 3.4: output of a PWM

IV. RESULT

This new five level H-bridge cascaded multilevel inverter topologies are implemented in MATLAB/SIMULINK software. HMLI with six switches is shown in figure-3.2 and control signals for all six switches with new logical scheme, output wave forms are shown in figure - 4.1.

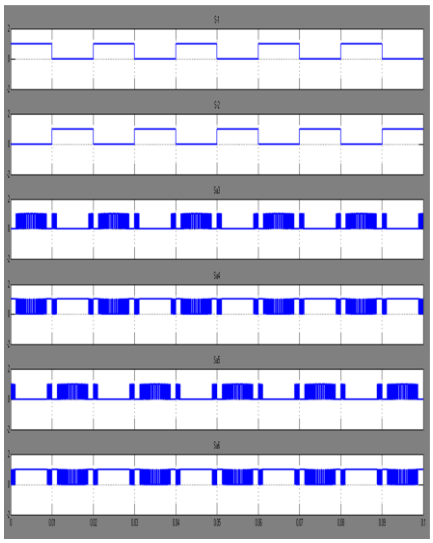

Fig. 4.1: control signals for five level HMLI.

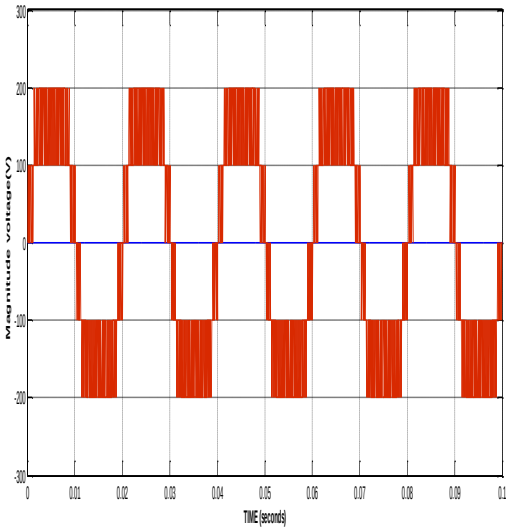

Fig. 4.2: output voltage waveform for five level hybrid cascaded multilevel inverter.

The output voltage waveform of a five level is designed using a MATLAB. My proposed work has a five level hybrid cascaded multilevel inverter. This uses only five switches for a five level.

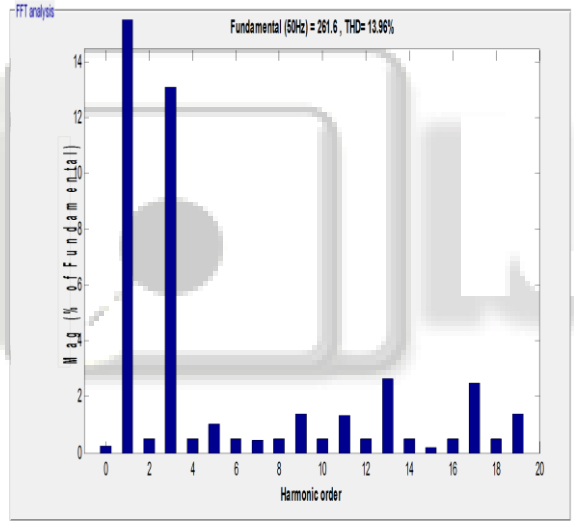

Fig. 4.3: FFT analysis for new five level hybrid cascaded multilevel inverter.

Figure 4.3 shows in THD (total harmonics distortion) value for a proposed H-bridge cascaded multilevel inverter circuit in a five level. This proposed circuit has THD-13.96% for a five level output voltage waveform.

The topology of an inverter circuit is based on the requirement and range. All topologies have both advantages and disadvantages. The two level inverters cost is very low as compared to other conventional inverter topologies. But very high value of THD. Then to reduce THD levels of a inverter voltage waveforms should be increased. And the number of level increases in a inverter then switching losses increased. Theses all above problems can be avoided by hybrid multilevel inverter.

V. CONCLUTION

This proposed inverter circuit the numbers of switches and their switching losses are reduced as compared to other five level conventional inverter circuit. This inverter topologies uses a new pulse width modulation scheme hence this inverter circuit is less complicated as compared to other five level conventional inverter circuit. This inverter topology has less harmonics and the total harmonics distortion can be analyzed through a powerful /FFT toolbox.

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