Verification of Four Port Router for NOC

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Abstract— The focus of this Paper is the actual implementation of Network Router and verifies the functionality of the four port router for network on chip using the latest verification methodologies, Hardware Verification Languages and EDA tools and qualify the IP for Synthesis an implementation. This Router design contains three output ports and one input port, it is packet based Protocol. This Design consists Registers and FIFO. For larger networks, where a direct-mapped approach is not feasible due to FPGA resource limitations, a virtualized timemultiplexed approach was used. Compared to the provided software reference implementation, our direct-mapped approach achieves three orders of magnitude speedup, while our virtualized time multiplexed approach achieves one to two orders of magnitude speedup, depending on the network and router configuration.

Keywords: Network-on-Chip, Simulation Router, FIFO, FSM, Register blocks

I. INTRODUCTION

90% of ASIC respins are due to functional bugs. As the functional verification decides the quality of the silicon, we spend 60% of the design cycle time only for the verification/simulation. In order to avoid the delay and meet the TTM, we use the latest verification methodologies and technologies and accelerate the verification process.

This project helps one to understand the complete functional verification process of complex ASICs an SoC's and it gives opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification.

II. FUNCTIONAL VERIFICATION APPROACHES

A. Black box verification

With a black-box approach, functional verification is performed without any knowledge of the actual implementation of a design. All verification is accomplished through the available interfaces, without direct access to the internal state of the design, without knowledge of its structure and implementation.

B. White box verification

As the name suggests, a white-box approach has full visibility and controllability of the internal structure and implementation of the design being verified.

C. Gray box verification

Grey-box verification is a compromise between the aloofness of black-box verification and the dependence on the implementation of white-box verification

D. Router Overview

The communication on network on chip is carried out by means of router, so for implementing better NOC , the router should be efficiently design. This router supports four parallel connections at the same time. It uses store and forward type of flow control and Fsm Controller deterministic routing which improves the performance of router. The switching mechanism used here is packet switching which is generally used on network on chip.

In packet switching the data the data transfers in the form of packets between cooperating routers and independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels. The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides.

A router is a device that forwards data packets across computer networks. Routers perform the data "traffic direction" functions on the Internet. A router is a microprocessor-controlled device that is connected to two or more data lines from different networks. When a data packet comes in on one of the lines.the router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table, it directs the packet to the next network on its journey.

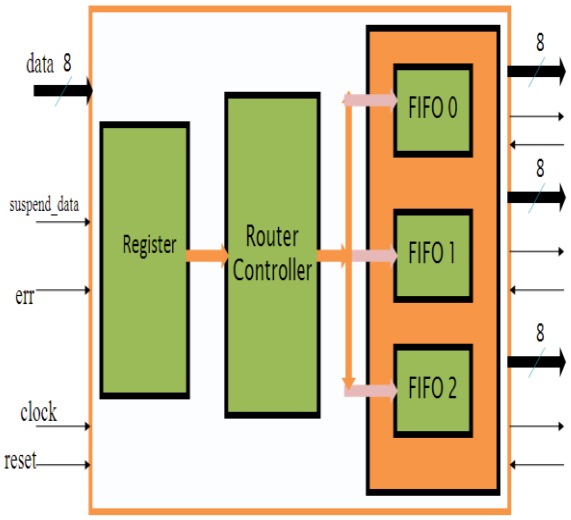
III. FOUR PORT NETWORK ROUTER

The router is a " Four Port Network Router" has a one input port from which the packet enters. It has three output ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be between 1 bytes to 63 bytes. Packet header contains three fields DAand length. Destination address(DA) of the packet is of 8 bits. The switch drives the packet to respective ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63. Length is measured in terms of bytes. Data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calculated over the header and data.

A data packet is typically passed from router to router through the networks of the Internet until it gets to its destination computer. Routers also perform other tasks such as translating the data transmission protocol of the packet to the appropriate protocol of the next network.

A. Packet Format

Packet contains 3 parts. They are Header, payload and parity.



Four Port Router Architecture

The router_reg module contains the status, data and parity registers for the Network router_1x3.

These registers are latched to new status or input data through the control signals provided by the fsm_router. There are 3 fifo for each output port, which stores the data coming from input port based on the control signals provided by fsm_router module.

The fsm_router block provides the control signals to the fifo, and router_reg module. The Router blocks Diagram shown below fig…

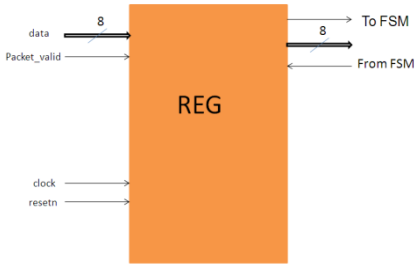
Router blocks are

(1) Register
(2) Router controller(FSM)
(3) FIFO Output Block

IV. REGISTER BLOCK

This module contains status, data and parity registers required by router. All the registers in this module are latched on rising edge of the clock.

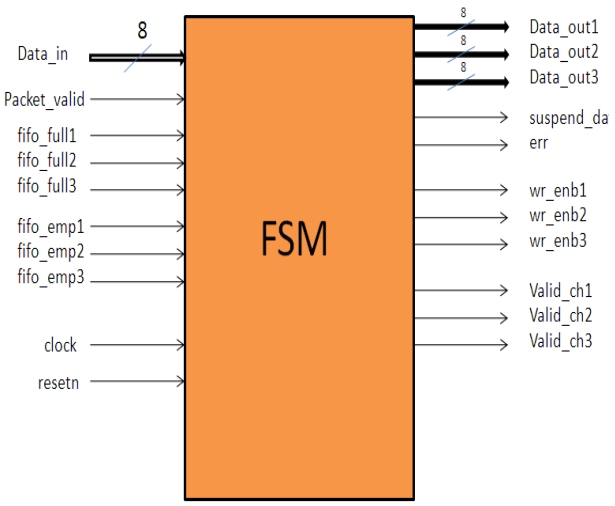
Data registers latches the data from data input based on state and status control signals, and this latched data is sent to the fifo for storage. Apart from it, data is also latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity.



Four Port Router Register

A. Router Controller (Fsm)

This module generates all the control signals when new packet is sent to router. These control signals are used by other modules to send data at output, writing data into the fifo.



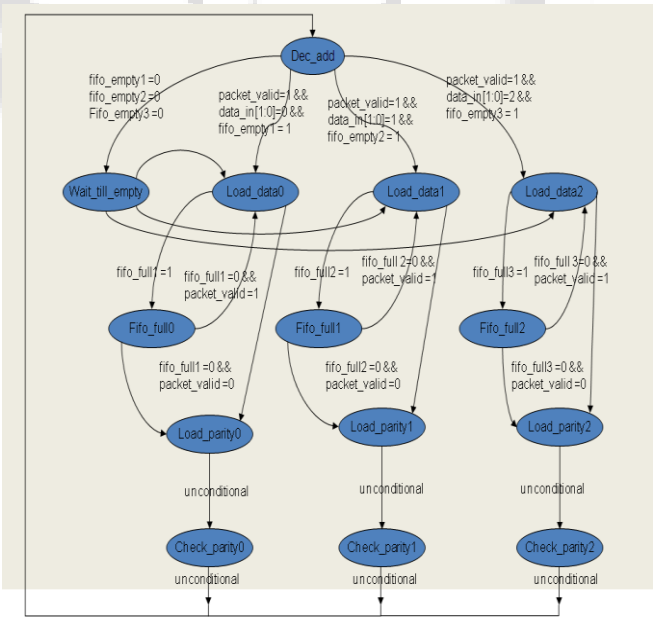
Four Router Controller Block

The 'fsm_router' module is the controller circuit for the router.

This is the default state. It waits for the packet_valid assertion, After packet_valid signal goes high, if the address is valid and fifo for that address is empty (fifo_empty signal will be high), data can be loaded, so, it goes to the next state LOAD_FIRST_DATA.

If fifo is not empty it goes to WAIT_TILL_EMPTY so that, new data couldn't be accepted till fifo is ready.

The output signal detect_add is made high, so that ff_sync module can detect the address of fifo to be used. detect_add signal is also used by router_reg module to latch the first byte in internal register.



Four port Router Controller State machine

B. Router Output Block

There are 3 fifos used in the router design. Each fifo is of 8 bit width and 16 bit depth.

The fifo works on system clock. It has synchronous input signal reset.

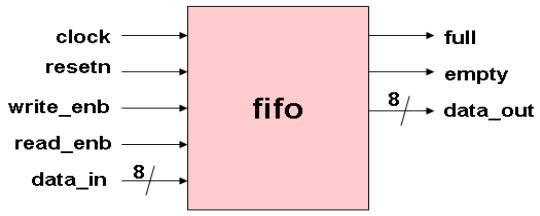
If resetn is low then full =0, empty = 1 and data_out = 0

The FIFO has doing 3 deferent operations

Write Operation

Read operation

Read and Write Operation
The functionality of FIFO explain Below



Four port Router FIFO

C. Write operation

The FIFO write operation is done by when the data from input data_in is sampled at rising edge of the clock when input write_enb is high and fifo is not full.in this condition onaly FIFO Write operation is done.

D. Read Operation

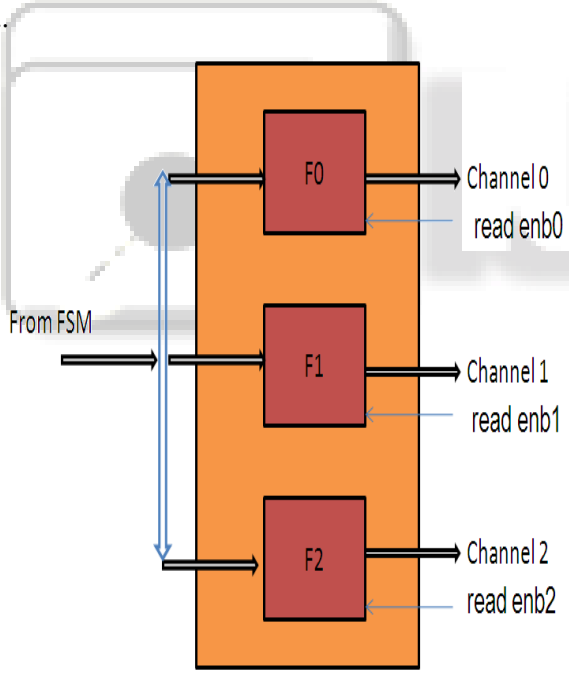
The FIFO Read Operation is The data is read from output data_out at rising edge of the clock, when read_enb is high and fifo is not empty.

Read and Write operation can be done simultaneously.

Full – it indicates that all the locations inside fifo has been written.

Empty – it indicates that all the locations of fifo are empty.

The Output Block of Network Router conisistes of three FIFO .each FIFO is a 8-Bit data Width and 16 bit data depth .the strcture of OUTPUT Block is shown in below fig..



Four Port Router Output Block

This module provides synchronization between fsm and fifo modules. It provides faithful communication between single input port and three output ports.

It will detect the address of channel and will latch it till packet_valid is asserted, address and write_enb_sel will be used for latching the incoming data into the fifo of that particular channel.A fifo_full output signal is generated, when the present fifo is full, and fifo_empty output signal is generated by the present fifo when it is empty.The output vld_out signal is generated when empty of present fifo goes low, that means present fifo is ready to read(vld_out_0 = ~empty_0,vld_out_1 = ~empty, vld_out_2 = ~empty_2).

The write_enb_reg signal which comes from the fsm is used to generate write_enb signal for the present fifo which is selected by present address

V. Conclusion

In this Four Port Router project I Design and verified the functionality of Router with the latest Verification methodology i.e.,System Verilog and observed the code coverage and functional coverage of Router by using coverpoints ,cross and different test cases like constrained, weighted and directed testcases.By using these testcases I improved the functional coverage of Router. In this I used one master and eight slaves to monitor the Router.Thus the functional coverage of Router was improved

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