A Verilog Based Simulation Methodology for Estimating Statistical Test for the Time Constancy of Scaling Exponents Power and Area

Lokeshwari Sharma[1]
[1]Research Scholar
[1]Department of Electronics and Communication
[1]Institute of Technology and Management, Bhilwara

Abstract— The low Power estimation is an important aspect in digital VLSI circuit design. The estimation includes a power dissipation of a circuit and hence this to be reduces. The power estimations are specific to a particular component of power. The process of optimization of circuits for low power, user should know the effects of design techniques on each component. There are different power dissipation methods for reduction in power component. In this paper, estimating the power like short circuit and the total power, power reduction technique and the application of different proposed technique has been presented here. Hence, it is necessary to provide the information about the effect on each of these components.

Keywords: Power estimation, Verilog Based Simulation Methodology, Power Theater.

I. INTRODUCTION

Power consumption was a part of the design process but not very visible. The reduced area of digital circuits is not a big point of matter today because with new IC production techniques, many millions of transistors can be fabricated in a single IC. But, reducing the sizes of circuits have paved the way for reduced power consumption in order to have an extended battery life. Generally, power is consumed when capacitors in the circuits are either charged or discharged due to the switching activities of CMOS. Estimating the short circuit dissipation has been coupled with the dynamic dissipation and report the switching energy. So at higher order of a system this power dissipation is well-kept by reducing the switching activities which is done by shutting down portions of the system when they are not in use. The short circuit models are proposed and studied .The correct model taken into account of capacitance load effect, the input rise and fall times. The overall current flow can be determined by the rise and fall time. Large VLSI circuits comprise of number of components like a processor, controllers and a functional unit. The power reduction has to stop in any of the components of the processor which is not in use, so that less power will be dissipated when the processor is operating. The circuit level power estimation can accurately and efficiently estimate various power components and the total power and provide information to a designer. With the modification and significant advances made in logic simulation, timing analysis and delay areas through the use of the bounded delay model and also be extended to include leakage power.

II. POWER DISSIPATION IN CMOS CIRCUITS

Three prime sources of power dissipation in CMOS circuits:

- Dynamic power
- Short circuit power
- Leakage power

The average power dissipation of a digital CMOS circuits can be calculated by

$$P_{avg} = P_{dynamic} + P_{short\text{-}circuit} + P_{leakage} + P_{static}$$

Where P_{avg} is the average power dissipation, $P_{dynamic}$ is the dynamic power dissipation due to switching of transistors, $P_{short\text{-}circuit}$ is the short-circuit current power dissipation when there is a direct current path from power supply down to ground, $P_{leakage}$ is the power dissipation due to leakage currents, P_{static} and is the static power dissipation[12].

A. Dynamic power

Dynamic Power is the dominant source of power dissipation in hardware design, and is highly dependent on the application and architecture. A lot of opportunities to reduce dynamic power exist at high-level. Power reduction techniques discussed in this thesis concentrate on reducing the dynamic power consumption of the hardware design. Switching activity and capacitance are two most important factors to keep in mind at high level because small changes in hardware architecture may impact the capacitance and activity profile of the design.

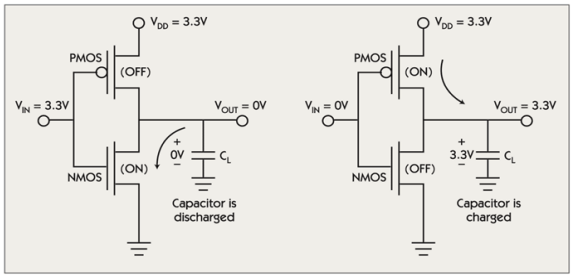

Fig. 1: Dynamic Power in CMOS Invertor

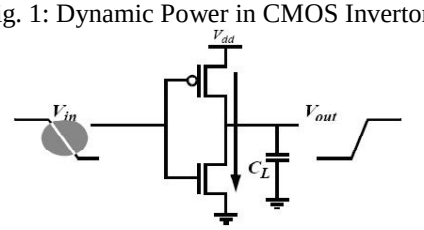

Fig. 2: Static Power in CMOS Invertor

B. Leakage power

It is the static component of the power dissipation and occurs due to spurious currents in the non-conducting state of the transistors. Static power has two important factors, namely Sub-threshold leakage and gate to source leakage. As process technology node size is decreasing sub-threshold leakage is increasing. This factor exponentially in- creases with newer technology node. Some of the prominent techniques to reduce leakage power include power-gating and stacking of transistors. These techniques are applied after the net list is finalized for the design. Gate to source

leakage can be reduced by improving the gate insulation of a node of transistor.

C. Short-circuit Power:

It occurs due to the stacked P and N devices in a CMOS logic gate that are in the ON state simultaneously, and can be minimized by reducing the signal transition times. It is hard to reduce this component of power through synthesis-time optimizations. After the netlist is finalized, a lot of care is given to place the design so that there is not much voltage drop for some transistors. Voltage drop on nodes may not only cause timing issues but also short circuit power issues. If short circuit power persists for longer time it may cause extremely high power consumption.

Various tools exist in industry that can perform power estimation accurately at the RTL or lower- level such as Power Theater [11].Power Theater [11] is an RTL/gate-level power estimation tool, which provides good accuracy for RTL power estimation with respect to the corresponding gate-level and silicon implementation. These tools require design information for models in Verilog/VHDL, simulation dump from the RTL or lower-level simulation (such as Value Change Dump (VCD) or FSDB) for activity analysis, and technology library etc. Such information helps in doing power estimation accurately and efficiently at the RTL and lower level.

III. HIGH LEVEL POWER ESTIMATION

Accurate power estimation at high level is very important for any successful design methodology. In this section, we include spread sheet based approach, Power Estimation Approaches utilizing Power Models, commercial tools available for RTL and gate-level power estimation etc.

A. Spreadsheet Based Approaches:

Spreadsheets are very useful in the early stage of design process, when initial planning is going on and a lot of important decisions are being taken [13]. One of the biggest advantages of spreadsheet based analysis is that the user does not really need to learn any complex/sophisticated tool for taking design decisions. One of the basic application of spreadsheet is area estimation. He/She can easily get an estimate on area by using data sheets from intellectual property (IP) provider, library cell estimates, etc. Spreadsheet provides a capability to capture such information, which can be utilized for quick area estimation. Similarly, some decisions to control power can also be taken using spreadsheet based approach. Power calculating approaches using spreadsheets are very helpful for voltage regulators , heat sink, printed circuit board (PCB), power supplies, and cooling systems.

B. Power Estimation Approaches utilizing Power Models

One of the first works in the area of model based power estimation was proposed by Tiwari et al. [14] for the architecture level power estimation of microprocessors. They provide a method to estimate power/energy number of a given program on a given processor. It states "By measuring the current drawn by the processor as it repeatedly executes certain instruction sequences, it is possible to gain most of the information that is needed to estimate the power cost of a program for that processor" [14].

Power consumption of a microprocessor can be represented as P = VCC x I, where VCC is operating voltage and I is the current drawn by the microprocessor. In their approach, they measured the current drawn by the processor and then utilize it for power measurement purpose. They assumed that during the calculation, the operating voltage for the processor will not change. For average power estimation purpose they had first estimated energy over different cycles and then averaged it. To conclude with, they have proposed a way in which one can gauge the impact on average current from the execution of an instruction. This also proposed a method to measure inter- instruction effects on prevailing values. To compute the average power consumption of a processor while executing a software program, these values are used.

Most of the approaches for power models are proposed for CPU or micro architecture of processors. In an ASIC design flow where mainly design stage starts at RTL and mostly design is represented as a Finite State Machine with Data path (FSMD), similar approach may not be useful.

IV. POWER REDUCTION AT THE RTL AND HIGH LEVEL

Clock-gating is implemented at the RTL by tools such as Power Theater [15], Power compiler [16], etc. Power Theater suggests opportunities to clock-gate registers for which there is no multiplexer in the feedback path. They find the conditions under which clock is required when and only when there is a change in data input to a register. Power compiler recommends particular RTL coding styles to enable clock-gating during synthesis.

Clock gating and operand isolation are two techniques to reduce the power consumption in state- of-the art hardware designs. Both approaches basically follow a two-step procedure: first, a hardware circuit is statically analyzed to determine irrelevant computations. Secondary, all parts that are responsible for these computations are replaced by others that consume less power in the average case, either by gating clocks or by isolating operands. Jens et al. [17] defines the theoretical basis for adoption of these approaches in their entirety. They show how irrelevant computation can be eliminated using their approach. They present passiveness conditions for every signal x, that shows that the value currently carried by x does not contribute to the final result of the system. After showing how their theory can be generally used in the context of clock gating and operand isolation a classification of many state-of-the-art approaches is performed and shown that most of the approaches in the literature are conservative approximations of their general setting.

Recently power reduction techniques have also been used for security purpose. With increased outsourcing, confirming the genuineness of third party manufactured ICs has emerged as a major challenge. Researchers have effectively used various side-channel analysis techniques to finger- print ICs viz. power, timing, EM-radiation. In [18], [19] authors have used circuit partitioning techniques to selectively exaggerate power consumption in targeted portions while reducing the overall power of the chip.

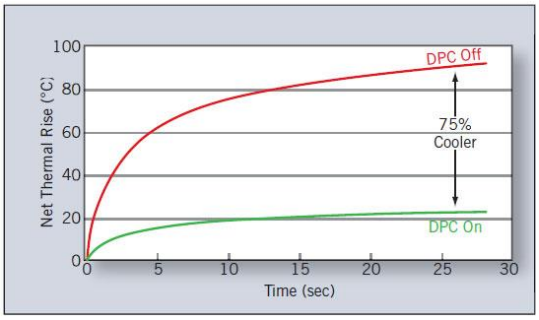

Fig. 3: Dynamic Power Control Lower Power Consumption and Eliminates Power Loss

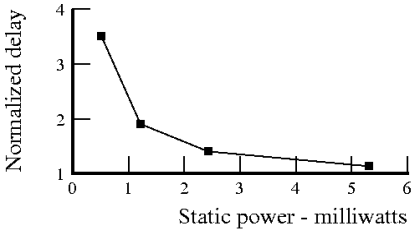

Fig. 4: Static Power Versus Normalized delay

V. Application of the Proposed Techniques

In this paper, propose techniques that can be utilized with HLS or high-level design flows. Here we briefly discuss the application of the proposed techniques.

A. Early Power Estimation

This approach is applicable in scenarios where designers want to measure power consumption of the target hardwares using models that can be utilized at higher abstraction levels than the RTL. It is given that the RTL or gate-level power estimation is extremely time consuming, such techniques can save time if proven to be accurate enough for crucial design decisions. A technique to characterize power model that is parameterized by the switching activity of each state of Finite State Machine with Datapath (FSMD) model of the design. Such a power model can then be simulated with high-level models. One could use such vectors or assertions to bring a high level simulation to a target state to measure state specific power consumption.

Since power consumption is very much design and technology dependent, it might be difficult to create power models that characterize power consumption of a target hardware at high-level. To perform power calculation at the RTL, the largest bottlenecks are simulating, processing and extraction of the activity information.

B. Power Reduction from high-level:

We consider clock-gating as a primary candidate for power reduction. We investigate how this can be enabled from high-level. A designer is operating on a behavioral description of the design at high-level. Clock-gating is needed to be insert from the behavioral description before synthesis. Similarly, sequential clock-gating requires optimizations across the register boundaries. Such optimizations may cause a lot of verification problems. Also, how system-level simulation can guide HLS to select the appropriate clock-gating candidates among all the registers. This approach is also useful to find out if aggressive application of clock-gating will lead to wastage.

VI. Conclusion

The estimation techniques are implemented for logic gate level estimation tool. The tool can estimate the different power dissipation components and also estimate the power dissipation while maintaining efficiency .Also capable of separating and estimating the different power dissipation components. The above technique can be used for estimating the power dissipation. There have been other notable works focusing on particular power components.

For the power estimation Techniques discussed above show that power modeling of a hardware block can be very complex and application dependent. On enhancing the levels of abstraction, power estimation of a hardware block becomes crucial. Different techniques at different abstraction levels exist to obtain the power consumption starting from spread-sheet, power model to macro-model based power estimation. The most popular approaches in industry are mainly power model based approach or by performing power estimation at RTL/gate-level description of a hardware design. While, at the lower level of abstraction, commercial tools contribute good certainty with respect to silicon, but as we go to higher levels of abstraction accuracy of the power estimation methodologies reduces.

Dynamic power is one of the most important components of power consumption of a design, and thus its reduction is targeted during most power-aware high-level synthesis processes. Most of the approaches do not provide any support for power reduction from the behavioral specifications itself. In this paper, propose approaches to enable clock-gating itself for various granularities of clock-gating such as fine grain at variable level and coarse grain at function or scope level. We also show how to extend this approach for sequential clock-gating. Finally, we present how to utilize power models to guide power reduction process at high-level. The advantage of such an approach is facilitation of power reduction features at the high-level. Also, the approaches for power estimation, which will be discussed later in detail, combined with power reduction approach can make the design flow completely at high-level. This will help in providing power aware design methodology at high-level with faster turnaround time.

Reference

[1] L. Bisdounis, S. Nikolaidis, and O. Loufopavlou, “Propagation Delay and Short-Circuit Power Dissipation Modeling of the CMOS Inverter,” IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications, vol. 45, no. 3, pp. 259–270, Mar. 1998.

[2] S. Bobba and I. N. Hajj, “Maximum Leakage Power Estimation for CMOS Circuits,” in Proc.15th International Conf. on VLSI Design and 7th Asia and South Pacific Design Automation Conf., Jan. 1999, pp. 116–124.

[3] A. Bogiolo, L. Benini, and B. Ricc`o, “Power Estimation of Cell-Based CMOS Circuits,” in Proc. Design Automation Conf., 1996, pp. 433–438.

[4] A. Boliolo, L. Benini, G. de Micheli, and B. Ricco, “Gate-Level Power and Current Simulation of CMOS Integrated Circuits,” IEEE Transactions on Very

Large Scale Integration (VLSI) Systems, vol. 5, pp. 473–488, Dec. 1997.
[5] S. Bose and V. D. Agrawal, "Delay Test Quality Evaluation Using Bounded Gate Delays,"Proc. 25th IEEE VLSI Test Symp, May 2007, pp. 23–28.
[6] S. Bose, H. Grimes, and V. D. Agrawal, "Delay Fault Simulation.
[7] H. Grimes, "Reconvergent Fan-out Analysis of Bounded Gate Delay Faults," Master's thesis, Auburn University, Aug. 2008. Dept. of ECE.
[8] H. Grimes and V. D. Agrawal, "Analysing Reconvergent Fan outs in Gate Delay Fault Simulation," in Proc. 17th IEEE North Atlantic Test Workshop, May 2008, pp. 98–103.
[9] R. X. Guand M. I. Elmasry, "Power Dissipation Analysis and Optimization of Deep Submicron Circuits," IEEE Journal of Solid-State Circuits, pp. 707–713, May 1996.
[10] S. Hassoun, "Critical Path Analysis Using a Dynamically Bounded Delay Model," in Proc. 37th Design Automation Conf., 2000, pp. 260–265.
[11] Sequence Design Inc., "RTL power management," http://sequencedesign.com/solutions/powertheater.php
[12] L. Cai and D. Gajski, "Transaction level modeling: an overview," IEEE/ACM/IFIP Interna- tional Conference on Hardware/Software Codesign and System Synthesis, 2003.
[13] W. Wolf, "Household hints for embedded systems designers," IEEE Computer Society Press, 2002.
[14] V. Tiwari, S. Malik, and A. Wolfe, "Power analysis of embedded software: a first step to- wards software power minimization," in ICCAD '94: Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design. Los Alamitos, CA, USA: IEEE Com- puter Society Press, 1994, pp. 384–390.
[15] Sequence Design Inc., "RTL power estimation," in Power heater User guide, release 2007.2, 2007.
[16] "Power Compiler, Synpsys Inc." http://www.synopsys.com.
[17] J. Brandt, K. Schneider, S. Ahuja, and S. K. Shukla, "The model checking view to clock gating and operand isolation," June 2010.
[18] M. Banga, M. Chandrasekar, L. Fang, and M. S. Hsiao, "Guided test generation for isolation and detection of embedded trojans in ics," pp. 363–366, 2008.
[19] M. Banga and M. S. Hsiao, "A region based approach for the identification of hardware trojans," pp. 40–47, 2008.

