Design and Analysis of Sequential Circuit for Leakage Power Reduction Using Stacking Effect

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Abstract— The rapid growth in semiconductor device industry has led to the development of high Performance potable systems with improve reliability. In such applications, it is extremely important to minimize current consumption due to the limited availability of battery Power. Consequently, power dissipation is becoming recognized as a top priority issue for VLSI circuit design. Leakage power makes up to 50% of the total power consumption in today's high performance microprocessors. Therefore leakage power reduction becomes the key to a low power design. Leakage power dissipation is the power dissipated by the circuit when it is in Sleep mode or standby mode. A significant portion of the total power consumption in high performance digital circuits in deep submicron regime is mainly due to leakage power. Leakage is the only Source. of power consumption in an idle circuit. Therefore it is important to reduce leakage power in portable system.

Keywords: Dynamic Power, Delay, Low Power Design

I. INTRODUCTION

ONE of the major dynamic power consumers in computing and consumer electronics products is the system's clock signal, typically responsible for 30%–70% of the total dynamic power consumption . Several techniques to reduce the dynamic power are developed, of which clock gating is predominant. Ordinarily, when a logic unit is clocked, its underlying sequential elements receive the clock signal, regardless of whether or not they will toggle in the next cycle. With clock gating, the clock signals are ANDed with explicitly predefined enabling signals.

Clock gating is employed at all levels: system architecture, block design, logic design, and gates. With the rapid increase in design complexity, computer aided design tools supporting system-level hardware description have become commonly used. Although substantially increasing design productivity, such tools require the employment of a long chain of automatic synthesis algorithms, from register transfer level (RTL) down to gate level and net list. Unfortunately, such automation leads to a large number of unnecessary clock toggling, thus increasing the number of wasted clock pulses at flip-flops (FFs) as a result, development of automatic and effective methods to reduce this inefficiency is desirable. In the sequel, we will use the terms toggling, switching, and activity interchangeably.

The clock signal driving a FF is disabled (gated) when the FFs state is not subject to change in the next clock cycle . Data driven gating is causing area and power overheads that must be considered. In an attempt to reduce the overhead, it is proposed to group several FFs to be driven by the same clock signal, generated by oring the enabling signals of the individual FFs. This may however, lower the disabling effectiveness. It is therefore beneficial to group FFs whose switching activities are highly correlated and derive a joint enabling signal. In a recent paper, a model for data-driven gating is developed based on the toggling activity of the constituent FFs . The optimal fan out of a clock gate yielding maximal power savings is derived based on the average toggling statistics of the individual FFs, process technology, and cell library in use. In general, the state transitions of FFs in digital systems depend on the data they process. Assessing the effectiveness of data-driven clock gating requires, therefore, extensive simulations and statistical analysis of the FFs' activity.

Another grouping of FFs for clock switching power reduction, called MULTIBIT FF (MBFF), has recently been proposed in. MBFF attempts to physically merge FFs into a single cell such that the inverters driving the clock pulse into its master and slave latches are shared among all FFs in a group. MBFF grouping is mainly driven by the physical position proximity of individual FFs, while grouping for data driven clock gating should combine toggling similarity with physical position considerations.

A conventional flip-flop connected to a logic block through its input terminal. The clock signal keeps changing its state in certain time points according to its frequency even if the logic output doesn't change "hold mode". A promising technique to reduce the power consumption of the clock signal is called clock gating, it depends on deactivating the clock signal on portions of the circuit that are inactive for certain periods of time. Different clock gating techniques have been used to minimize the clock power consumption as it is the main source of chip power dissipation. Deactivating the clock signal leads to reduced power dissipations of both its internal nodes and clock lines, but the overhead involved limits its use in low data switching situations. In this paper we reduce the clock gated flip-flop overhead and make it applicable to data signals with higher switching activity. In synchronous digital circuits the clock net is responsible for significant part of power dissipation up to 40%.. Previous work on clock gated flip-flops is reviewed in section II. Section III describes the proposed work. Section IV provides the simulation results in 90 nm CMOS technology to verify the performance of proposed circuit. Finally, conclusion is provided in section V.

II. PREVIOUS SYSTEM DIAGRAM

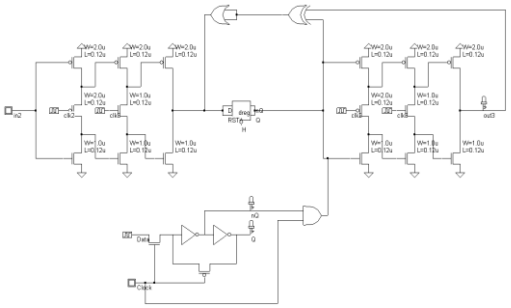

Fig. 1.1

Clock gating is a predominant technique used for power saving. It is observed that the commonly used synthesis based gating still leaves a large amount of redundant clock pulses. Data-driven gating aims to disable these. To reduce the hardware overhead involved, flip-flops (FFs) are grouped so that they share a common clock enabling signal. A FF finds out that its clock can be disabled in the next cycle by XORing its output with the present data input that will appear at its output in the next cycle. The outputs of *k* XOR gates are ORed to generate a joint gating signal for *k* FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is commonly used by commercial tools. Such data driven gating has been used for a digital filter in an ultralow-power design.

III. PROPOSED SYSTEM DIAGRAM

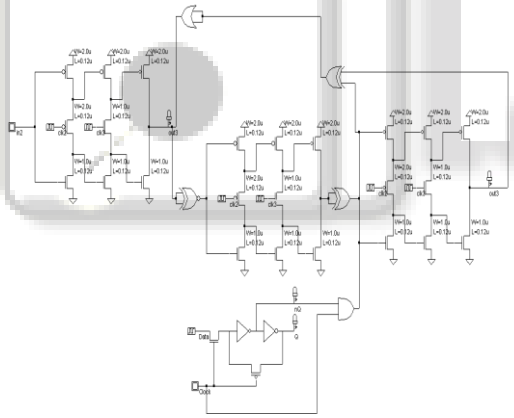

Fig. 1.2

In this paper instead of grouped flip flop we are using D flip flop. By using this memory element we can implement a low power and high speed design. In this proposed system the leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF to produce "Stacking Effect". When two or more transistors that are switched OFF are stacked on top of each other then they dissipate less leakage power than a single transistor that is turned OFF. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage.

IV. SIMULATION RESULTS

A. Schematic design includes leakage power using sequential logic

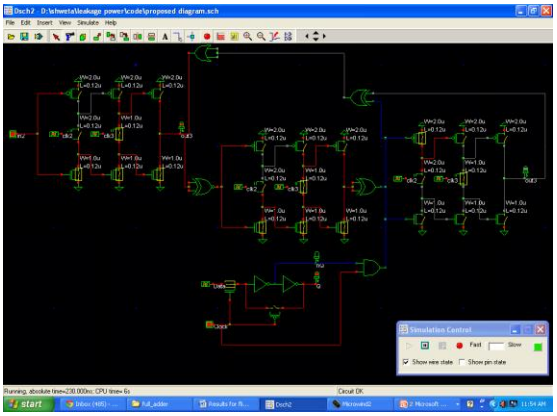

Fig. 1.3: Layout design for the proposed method

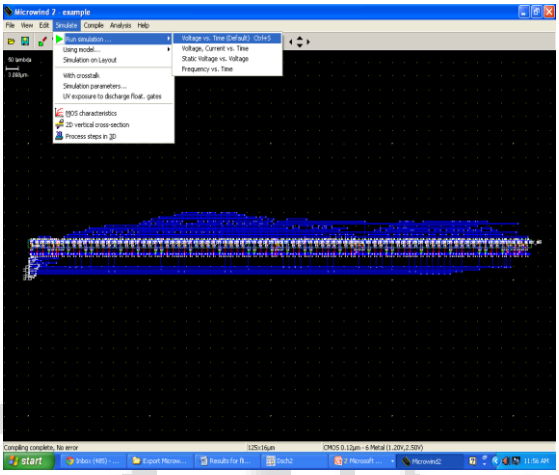

Fig. 1.4: Simulation waveforms for different parameters are shown below:

In figure below shows the simulation waveforms for voltage with respect to the time. By simulation result can compare the power consumption for the design with conventional method.

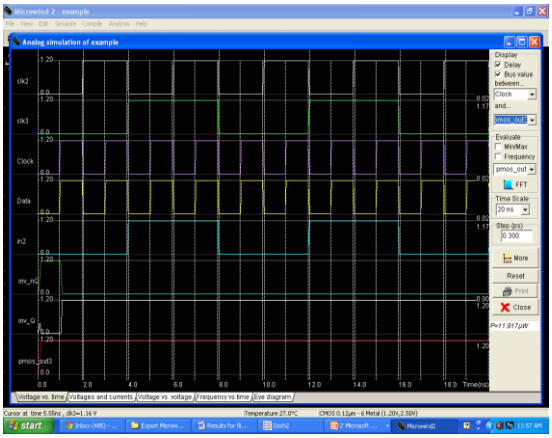

Fig. 1.5: Voltage vs Time

Fig. 1.6 shows the simulation waveforms for Voltage vs Current

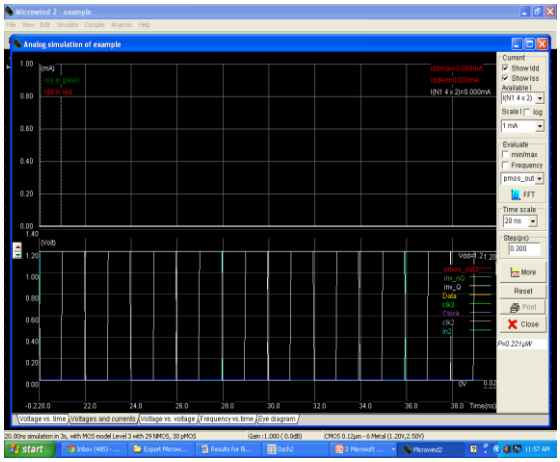

Fig. 1.6 Voltage vs Current

Fig. 1.7 shows the simulation waveforms for Voltages vs voltage

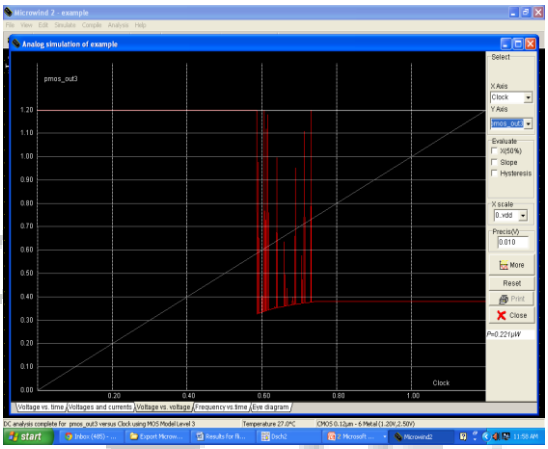

Fig. 1.7 Voltages vs voltage

Fig. 1.8 : shows the simulation waveforms for frequency and time graph

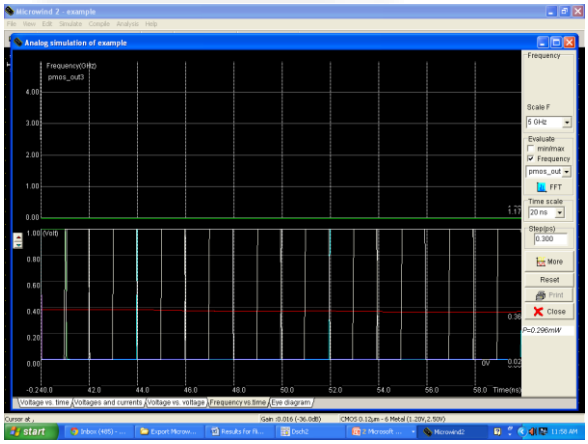

Fig. 1.8: frequency and time graph.

Characteristics parameters	Existing system(power consumption)	Proposed system(power consumption)
Voltage Vs Time	0.729mW	16.152microW
Voltages and Current	0.750mW	0.447microW
Voltage Vs Voltage	0.750mW	0.447microW
Frequency Vs Time	0.741mW	0.295mW

Table 1: comparison table

V. CONCLUSION

It has been shown that reducing the supply voltage is the most direct means of reducing dissipated power and operating CMOS devices is considered to be the most energy-efficient solution for low-performance applications.

VI. FUTURE DEVELOPMENTS

With the increasing demand for battery-operated portable applications such as cell phones, PDAs and laptop computers, as well as low-intensity applications such as distributed sensor networks, the need for power sensitive design has grown significantly. So , for future work we can further change the design to get minimal power.

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