LDR Based Power Switching System

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Abstract— this paper proposes a power switching system based on op-amp and flip flop. The main objective is to design a shockproof power switching system for controlling power supply to electrical appliances via Light Dependent Resistor (LDR). This system consists of an op-amp, JK flip-flop, relay, Bi-polar Junction Transistor (BJT), Light Dependent Resistor (LDR). The system is designed to detect the change in the intensity of the light in the surroundings to perform the switching action. Several tests have been conducted to test and validate the proposed prototype in different environment. As conclusion, a shockproof switching system can be achieved reducing the chances of hazardous electrical shocks because of no physical contact with the switch.

Key words: Shockproof, power switching system, Light Dependent Resistor (LDR), Bi-polar Junction Transistor (BJT), op-amp, JK flip-flop, relay.

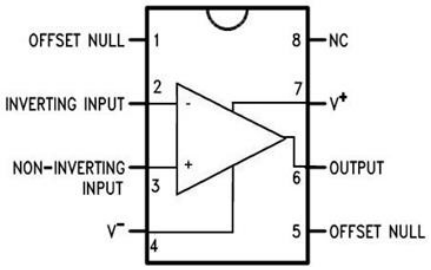
I. INTRODUCTION

Basically, power switching system is one of the important parts of an electrical network where the main function is to provide power to electrical appliances. Previously the switches when turned on or off resulted in sparks, though with improvement in technology better switches have come up in the market but they still face this problem of sparking which may be dangerous. Therefore in order to make a better switching system, the basic need is to make it in a way that it does not requires any physical contact so as to make it shockproof and thus preventing from any casualties. Power switching system is a very useful switching system which can be used almost everywhere from homes to industries. It uses a LM741 and a CD4027 both in plastic dual in-line package and a few external components. In this the Light Dependent Resistor (LDR) is used to detect the intensity of light at any given moment in its surroundings. The op-amp LM741 produces an output voltage that is hundreds of thousands of times larger than the difference between its input terminal voltage. Here the master slave JK flip flop IC(CD4027) is employed in toggle mode. This IC can be used to change the state by the signal applied to one or more control inputs and will have one or two outputs. CD4027 has four inputs J, K, Set and Reset and it contains two outputs Q and bar (Q not). The value of output not merely depends on the present input state but also on what the present state is (also depend on the earlier state). Memory circuit in computers mainly use flip flops.

The relationship between the incident light on the device and the resulting output signal is called the sensitivity of a photo detector. While in a photo resistor, sensitivity is defined as the relationship between the incident light and the resulting resistance of the cell.

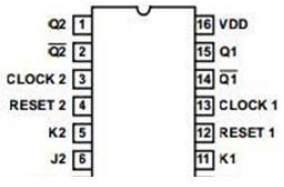
A photo resistor or light-dependent resistor (LDR) or photocell is a light-controlled variable resistor. The resistance of the photo resistor decreases with increasing incident light intensity; in other words, it exhibits photoconductivity. Thus a photo resistor has very high resistance in the absence of light. . A photo resistor can be applied in light-sensitive detector circuits and switching circuits.

LM741 Pinout Diagram



- Pin 1: Offset Null: This is the pin where we give a voltage to the IC if we want to eliminate the offset voltage
- Pin 2: Inverting Input: This is the pin where the positive part of the input signal that we want to amplify goes if we want our amplified signal to be inverted. If we don't want to invert the signal, we place the positive part of the signal into the Non-inverting terminal and the negative or ground part of our signal here.
- Pin 3: Non-inverting Input: This is the pin where the positive part of the input signal that we want amplified goes if we want our signal non-inverted.
- Pin 4: V: The LM741 op-amp is a dual power supply op- amp, i.e. it must be supplied with a positive DC voltage and negative a DC voltage. The negative DC voltage to the op-amp is supplied through Pin 4.
- Pin 5: Offset Null: This is the pin where we add voltage to if we want to eliminate the offset voltage.
- Pin 6: Output: This is the pin where the output, the amplified signal, comes from. Whatever output the amplifier will drive gets connected to this terminal.
- Pin 7: V+: This is the terminal where positive DC voltage is given.
- Pin 8: NC: This pin stands for "Not Connected". This pin is not used for anything and should be left open

CD4027 Pinout Diagram



- Pin 1: Q2: This is the terminal where the output, the signal of flip-flop 2 comes out of. There are two ways in which a load can be connected to the output terminal. One way is to connect the load between the output pin (pin 1) and the supply pin (pin 16) or between output pin (pin1) and ground pin (pin 8). The load connected between output pin and supply pin is called the *normally on load* and

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that connected between output pin and ground pin is called the *normally off load.*

- Pin 2: Q2 bar: This is the terminal where the complement of the output, the signal of flip-flop 2 comes out of.
- Pin 3: CLOCK 2: This is the terminal used to give a clock pulse to flip-flop 2.
- Pin 4: RESET 2: If the flip-flop 2 is to be reset or disabled, a negative pulse is applied to this pin, and therefore it is named as reset terminal. This pin should be connected to + V_{CC} to avoid any possibility of false triggering if it is not to be used for reset purpose.
- Pin 5: K2: This terminal is used as synchronous input to flip-flop 2.
- Pin 6: J2: This terminal is used as synchronous input to flip-flop 2.
- Pin 7: SET 2: This terminal is set pin for flip-flop 2.
- Pin 8: VSS: All the voltages are measured with respect to the ground terminal.
- Pin 9: Q1: This is the terminal where the output, the signal of flip-flop 1 comes out of. There are two ways in which a load can be connected to the output terminal. One way is to connect the load between the output pin (pin 1) and the supply pin (pin 16) or between the output pin (pin1) and the ground pin (pin 8). The load connected between output pin and supply pin is called the *normally on load* and that connected between output pin and ground pin is called the *normally off load.*
- Pin 10: Q1 bar: This is the terminal where the complement of the output, the signal of flip-flop 1 comes out of.
- Pin 11: CLOCK 1: This is the terminal used to give a clock pulse to flip-flop 1.
- Pin 12: RESET 1: If the flip-flop 1 is to be reset or disabled, a negative pulse is applied to this pin, and therefore it is named as reset terminal. This pin should be connected to + V_{CC} to avoid any possibility of false triggering if it is not to be used for reset purpose.
- Pin 13: K1: This terminal is used as synchronous input to flip-flop 2.
- Pin 14: J1: This terminal is used as synchronous input to flip-flop 1.
- Pin 15: SET 1: This terminal is set pin for flip-flop 1.
- Pin 16: VDD: A supply voltage of -0.5 V to + 18 V is applied to this terminal with respect to ground (pin 8)

II. Literature Review

An operational amplifier (op-amp) is a high-gain electronic voltage amplifier with a differential input with a single-ended output and is a fundamental active element of analog circuit design. The op-amp LM741 produces an output voltage that is hundreds of thousands of times larger than the voltage difference between its input terminals [1].

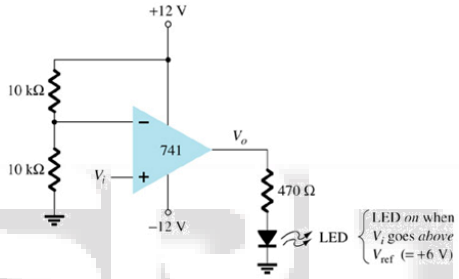
Operational amplifiers were initially used in analog computers for doing mathematical calculations. External components can be used to set the characteristics of an op-amp, with little dependence on temperature changes or manufacturing variations in the op-amp itself, makes op-amps popular building blocks for circuit design.

Op-amps are one of the most widely used electronic devices. They are being used in a vast array of industrial, consumer and scientific devices. Most of the standard IC op-amps cost only a few bucks ; however some integrated and hybrid operational amplifiers with special performance specifications cost over $100 US in small quantities.

The op-amp is a type of differential amplifier. The full differential amplifier, the instrumentation, the isolation amplifier , and the negative feedback amplifier (usually built from one or more op-amps and a resistive feedback network) are few other types of differential amplifier[2 – 4].

An op-amp can be used as a comparator, it can be used in 2 ways:

A. Non-inverting Comparator

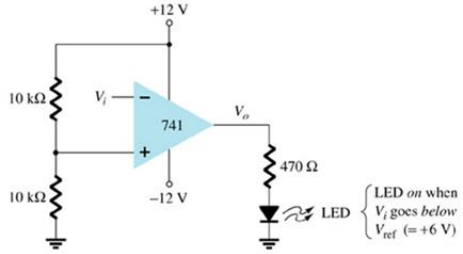


When the input Vi is greater than the reference, the output of the op-amp comparator goes high to $+V_{SAT}$. When Vi is less than the reference, the output is at $-V_{SAT}$.

The reference voltage in this case is via a voltage divider that establishes +6V at the non-inverting input. $+V_{SAT}$ = +V of the op-amp, or in this case +12V. $-V_{SAT}$ = -V or –12V in this case.

When Vi is greater than +6V, the output swings to +12V and the LED is on. When Vi is less than +6V, the output is at –12V and the LED is off.

B. Inverting Comparator Circuit



When the input Vi is greater than the reference, the output of the op-amp comparator goes low to $-V_{SAT}$. When Vi is less than the reference, the output is at $+V_{SAT}$.

When Vi is greater than +6V the output swings to -12V and the LED is off. When Vi is less than +6V the output is at +12V and the LED is on

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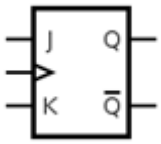
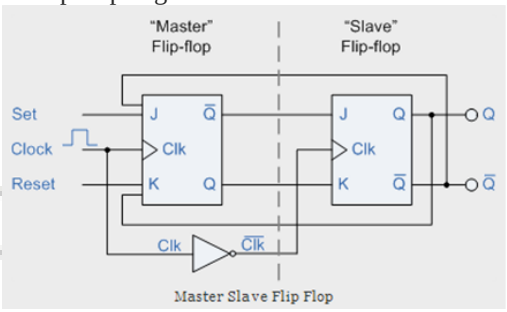


The JK flip-flop augments the behavior of the SR flip-flop (J=Set, K=Reset) by interpreting the S = R = 1 condition as a "flip" or "toggle" command. Specifically, the combination J = 1, K = 0 is a used to set the flip-flop; the combination J = 0, K = 1 is a used to reset the flip-flop; and the combination J = K = 1 is a used to toggle the flip-flop. We simply need to set K equal to the complement of J to synthesize a D flip-flop. Similarly, set K equal to J, to synthesize a T flip-flop. The JK flip-flop is thus a universal flip-flop, as it can be configured to work as a D flip-flop, SR flip-flop or a T flip-flop.

Master-slave flip flop is designed using two separate flip flops. Out of the two, one flip flop acts a as the master and the other one as a slave. The figure of a master-slave J-K flip flop is given below:



From the above figure you can see that both the J-K flip flops are presented in a series connection. The output of the master J-K flip flop is fed to the input of the slave J-K flip flop. The output of the slave J-K flip flop is given as a feedback to the input of the master J-K flip flop. The clock pulse is given to the master J-K flip flop and it is sent through a NOT Gate and thus inverted before passing it to the slave J-K flip flop.

When Clock=1, the master J-K flip flop gets disabled. The Clock input of the master input will be the opposite to that of the slave input. Thus the master flip flop output will be recognized by the slave flip flop only when the value of Clock becomes 0. Therefore whenever the clock pulse goes from 1 to 0, the locked outputs of the master flip flop are given through to the inputs of the slave flip-flop making this flip flop pulse or edge-triggered.

Thus, the circuit accepts the value in the input when the clock is 1, and passes the data to the output on the falling-edge of the clock signal. This makes the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal[5-6].

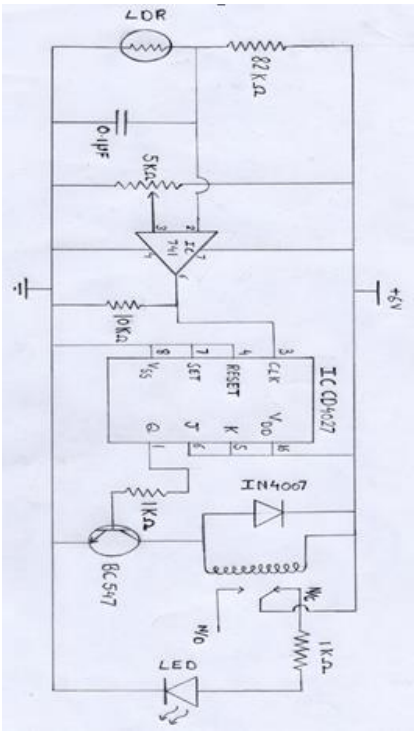
III. PROPOSED METHODOLOGY

The circuit is connected as shown in the figure below:

The working of the circuit depends mainly on LDR, op-amp and the master -slave J-K flip-flop.

The LDR in the absence of light shows a very high resistance of about 1 mega ohms while a very low resistance of about 2-5 k ohms in the presence of light(in terms of Ω). It responds to a large part of the light spectrum

The op-amp in this circuit works as inverting comparator with the voltage across the op-amp as the reference voltage (let it be **Vr**). To detect the present of light we have used LDR.



The LDR initially shows a very low resistance when light falls on it and thus the voltage across the LDR is very low. The current flowing through the capacitor charges the capacitor to a voltage proportional to that of across the LDR. Since the voltage at terminal "2" of the op-amp is less than that on terminal "3", a negative amplified voltage is given as the output of the op-amp. The negative voltage behaves as logic 0 for the clock pulse of the flip flop, thus there is no output (i.e logic 0) from the flip flop and no action of the circuit thereafter.

When hand is waved over the LDR , due to less intensity of light the resistance of LDR increases to a very large value. The current flowing through the capacitor charges the capacitor to a voltage proportional to that of across the LDR. Now since the voltage at terminal "2" of op-amp is more than that on terminal "3", a positive amplified voltage is given as the output of the op-amp. The positive voltage behaves as logic 1 for the clock pulse of the flip flop, and we get logic 1 as the output from Q, thus making the BJT forward biased. Thus current flows from relay to BJT and then to ground, this excites the relay and the common terminal moves from N/O to N/C. This makes the LED glow, analogous to the switching ON action of a light or any electrical appliance. The LED continues to glow until hand is again waved over the LDR.

When hand is again waved over the LDR , due to less intensity of light the resistance of LDR increases to a very large value. The current flowing through the capacitor charges the capacitor to a voltage proportional to that of across the LDR. Now since the voltage at terminal "2" of op-amp is more than that on terminal "3", a positive amplified voltage is given as the output of the op-amp. The positive voltage behaves as logic 1 for the clock pulse of the flip flop, and we get logic 0 as the output from Q, thus

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making the BJT reverse biased. Thus no current flows from relay, this de-excites the relay and the common terminal moves from N/C to N/O. Thus the LED stops glowing, analogous to the switching OFF action of a light or any electrical appliance

IV. CONCLUSION

The proposed system implements a new design of switching mechanism making it more safe and reliable. This circuit with slight modifications may have wide application almost anywhere there is a need of such a device. We can develop various applications using LDR like Automated Emergency Lights, in Car Parking systems etc. It has wide applications and can be used from households to big industries. It can have large industrial applications too. For further development of the technology we need to optimize the value of impedances in the circuit in order to prevent energy losses and come up with a more sophisticated design of the circuit.

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