Analysis and Study of Different Tunnel Diode Devices

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Abstract— This paper includes the principle of tunnelling and designing or construction of the different tunnel diode devices such as conventional or Esaki tunnel diode, nanowire tunnel diode, tunnel diode using heterostructures and resonant interband tunnel diodes.

Key words: Peak-to-valley current ratio, resonant interband tunnel diode (RITD), negative differential registration (NDR).

I. INTRODUCTION

Over the several decades, the world of electronics has been dominated by Si (Silicon) based technologies. Silicon is the principal component of most semiconductor devices, and most importantly integrated circuits (IC's). An example of such technology is the CMOS (Complementary Metal Oxide Semiconductor) circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM (Read Access Memory) and other digital logic circuits. CMOS is also used for a wide variety of analog circuits such as image sensors, data converters and highly integrated transceivers for many types of communication systems. Current modern technology is based on nanoelectronics (nanoscale) where integrated circuits are reduced in size (scaling) for high speed, less power consumption and simply using less physical space IC's for enhanced and improved application performances. This involves an integration of CMOS technology with various electronic devices. As the industry begins to address the theoretical limits of CMOS scaling, the current challenge is the integration of CMOS with new types of devices. The RTD, which utilizes electron-wave resonance in double potential barriers, has emerged as one of the most important testing grounds for modern theories of transport physics, and is central to the development of new types of semiconductor nanostructure. The "tunnelling devices" are candidates of new functional devices applicable to new integrated circuit technology in so-called "Beyond CMOS" region. Among the various tunnelling devices, the resonant tunnelling devices (tunnelling diodes) are promising because of their capability for high-speed operation, large Negative Differentiate Resistance (NDR) characteristics at room temperature, and adaptive design of device characteristics.

In this paper we will discuss the principle of tunnelling and different modelling techniques of tunnel diode which includes conventional tunnel diode, Esaki tunnel diodes based on vertical Si-Ge nanowire heterojunctions, heterostrucutre tunnel diode, and resonant interband tunnel diode.

II. PRINCIPLE OF TUNNELLING

Diodes are electrical semiconductor devices that allow electric current flow in one direction more than the other. The device depends on a depletion layer between N-type and P-type semiconductors to serve its purpose; when these are very heavily doped the depletion layer can be thin enough for tunnelling. Then, when a small forward bias is applied the current due to tunnelling is significant. This has a maximum at the point where the voltage bias is such that the energy level of the p and n conduction bands are the same. As the voltage bias is increased, the two conduction bands no longer line up and the diode acts typically. Because the tunnelling current drops off rapidly, tunnel diodes can be created that have a range of voltages for which current decreases as voltage is increased. This peculiar property is used in some applications, like high speed devices where the characteristic tunnelling probability changes as rapidly as the bias voltage.[1]

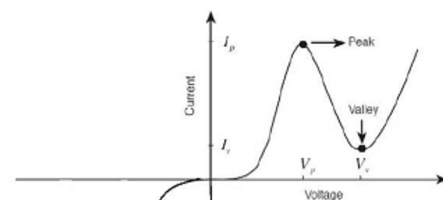

Fig. 1: I-V Characteristic of Esaki Tunnel Diode

The resonant tunnelling diode makes use of quantum tunnelling in a very different manner to achieve a similar result. This diode has a resonant voltage for which there is a lot of current that favours a particular voltage, achieved by placing two very thin layers with a high energy conductance band very near each other. This creates a quantum potential well that have a discrete lowest energy level. When this energy level is higher than that of the electrons, no tunnelling will occur, and the diode is in reverse bias. Once the two voltage energies align, the electrons flow like an open wire. As the voltage is increased further tunnelling becomes improbable and the diode acts like a normal diode again before a second energy level becomes noticeable. RTDs are very good rectifiers. [2]

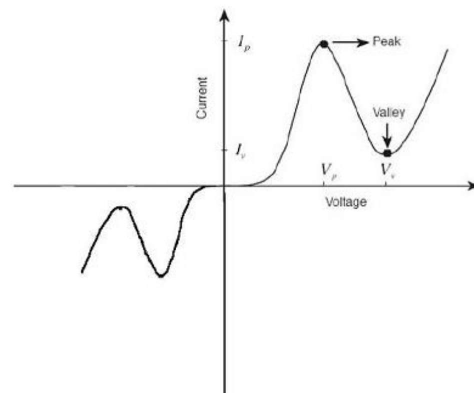

Fig. 2: I-V Characterstics of Resonant Tunnel Diode

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III. CONVENTIONAL OR ESAKI TUNNEL DIODE

The Conventional or Esaki tunnel diodes are simple PN junction diodes with high doping concentration (>1019) in both side n type as well as p type. Due to high doping concentration the depletion width of the junction became very narrow (less than 1000A) and narrow depletion width causes tunnelling of electrons.

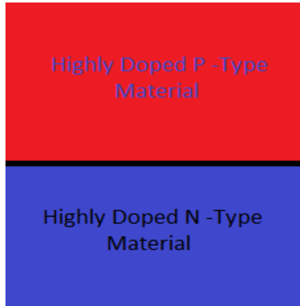

Fig. 3: Esaki Tunnel Diode

	Ge	GaAs	Si
I_P/I_V	8	15	3.5
V_P,V	0.055	0.15	0.065
V_V,V	0.35	0.50	0.42
V_F,V	0.50	1.10	0.70

Table 1: Typical Tunnel Diode Parameters

IV. ESAKI TUNNEL DIODES BASED ON VERTICAL SI-GE NANOWIRE HETEROJUNCTIONS

The device fabrication began with a Si (111) wafer degenerately doped with As to a resistivity of about 0.002 X-cm, which corresponds to an n-type doping level of $4x106^{19}cm^{3}$. 20 nm Au catalyst nanoparticles (Ted Pella, Inc.) were dispersed onto the substrate and vertical Ge nanowires were grown epitaxially using the vapour-liquid solid mechanism.14,15Nanowire nucleation took place at 380^0C for 1 min, followed by elongation at 300^0C for 45 min at a total pressure of 30 Torr (0.9% GeH4in H2). Fig. 4(a) shows a scanning electron microscopy (SEM) image of a representative vertical Ge nanowire, which is 20 nm in diameter and 1–2 nm in length. The sample was immediately transferred to an atomic layer deposition chamber where a 25 nm-thick conformal layer of Al_2O_3 was deposited at 150^0C. Next, the Al_2O_3film was selectively removed from the nanowires by masking the substrate with a 30 nm-thick layer of spin-on-glass (semiconductor grade 700B from Filmtronics, Inc.), followed by wet etching in a temperature controlled bath of 85% H_3PO_4 for 15 min. After a de-ionized (DI) water rinse and critical point drying, the sample was loaded into a tube furnace where a 2 nm-thick Si shell was grown around the nanowires at 465^0C and 5 Torr with a flow of 20 sccm SiH_4. The bottom portion of the core/shell nanowire was then encapsulated in a 250 nm-thick layer of spin-on-glass and cured at 300^0C for 45 min. To make electrical contact to the exposed upper portion, the sample was dipped briefly in buffered hydrogen-fluoride, rinsed in DI water, and immediately transferred to an evaporator where 100 nm Ni was deposited at an angle of 30^0–45^0 to ensure sufficient contact area between metal and nanowire. A drive-in current between the top and bottom contacts outside the nanowire contact window. Care was taken to ensure that the selected device under study contained only one nanowire. A schematic of the cross section of the completed device structure is shown in Fig.4(b).

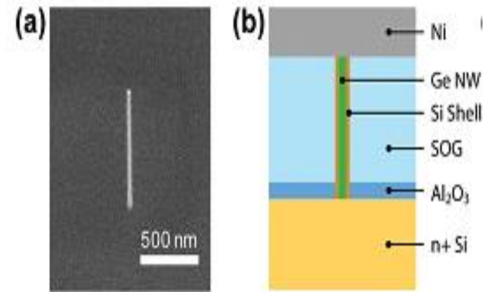

Fig. 4: Nanowire Tunnel Diode

In this technique a 2.75 peak to valley current ratio is achieve with high peak current density of 2.4 kA/cm^2, and high tunnelling current density of 237 kA/cm^2 at1 V reverse bias, all obtained at room temperature.[3]

V. TUNNEL DIODE HETEROSTRUCTURE DESIGN

In this work we use a Si/SiGe or two different material (heterostructure) for the tunnel diode fabrication. The diode consists of a highly doped p+ starting substrate upon which either intrinsic or partially doped SiGe was epitaxially grown and capped with a few nanometers of undoped Si. The Si and SiGe top layers were then doped n+ by proximity rapid thermal diffusion. The final device structure after the diffusion and before contact evaporation is shown in Fig. 5(a)

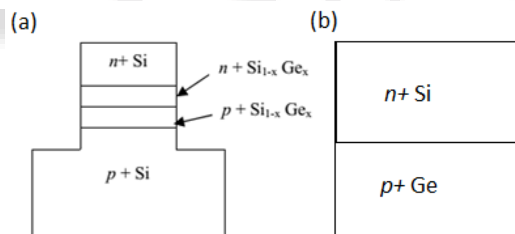

Fig. 5: The Si/SiGe heterostructure tunnel diode.

The thickness and position of the SiGe layer needs to be designed carefully in order to get the best depletion width and highest current density possible.[4]

VI. RESONANT INTERBAND TUNNEL DIODES:

There are five key features of the original structure of the Si/SiGe resonant interband tunnel diode (RITD) design: (i) an intrinsic tunnelling barrier called spacer (ii) d-doped injectors, (iii) off-set of the d-doping planes from the heterojunctions interfaces, (iv) low temperature molecular beam epitaxial growth (LT-MBE), and (v) post-growth rapid thermal annealing (RTA) for dopant activation and point defect reduction. The tunnel barrier in these structures nominally is defined by the placement of δ -doping planes; variations to the intrinsic layer between these planes allow the scaling of current density. Fig. 6 shows the RITD structure used as the control growth template in this study. [5]

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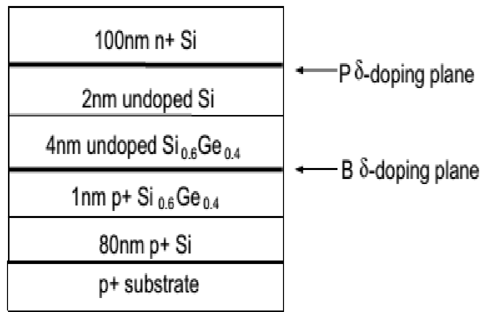

Fig. 6: Schematic diagram of the Si/SiGe RITD

VII. CONCLUSION

We have studied the principle of tunnelling and four different techniques to design/construct the tunnel diode and find that tunnel diode with interband/hetrostructures can be used for very high speed application and also the RITDs are very good rectifiers

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