Design and Analysis of 2:1 Multiplexer Using Low Power Adiabatic Technique and Its Application in Nibble Multiplexer

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Abstract—The power consumption and delay optimization has been the main concerns for the VLSI technology. In this paper we have proposed a new adiabatic circuit technique using diode connected transistors. The technique emphasizes on reduction of power by lowering the non-recoverable power consumption in adiabatic circuits. The technique achieves full adiabatic operation by providing separate charging and discharging paths. The PMOS devices provide the charging path while the diode connected NMOS devices provide low resistance discharge path which helps in reduction of power dissipation in the circuit. The paper compares the different logic style 2:1 multiplexes like CPL, EEPL and PFAL with the proposed design (ADDL) in terms of power and delay. The power consumption and delay is reduced up to a sufficient level with the help of new adiabatic logic technique. Nibble multiplexer is also designed using proposed logic. All the simulations have been performed at 90nm technology on Tanner EDA tool version 14.11.

Keywords:- Adiabatic Logic, 2:1 Multiplexer, PFAL, VLSI, T-Spice, Mux.

I. INTRODUCTION

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. Requirements for lower power consumption perpetuate to increment significantly as components become battery-powered, more minuscule and require more functionality. In the past the major concerns for the VLSI designers was area, performance and cost. Power consideration was the secondary concerned. Now a day's power is the primary concerned due to the remarkable magnification and prosperity in the field of personal computing contrivances and wireless communication system which demand high speed computation and intricate functionality with low power consumption. The motivations for reducing power consumption differ application to application. In the class of micro-powered battery operated portable applications such as cell phones, the goal is to keep the battery lifetime and weight plausible and packaging cost low. For high performance portable computers such as laptop the goal is to reduce the puissance dissipation of the electronics portion of the system to a point which is about a moiety of the total power dissipation. Finally for the high performance non battery operated system such as workstations the overall goal of potency minimization is to reduce the system cost while ascertaining long term contrivance reliability. For such high performance systems, process technology has driven power to the fore front to all factors in such designs.

In order to reduce the dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching, has been proposed in the last years. In such approach, the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved. In this paper we have proposed a new adiabatic technique .We have analyzed the various low power techniques like CPL, EEPL, PFAL and Proposed logic i.e. adiabatic diode discharge Logic (ADDL). Power and delay are the important factors calculated in this paper with the variation of power supply and frequency. The work is concentrated on design of low power multiplexer as Multiplexer is a basic block used extensively in communication systems, combinational circuits, data paths and FPGAs to implement logic functions. There are numerous designs of multiplexer which are based on pass transistor or transmission gates. The use of pass transistors provides optimum solution for multiplexer design with minimum number of devices. The inherent disadvantage involved in this technique is of low output swing. Different techniques have been proposed in designs like EEPL to restore the logic level at output. The designs are efficient in terms of device count and power but if we use adiabatic logic we can scale down power consumption dramatically. Such a design is presented [1] under the name PFAL MUX. The proposed design described in further sections shows better performance than PFAL in terms of power and delay.

A. Adiabatic Principle

The word ADIABATIC emanates from a Greek word that is utilized to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In authentic-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by decelerating the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat [4]. The adiabatic logic circuit is shown in figure 1.

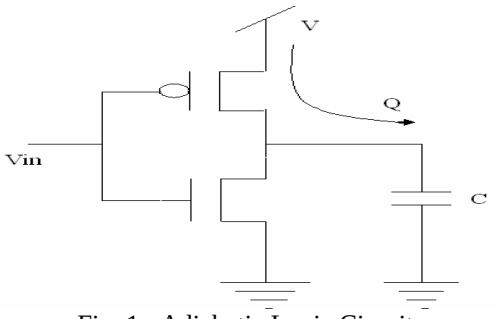

Fig. 1: Adiabatic Logic Circuit

The adiabatic logic is withal kenned as energy recovery CMOS. It should be noted that the plenary

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adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is decelerated. In most practical cases, the energy dissipation associated with a charge transfer event is conventionally composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requisites, this approach can sometimes be acclimated to reduce the power dissipation of the digital systems.

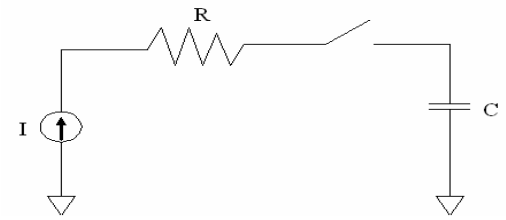

Fig. 2: Discharging Process of Adiabatic Logic

In fig. 2 output load capacitance is charged by a constant current source instead of a constant voltage source used in conventional CMOS structures. On resistance of pull up PMOS network is represented by R and C is the output capacitance [3]. Amount of energy dissipated through R can be given as

$$\text{Hence, } E = E_{diss} = \left(\frac{RC}{T}\right)CV^2 = \left(\frac{2RC}{T}\right)\left(\frac{1}{2}CV^2\right) \quad (1.1)$$

Thus energy dissipation depends upon on resistance R, by reducing it energy dissipation can be minimized. Also by increasing the charging time greater than 2RC dissipation can be reduced up to large extent. By reversing the direction of constant current source energy stored on capacitor can be achieved. Adiabatic circuits do not employ standard power supplies as in CMOS circuits, it uses pulsed power supply.

B. Multiplexer Designs

A logic style is the way how a logic function is derived from a set of transistors. It affects the speed, size, and power consumption and wiring complexity of a circuit. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance.[9]

C. CPL Design

A Complementary Pass-Transistor Logic (CPL) gate consists of two NMOS logic networks (one for each signal rail), two small pull-up PMOS transistors for swing restoration, and two output inverters for the complementary output signals. Fig. 3 depicts a two-input multiplexer which represents the basic and minimal CPL gate structure (ten transistors).

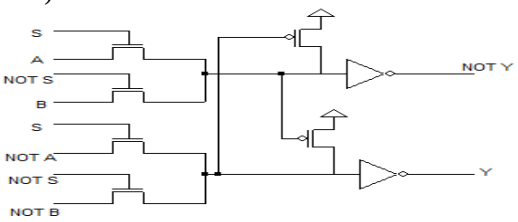

Fig. 3: 2:1 Multiplexer in CPL logic

D. EEPL Design

In the energy economized pass-transistor logic (EEPL), the sources of the PMOS pull-up transistors of a CPL gate are connected to the complementary output signal instead of Vdd. The main advantage of this design is smaller delay and smaller power dissipation compared to CPL [10-11]. Because of regenerative positive feedback which provides shorter delay than CPL logic.

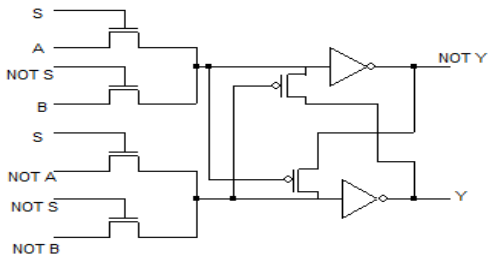

Fig. 4: 2:1 Multiplexer in EEPL logic

E. PFAL Design

This design 2:1 MUX is based upon a pair of cross coupled inverters. In this latch is made from two PMOS and two NMOS that avoids the degradation of the logic level at the output node. These NMOS devices are connected between output and ground. A sinusoidal supply is applied. This design works on the principle of adiabatic logic.[1]

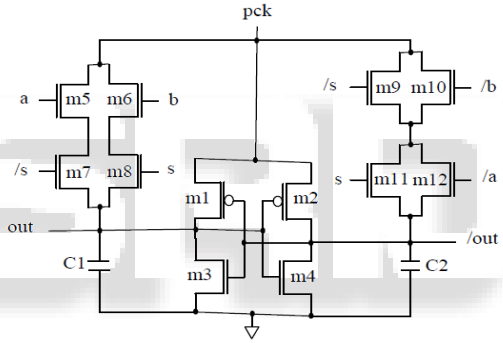

Fig. 5: 2:1 Multiplexer in PFAL logic

II. Proposed Multiplexer Logic

In the proposed 2:1 multiplexer logic the 2 PMOS & 10 NMOS transistors are used. This is the adiabatic diode discharge logic (ADDL) which consumes very less power as compared to PFAL Logic. Given below is the schematic for the proposed multiplexer logic. The new design is using diode connected transistors to achieve fully adiabatic operation without any residual charge at the output nodes. The PMOS devices provide the charging path once voltage at its gate (which is connected to out/outb) crosses the threshold. During charging of outputs the diode connected NMOS devices remain off as the Vgs (Gate to source voltage) is below Vt. Once the output charges completely, the discharge cycle begins. During this cycle the diode connected NMOS turn on and provide a low resistance (in comparison to logic branches) discharge path to pck. The low resistance path reduces power consumption in two ways in comparison to other designs. First is the design becomes fully adiabatic as there is no discharge path to ground in comparison to PFAL. Second is Low resistance path reduces the power wasted due to loss in resistance (I^2R) which is not recoverable during second cycle.

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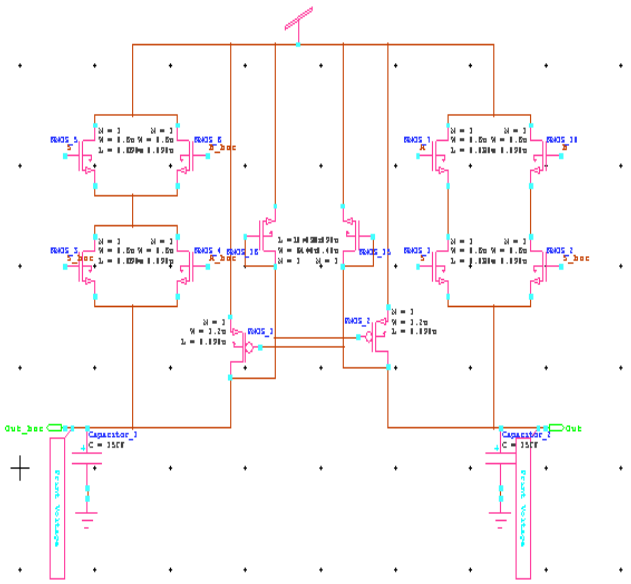

Fig. 6: Schematic of Proposed 2:1 Multiplexer

In this, the input terminals are A, A_bar, B, B_bar, S and S_bar. Vdd here is also given to supply power as well as clock to the circuit and thus called as Power clock. The Output terminals Out and Out_bar obtained complimentary to each other. Simulation is done on 90nm technology and the power dissipation & Delay are calculated with the variations of Vdd & frequency. The output waveform for the 2:1 multiplexer is shown below in the Fig. 7. Table -1 shows the effect of vdd variation on the power dissipation for various designs. All the results are calculated at 66MHz frequency at 90nm technology.

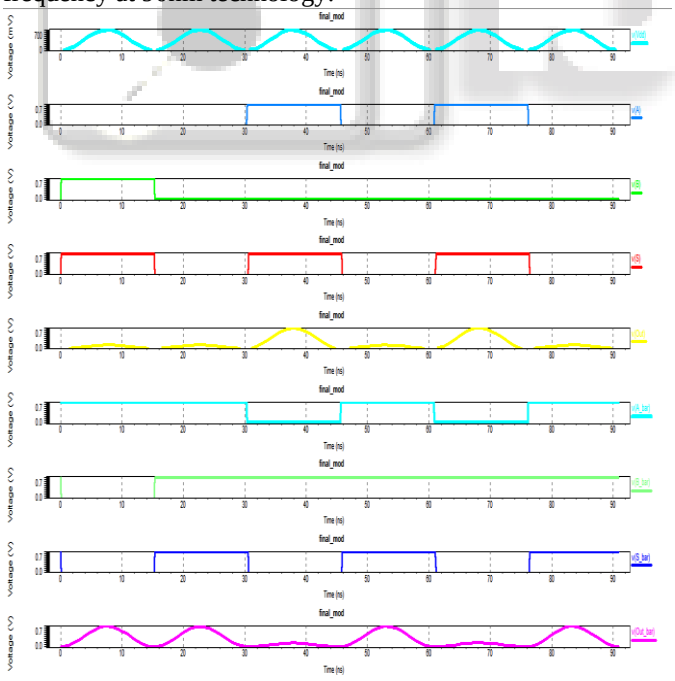

Fig. 7: Output Waveforms of 2:1 Multiplexer

In the output waveform First wave is vdd then two inputs A and B are shown. After that select line S and finally Output waveform is shown. Here inverted results are also shown after that.

Table.1 Comparison of CPL, EEPL, EEPL and Proposed logic in terms of Power (µW) and VDD

Technique	CPL	EEPL	PFAL	Proposed
VDD(V)	Power(µW)			
0.6	0.1179	0.0978	0.1863	0.1104
0.8	0.1948	0.1826	0.1260	0.0757
1	0.3604	0.2925	0.0966	0.0616
1.2	0.5241	0.4517	0.0910	0.0666

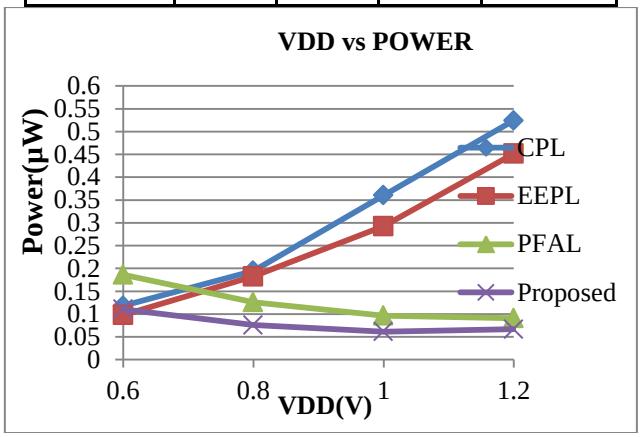

Fig. 8: Variations of CPL, EEPL, EEPL and Proposed logic in terms of Power (µW) and VDD

Table.3 shows the comparison of PFAL Logic and Proposed Logic in terms of power and delay at 1.2 volt power supply and 66MHz frequency

Table.3 Comparison of Proposed Logic with PFAL logic

Parameters	PFAL Logic	Proposed Logic
Power (µW)	0.09104	0.0666
Delay (ns)	0.11543	0.0437
PDP (W-s)	10.5095E-18	2.8638E-18

III. NIBBLE MULTIPLEXER USING PROPOSED LOGIC

A nibble multiplexer is a 4-bit multiplexer as shown in figure below:

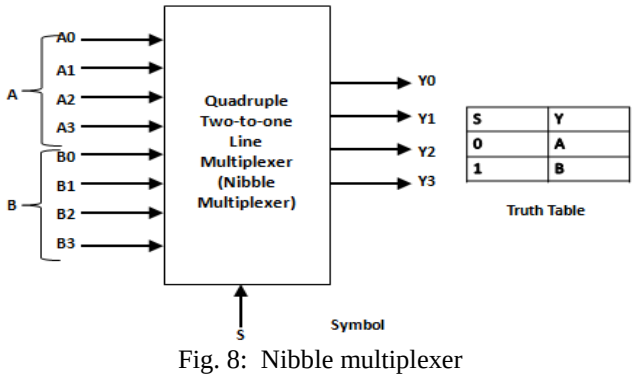

Fig. 8: Nibble multiplexer

Here four sets of 2:1 multiplexer are used such that this circuit is using a common select line to pass the one nibble of data or say four bits of data out of eight bits of data. It has been observed that the power consumed by the CMOS nibble multiplexer is more than the power consumed by the nibble multiplexer using proposed logic.

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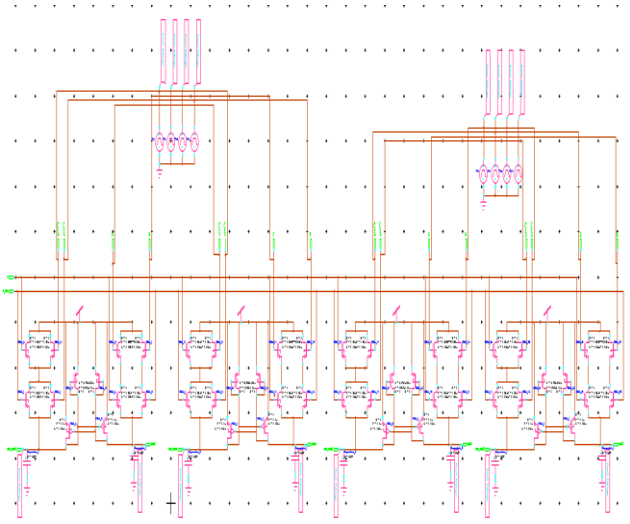

Fig. 9: Nibble Multiplexer using proposed logic.

IV. Power And Delay Comparison Of Nibble Multiplexer Using Cmos And Proposed Logic

Nibble Multiplexer using CMOS logic and proposed logic is implemented and compared in the tabular form. All these results are verified on 66MHz frequency and 1volt power supply using 90nm technology.

Table.2 Power and Delay for CMOS and Proposed Logic

Technique	Power(µW)	Delay(ns)
CMOS LOGIC	0.8155	0.2975
PROPOSED	0.2442	0.0941

V. Conclusion

We have designed and analyzed a new technique for the power reduction and delay optimization in the 2:1 multiplexer and by taking that in consideration a new nibble multiplexer has been designed and the results are compared with the conventional circuit. Results show. Proposed Multiplexer shows good performance with supply voltage variations as compare to EEPL, CPL, and PFAL multiplexer.

VI. Future Scope

The adiabatic technique is the latest in reducing the power dissipation in digital circuits. There can be improvement in the techniques of adiabatic logic. We have proposed one such Design Adiabatic diode discharge logic (ADDL). One can also Realize 4:1, 8:1, 16:1 multiplexers using 2:1 multiplexer. The future scope for the proposed design would be of great importance for the VLSI technology as the VLSI engineers are steadily working for the power reduction and higher performance.

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