Performance analysis of LSDCCFF at 90 nm technology

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Abstract— Average power consumption is a big issue in nanometer technology. With the reduction in process geometries, device density increases and threshold voltage along with oxide thickness decrease to keep pace with performance[1]. In this paper , a modified LSDCCFF[5] (Low swing differential conditional capturing flip flop) with reduced average power consumption is introduced.It operates with a low-swing sinusoidal clock by using reduced swing inverters at the clock port.. The circuits were designed and simulated in Tanner using 90 nm technology files. Average power consumption of modified circuit is reduced by 9.98% , D to Q delay is increased by 5% compared to low swing circuit.

Keywords: - Delay, flip-flop, low-swing, power, area.

I. INTRODUCTION

In recent years, the demand for low power-sensitive designs has grown significantly. This is mainly been due to the fast growth of battery-

operated portable devices such as notebook and laptop computers, personal digital assistants,cellular phones, and other portable communication devices. Semiconductor devices are aggressively scaled to achieve high-performance and high integration density. With the increase in density of transistors in a die and higher frequencies of operation, the power consumption in a die is increasing every technology generation. Supply voltage is scaled to maintain the power consumption within limit.

A variety of circuit techniques include transistor sizing,clock gating, multiple and dynamic supply voltage to reduce the dynamic power. For reduction in leakage power[4], techniques include, dual Vt_h, forward/reverse bias,dynamically varying the V_{th} during run time, sleep transistor[2], natural stacking.

Reduced swing inverters demonstrated in [3] are used at the node fed by the low-swing sinusoidal clock signal. This is done to decrease the effect of short circuit power. C. Kim. [7] showed that a low-swing square-wave clock double-edge triggered flip-flop allowed a 78%

power savings in the clock distribution network (CDN). Low-swing clocking requires two voltage levels, and these voltage levels can be generated by one of the two schemes: 1) dual-supply voltages and 2) regular power supply.Complexity in circuit and area of chip design and layout increases in first technique.However, it allows reduction in the number of clock network transistors thereby allowing improvement in power saving [8].

In this paper we have introduced a modified LSDCCFF(Low swing differential conditional capturing flip flop) with reduced average power consumption. The remainder of the paper is as follows:Section i describes different types of power dissipation followed by section ii which briefs different types of circuit. Section iii includes simulation and measurement results. The conclusion of the paper is provided in section iv.

II. DIFFERENT TYPES OF POWER DISSIPATION.

Two types of power dissipation that take place are :

A. *Static power dissipation*

B. *Dynamic power dissipation.*

Static power dissipation happens due to the leakage current and leakage current[6] occur due to the off transistor because some minutely current flow in off transistor whether it is PMOS or NMOS[10].

Dynamic power dissipation takes place due to the charging and discharging of a device.

$$P = ACV^2F \quad (1)$$

P is the power consumed, A is the activity factor, i.e., the fraction of the circuit that is switching, C is the switched capacitance, V is the supply voltage, and F is the clock frequency[9].

III. DIFFERENT TYPES OF CIRCUIT.

A. *LOW SWING CIRCUIT*

This circuit is the conventional LSDCCFF[1].The load PMOS transistor in the reduced swing inverter is always in saturation since Vgs=Vds. It reduces the voltage at the source of the second PMOS in each inverter to approximately Vdd-Vtp thus switching it off when the low-swing clock signal[8] reaches its peak voltage.

When the set glitch occurs ,data of D is transferred to Q but with a delay.Q and Q_B are the outputs of the NAND based SR latch. Schematic of low swing circuit is shown in Fig.1.

B. *Full Swing Circuit*

This circuit is similar to low swing circuit but without using reduce swing inverters.The operation of the circuit is similar to the low swing circuit. When the set glitch occurs ,data of D is transferred to Q but with a delay.Q and Q_B are the outputs of the NAND based SR latch.Schematic of full swing circuit is shown in Fig.2.

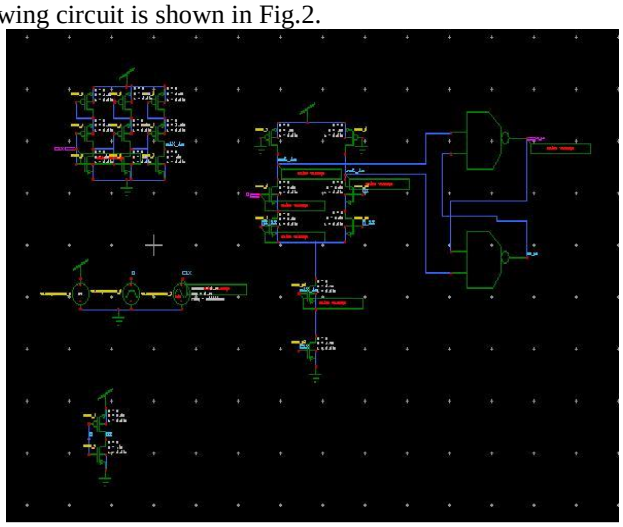

Fig. 1: Schematic for low swing circuit

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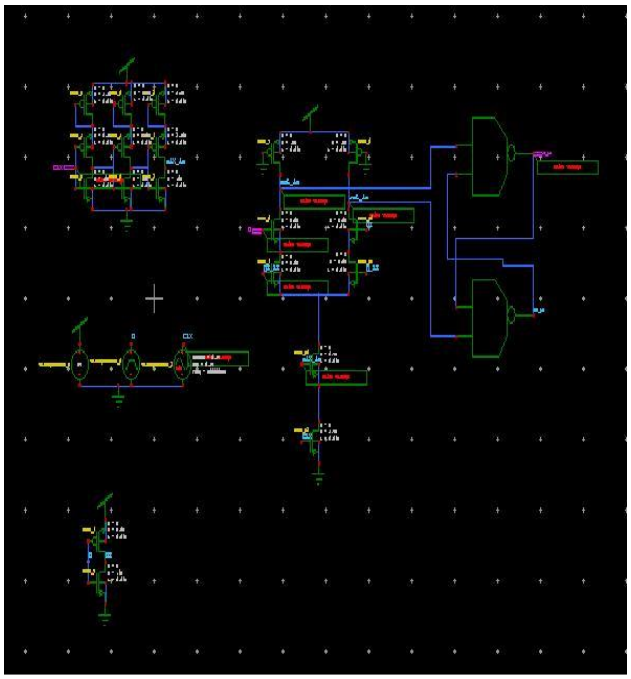

Fig. 2: Schematic for full swing circuit

C. Modified Circuit

This circuit is the conventional LSDCCFF[1] but with a modification.The load PMOS transistor in the reduced swing inverter is always in saturation since $V_{gs}=V_{ds}$. It reduces the voltage at the source of the second PMOS in each inverter to approximately $V_{dd}-V_{tp}$ thus switching it off when the low-swing clock signal reaches its peak voltage.

When the set glitch occurs ,data of D is transferred to Q but with a delay.Q and Q_B are the outputs of the NAND based SR latch.Two PMOS devices are added at the top which acts as a load to reduce the average power consumption.Schematic for modified circuit is shown in Fig.3.

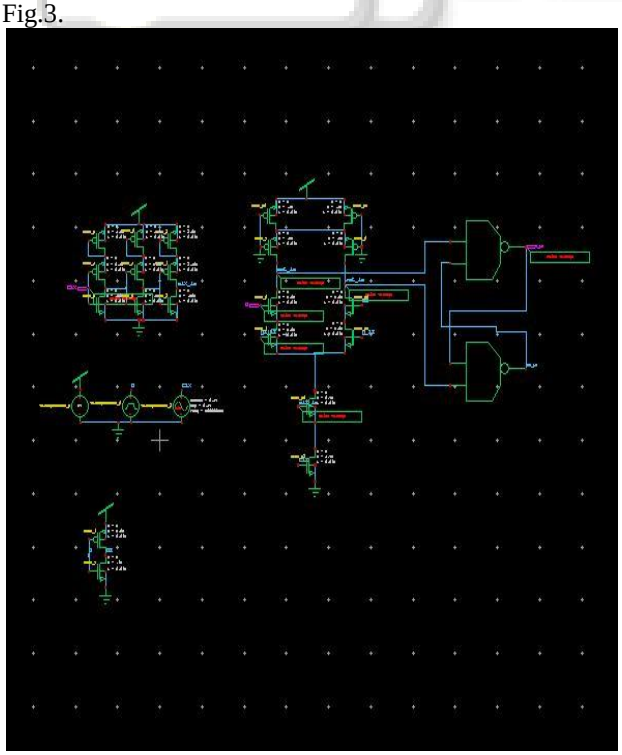

Fig. 3: Schematic for modified circuit

IV. Simulation Results

The simulation have been performed on Tanner.First the schematics are drawn using SEDIT.Then it is simulated with 90nm technology.Average power consumption ,and D to Q delay is observed in each case.

The simulation results for Power consumption, D to Q dealy is shown in Table 1.Figure.7. shows how Tanner is used to estimate Delay and other parameters.Sizing W/L of mos devices are kept such that functionality of circuit is not affected.Different Power and D to Q delay can be observed for different circuits.All simulations have been performed using 90nm technology.

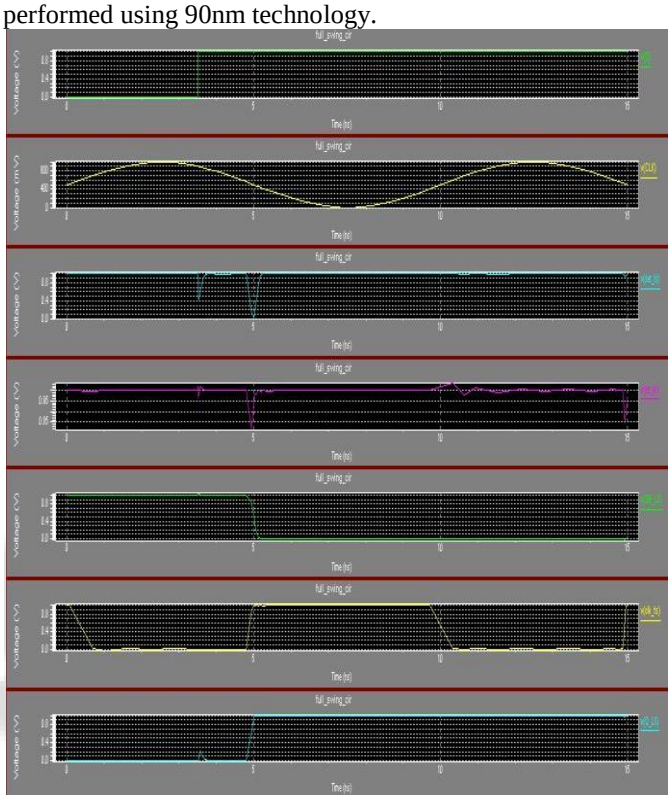

Fig. 4: Simulated output for full swing circuit

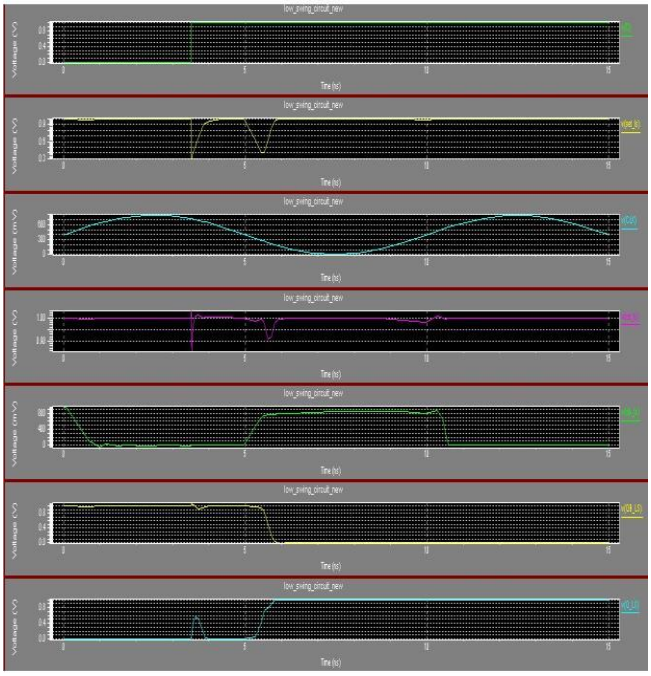

Fig. 5: Simulated output for low swing circuit

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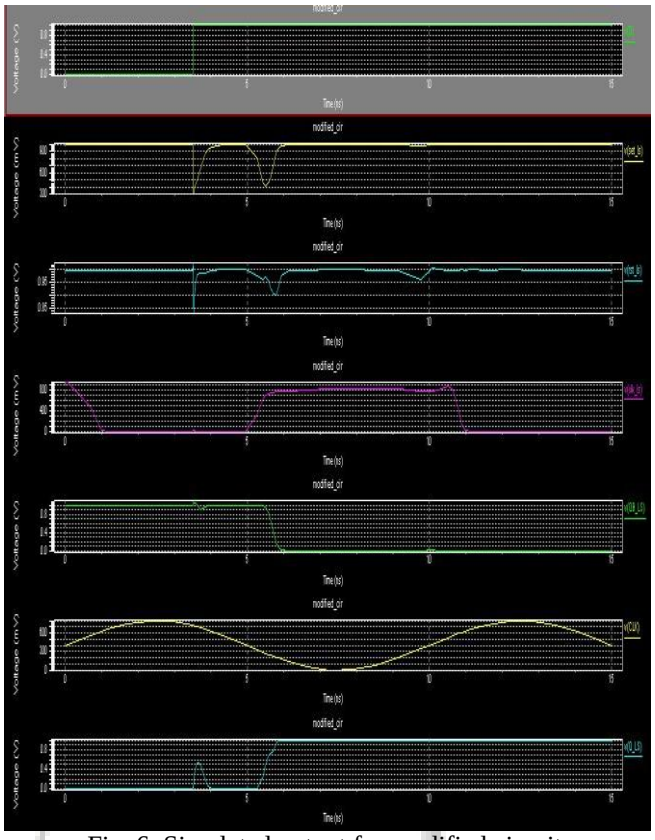

Fig. 6: Simulated output for modified circuit

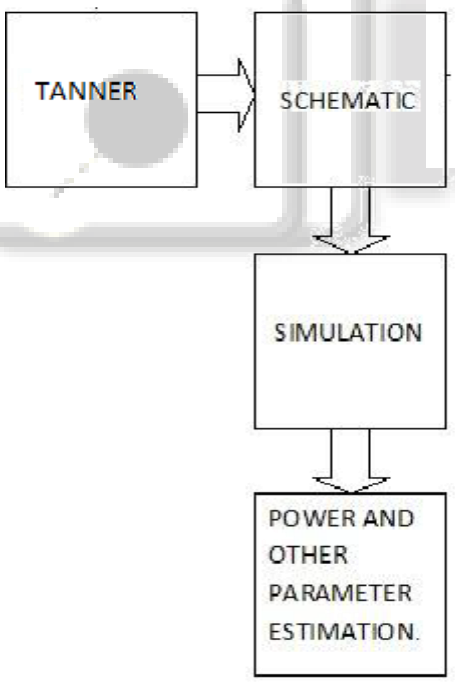

Fig. 7: Flow Graph for Power and other parameter estimation

Circuit type	D to Q delay(ns)	Average Power consumption(µw)
Full Swing	1.4	34.74
Low swing	1.9	8.61
Modified	2	7.75

Table 1. Power and other parameter comparison for different circuits.

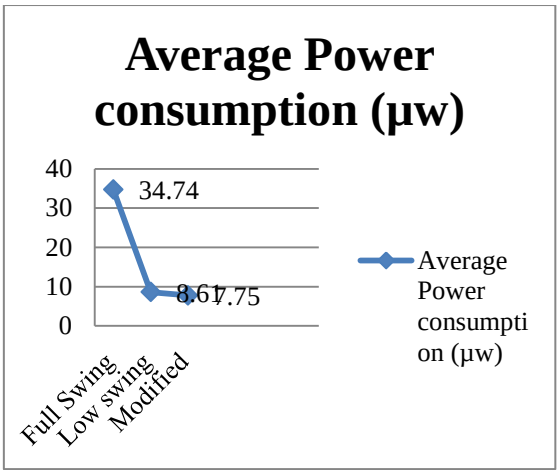

Fig. 8: Power dissipation graph for various circuits

V. CONCLUSION

This paper proposes a modified LSDCCFF with reduced power dissipation. Average power consumption of modified circuit is reduced by 9.98% and , D to Q delay is increased by 5% compared to low swing circuit.

The circuits were designed in 90 nm technology in Tanner. Reduced power consumption occurs due to voltage scaling. Further improvements can be done by exploring techniques to reduce delay which is a drawback in the case of modified circuit.

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