Descriptive Analysis of Clocked Paired Shared Flip-Flop for Low Power VLSI applications

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Abstract— The power consumption in VLSI circuits has become the most important factor for considering the efficiency of a circuit. The digital systems are required to operate at very low power and needs to be modified for the same. A Digital system consists of flip flops and latches which consumes a large amount of power due to redundant transitions and clocking systems. In order to reduce the power consumption we need to use the low power flip-flops for low power VLSI digital systems. In this paper we have taken a review of the low power clock paired shared flip-flop (CPSFF) for higher performance.

Keywords: Flip-Flop, Low Power VLSI Circuits, CMOS circuit.

I. INTRODUCTION

In the past, the major concerns of the VLSI design were area, performance, cost and reliability. Power consideration was mostly of only secondary paramount. In recent years, however, this has commenced to transmute and, increasingly, power is being given commensurable weight to area and speed considerations. One of the consequential factors is that exorbitant power consumption is becoming the inhibiting factor in integrating more transistors on a single chip or on a multiple-chip module. Unless power consumption is dramatically reduced, the resulting heat will inhibit the feasible packing and Performance of VLSI circuits and systems. Most of the current designs are synchronous which implicatively insinuates that flip-flops and latches are involved in one way or another in the data and control paths. One of the challenges of low power methodologies for synchronous systems is the puissance consumption of the flip-flops and latches. It is consequential to preserve power in these flip-flops and latches without compromising state integrity or performance. Power Consumption is tenacious by several factors including frequency f, supply voltage, data activity, capacitance, leakage and short circuit current. Circuit power which is caused by the finite elevate and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short period

$$P_{shortcircuit} = I_{short\ circuit} * V_{dd}.\ P_{leakage}$$

is the leakage potency. With supply voltage scaling down, the threshold voltage withal decreases to maintain performance. However, this leads to the exponential magnification of the sub threshold leakage current.

$$P_{leakage\ current} = I_{leakage\ current} * V_{dd.}$$

Based on the above factors, there are sundry techniques for lowering the puissance consumption shown as follows: In Double Edge Triggering, Using half frequency on the clock distribution network will preserve approximately a moiety of the puissance consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. Double clock edge triggering method reduces the potency by decrementing frequency. Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip- flop. The low swing method reduces the puissance consumption by decrementing voltage.

II. LOW POWER FLIP-FLOP DESIGN

There are three source of potency dissipation in digital complementary metal-oxide-semiconductor (CMOS) circuit i.e. Static power dissipation, dynamic power dissipation and short circuit power dissipation. Dynamic and short circuit power dissipation fall under the category of Transient Power Dissipation. Static power dissipation is due to leakage currents.

$$P= P_{Dynamic\ +}\ P_{short\ circuit} + P_{leakage}$$

Dynamic Power is also called as switching Power. It is caused by continuous charging and discharging of output parasitic capacitance. Short circuit power is the result when pull up and pull down network will conduct simultaneously. Leakage power dissipation arises when current flow takes place from supply to ground in idle condition. Power consumption is directly proportional to supply voltage, frequency and capacitance.

There are several techniques used to reduce the power of a digital circuit like low swing voltage, clock gating, Conditional operation, Double Edge triggering, Clock gating, Dual Vt/MTCMOS, Proposed Pulsed flip flop and reducing the capacity of clock load etc.

III. CLOCKED PAIRED SHARED FLIP-FLOP

Earlier we used to have Clocked Data Mapping Flip flops (CDMFF) instead of Clocked Paired Shared Flip-flops (CPSFF) as these are improved versions of CDMFFs. It has totall19 transistors including 4 clocked transistors as shown in Figure.

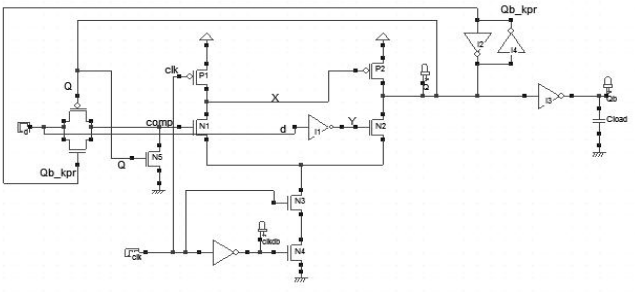

Fig. 1: CLOCKED PAIRED SHARED FLIP-FLOP (CPSFF)

The N3 and N4 are called clocked pair which is shared by first and second stage. The floating problem is avoided by the transistor P1 (always ON) which is used to

charge the internal node *X*. This flip flop will operate, when clk and clkdb is at logic '1'. When D=1, Q=0, Qb_kpr=1,N5=OFF, N1=ON, the ground voltage will pass through N3,N4 and N1 then switch on the P2. That is Q output pulls up through P2. When D=0, Q=1, Qb_kpr=0, N5= ON, N1= OFF,Y=1, N2= ON, then Q output pulls down to zero through N2,N3 and N4.The flip flop output is depending upon the previous output Q and Qb kpr in addition with clock and data input. So the initial condition should be like when D=1 the previous state of Q should be '0' and Qb_kpr should be '1'. Similarly when D=0 the previous state of Q should be '1' and Qb_kpr should be '0'. Whenever the D=1 the transistor N5 is idle, whenever the D=0 input transmission gate is idle.

IV. PROPOSED RESEARCH WORK

Our main aim is to reduce the power consumption and optimization of delay and to increase the performance of digital system. In order to reduce power double edge triggered flip-flop can be applied to reduce the power consumption or we can make the flip-flop independent of previous stage i.e. without initial conditions and removal of noise from the circuit.

V. CONCLUSION

We have done a survey of low power design for flip-flop for the combinational and sequential circuits and presented the design of low power flip-flops. In general, low power design for combinational and sequential circuits is an important field and gaining more importance as time goes by and will stay an important area of research for along time.

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