Low Power SOC Design Techniques

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Abstract—Power is a primary consideration in many segments of today's electronics business. The thriving market for wireless/mobile devices such as cell phones, laptop and net book, and home entertainment electronics such as set-top boxes, digital cameras and broadband modems, is driving the need for low-power and energy-efficient system-on-chip designs. Power reduction has become a vital design goal for sophisticated design applications. Power consumption in chips, especially for technology at 90nm or below, must be lowered in order to reduce the packaging, reliability, manufacturing and operational costs of these devices. In addition, energy consumption as well as the amount of power loss over time must be managed to extend the use time of battery-powered applications. So in this paper different techniques are discussed for designing of low power SoC.

Keywords: Static Power Dissipation, Dynamic Power Dissipation, Clock Gate, Power Gate, Multi Voltage, Multi Threshold, Substrate Biasing, Multi-bit Flip-flop

I. INTRODUCTION

The CMOS power dissipation has become a very hot topic during the last decade. The number of battery powered applications like mobile phones and laptop are steadily increasing and more and more functions are integrated into the systems. This is one of the driving forces for analysis of the mechanisms of power dissipation and power reduction techniques.

Irrespective of application, three components are attributed to power dissipation in digital CMOS circuits. Dynamic switching current is used in charging and discharging circuit load capacitance, which is composed of gate and interconnect capacitance. The greater this dynamic switching current is, the faster you can charge and discharge capacitive loads, and your circuit will perform better.

Short-circuit current flows between the power to ground when both P and N type of transistors can be on simultaneously for a rising signal is applied to input of CMOS inverter that is defined as the short circuit power. For circuit with fast transition times, short circuit power can be very small.

Leakage, or DC standby current, occurs because of sub-threshold conduction in MOSFETs. This current is independent of switching activity, but is a strong function of power supply voltage and operating temperature. Leakage current is usually small, but in large ultra low power designs (such as memories), it can represent the majority of the standby power consumed by the device.

II. LOW POWER TECHNIQUES

A. Clock Gating:

A significant fraction of the dynamic power in a chip is in the distribution network of the clock. 50% or more of the dynamic power can be spent in the clock buffers because they have the highest toggle rate in the system, there are lots of them, and they often have high drive strength to minimize clock delay. In addition, the flops receiving the clock dissipate some dynamic power even if the input and output remain the same. The most common way to reduce this power is to turn clocks off when they are not required. This approach is known as clock gating.

Modern design tools support automatic clock gating; they can identify circuits where clock gating can be inserted without changing the function of the logic. The figure shows how this works.

In the original RTL, the register is updated, or not, depending on a variable (EN). The same result can be achieved by gating the clock based on the same variable. If the registers involved are single bits, then a small saving occurs. If they are 32-bit registers, then one clock gating cell can gate the clock to all 32 registers (and any buffer in its clock tree). This can result in considerable power savings.

In the early days of RTL design, engineers would code clock gating circuits explicitly in the RTL. This approach is error prone – it is very easy to create a clock gating circuit those glitches during gating, producing functional errors. Today, most libraries include specific clock gating cells that are recognized by the synthesis tool. The combination of explicit clock gating cells and automatic insertion makes clock gating simple and reliable by reducing power. No change to the RTL is required to implement this style of clock gating.

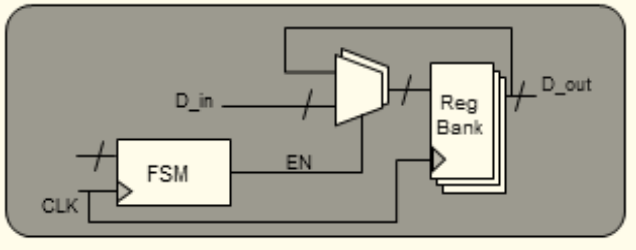

Fig. 1: Synchronous load enable Registers

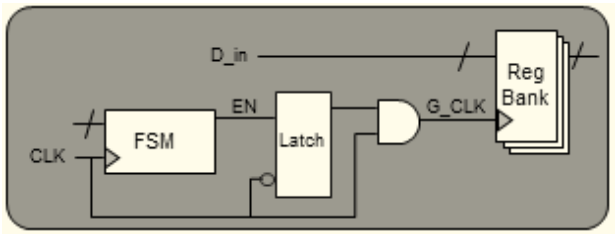

Fig. 2: Latch based Clock Gating

B. Power Gating:

Power-gating is one of the most effective standby-leakage reduction methods. The basic strategy of power gating is to provide two power modes: a low power, or shutdown, mode and an active mode. The goal is to switch between these

modes at the appropriate time and in the appropriate manner to maximize power savings while minimizing the impact to performance. Power gating is more invasive than clock-gating; it affects inter-block communication and adds significant time delays to safely enter and exit power gated modes but, where leakage reduction is critical MTCMOS power-gating is a more and more common method to do so.

To reduce the overall leakage power of the chip, it is highly desirable to add mechanisms to turn off blocks that are not being used. This technique is known as power gating. The basic strategy of power gating is to provide two power modes: a low power mode and an active mode. The goal is to switch between these modes (with the help of power gate cells) at the appropriate time and in the appropriate manner to maximize power savings while minimizing the impact to performance. One challenge for power gating designs is that the outputs of the power gated block may ramp off very slowly. The result could be that these outputs spend a significant amount of time at threshold voltage, causing large crowbar currents in the always powered on block. To prevent these crowbar currents, isolation cells are placed between the outputs of the power-gated block and the inputs of the always on block. These isolation cells are designed so that they do not experience crowbar current when one of the inputs is at threshold, as long as the control input is off. The power gating controller provides this isolation control signal.

For some power-gated blocks, it is highly desirable to retain the internal state of the block during power down, and to restore this state during power up. Such a retention strategy can save significant amounts of time and power during power up.

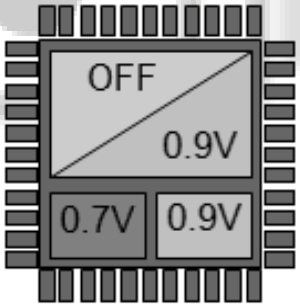

Fig. 3: Power Gating

One way of implementing such a retention strategy is to use retention registers in place of ordinary flip-flops. Retention registers typically have an auxiliary or shadow register that is slower than the main register but which has much less leakage current. The shadow register is always powered up and stores the contents of the main register during power gating. These retention registers need to be told when to store the current contents of the main register into the shadow register and when to restore the value back to the main register. This control is provided by the power gating controller.

Always-on buffers are used in power-off blocks to route signal from active block through the powered-off block to another active block. Special filler cells are used to connect n-well/p-well to global power/ground buses.

C. Substrate biasing:

Body biasing is a more complex method to reduce power. Voltages which differ from supply/ground are applied to the bodies of CMOS transistors which results in an increase of the threshold voltage and thus provides leakage reduction but a reduction of performance if a back-bias is applied. If a forward-bias is applied the performance of the design is improved but leakage is increased because of the decrease in the threshold voltage.

The body bias circuit technique utilizes the body terminal to dynamically modify the threshold voltage of a transistor during circuit operation. Depending upon the polarity of the voltage difference between the source and body terminals the threshold voltage can be either increased or decreased as compared to a non-body biased transistor. When a negative voltage differential is applied across the source-to-substrate p–n junction the reverse body bias increases the threshold voltage of a MOSFET. When the threshold voltage increases due to that the leakage of the transistor decreases and the activation time for the transistor increases. Thus, the performance of the circuit is decreasing.

An alternative body bias scheme is forward body biasing. When a positive voltage differential is applied across the source-to-substrate p–n junction, the threshold voltage of a MOSFET is reduced. When the threshold voltage is decreased in such condition the activation time for the transistor decreases thereby improving the performance of the circuit. When this is done, though, the leakage of the transistor increases.

With this technique it is thus possible to actively trade off leakage for performance with a small performance degradation improving leakage significantly and a small performance improvement degrading leakage significantly. Generally this technique is used for leakage reduction at 90nm and above. At 65nm, and especially below, the thresholds are small enough that leakage reduction using back biasing is insignificant

D. Multibit Flip-Flop:

Due to the rapid growth of the chip density and the increasing of clock frequency in the modern high performance designs, power consumption is an important issue in chip manufacturing. **P**ortable multimedia and communication devices have experienced explosive growth recently.

Longer battery life is one of the crucial factors in the widespread success of these products. As such, low-power circuit design for multimedia and wireless communication applications has become very important**.**

A large portion of total power dissipation in synchronous systems is due to the operation of flip-flops in clock network.

In the recent years, as the process technology advances, feature size of IC is shrank, the minimum size of clock drivers can trigger more than one flip-flop. As a result, merging 1-bit flip-flops into one multi-bit flip-flop by sharing the inverters in the flip-flops can reduce the total clock dynamic power consumption, and the total area contributed by flip-flops.

In this section, we will introduce multi-bit flip-flop conception. Before that, we will review single-bit flip-flop. Figure 4 shows an example of single-bit flip-flop. A single-

bit flip-flop has two latches (Master latch and slave latch).The latches need "Clk" and "Clk' " signal to perform operations, such as Figure4 shows.

In order to have better delay from Clk-> Q, we will regenerate "Clk" from "Clk'". Hence we will have two inverters in the clock path. Figure 4 shows an example of merging two 1-bit flip-flops into one 2-bit flip-flop. Each 1-bit flip-flop contains two inverters, master-latch and slave-latch.

Due to the manufacturing rules, inverters in flip-flops tend to be oversized. As the process technology advances into smaller geometry nodes like 65nm and beyond, the minimum size of clock drivers can drive more than one flip-flop.

Merging single-bit flip-flops into one multi-bit flip-flop can avoid duplicate inverters, and lower the total clock dynamic power consumption. The total area contributing to flip-flops can be reduced as well.

By using multi-bit flip-flop to implement ASIC design, users can enjoy the following benefits:

- Lower power consumption by the clock in sequential banked components
- Smaller area and delay, due to shared transistors and optimized transistor-level layout.
- Reduced clock skew in sequential gates

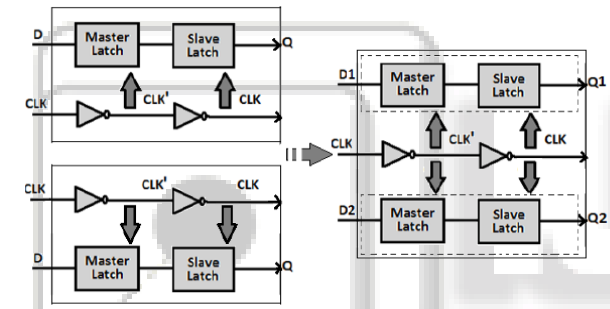

Fig. 4: Multi-bit Flip-flop[2]

E. Multiple Threshold Voltage:

When excessive power consumption became a problem, foundries started to offer libraries for low-power and high-speed design. For example, TSMC (Taiwan Semiconductor Manufacturing Co) offers a standard, or nominal, library; a high-speed library; and a low-power library, each having several types of cells. For instance, each of TSMC's libraries includes low-threshold-voltage, high-threshold-voltage, and threshold-voltage-with-MTCMOS (multi-threshold-CMOS) cells. Multiple-cell libraries help designers deal with both leakage and dynamic power. To deal with leakage power using multiple types of cells, designers today employ multi-threshold design.

Multiple threshold voltage techniques use both Low Vt and High Vt cells. Use lower threshold gates on critical path while higher threshold gates off the critical path. This methodology improves performance without an increase in power. Flip side of this technique is that Multi Vt cells increase fabrication complexity. It also lengthens the design time. Improper optimization of the design may utilize more Low Vt cells and hence could end up with increased power.

There are multiple ways to implement MTCMOS in synchronous circuits. One method is to use low threshold (low-Vt) transistors to build the circuit units on critical paths, while those on non-critical paths use high threshold (high-Vt) transistors. This allows the critical paths of a circuit to retain high speed, but use less leaky transistors in portions of the circuit with lower speed requirements. In addition to this path replacement methodology, there are two other architectures of implementing MTCMOS.A large scale technique is to use low threshold logic for all circuit functions and to gate the logic with high threshold sleep transistors between the logic and the power source, as shown in Figure 1.The sleep transistors are controlled by the Sleep signal. During the active mode, the Sleep signal is de-asserted, causing both high-Vt transistors to turn on and provide a virtual power and ground to the low-Vt logic. When the circuit is inactive, Sleep signal is asserted, forcing both high-Vt transistors to cut-off and disconnect the power lines from the low-Vt logic; this results in a very low sub-threshold leakage current from power to ground when the circuit is in standby mode. The drawback of this method is that partitioning and sizing of the sleep transistors is difficult for large circuits.

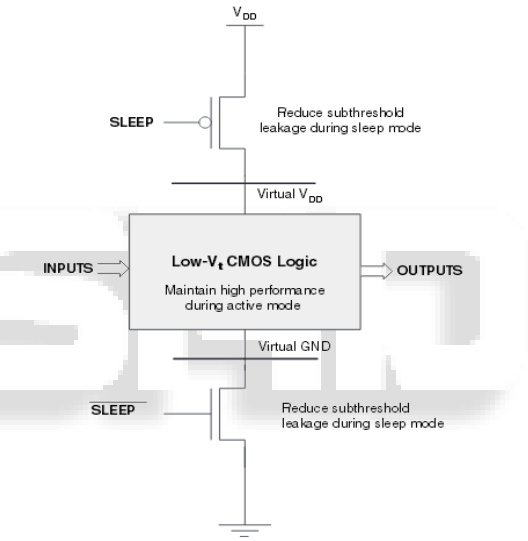

Fig. 5: SOC MT CMOS[3]

F. Multivoltage Design:

Although multi-threshold design helps engineers to minimize leakage of their designs through the use of multiple libraries. Similar to multi-threshold design, multi-voltage design enables designers to give the critical paths and blocks in their designs access to maximum voltage for the process and specification, but the designers then reduce the voltage for less power-hungry blocks. For example, a processor block may require a clock speed of 500 MHz, but a USB core may require only 30 MHz to comply with the USB protocol and thus require less voltage to run. So, if designers give the USB core only the power it needs, they can drastically reduce the overall power the design consumes. To implement the method, designers traditionally put level shifters between blocks that are running at different voltages. "If you have a 0.9V region on your IC design that is sending a signal to a 1.2V region, you have to put a level shifter between the two regions so you can boost it to the swing in voltage and control timing.[4]

Although a fairly simple concept, its implementation is more complex. First, designers must get

used to dealing with multiple voltages on a die. There are also some fairly significant challenges on the tools front. Most commercial synthesis and physical-design tools can insert level shifters and can perform multi-voltage, but creating RTL is a problem. "HDLs don't yet have a mechanism for describing power connectivity". This lack is one area that EDA vendors are addressing by trying to implement a low-power standard.

Dynamic voltage scaling and frequency scaling (acronym shorted to DVFS) use power controller and, depending on the required performance, the supply voltage on certain blocks can be increased or decreased during normal operation to conserve power. When the supply voltage is lowered on a block, its operating frequency may need to be lowered to maintain its functionality. This is "frequency scaling" portion of DVFS. If frequency scaling is not implemented, then we have simply dynamic voltage scaling (or just DVS). In addition, if blocks are non-critical for a functional mode they can be turned off altogether.

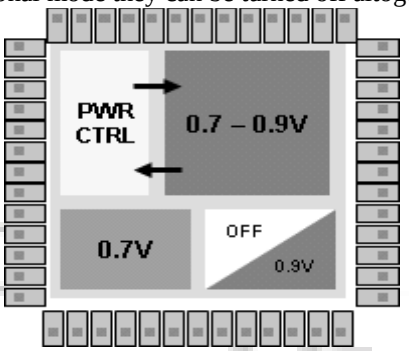

Fig. 6: Dynamic voltage & Frequency scaling

III. CONCLUSION

Power consumption affects the overall structure of the design and impacts on power grid. As we move to smaller technologies, power management and power grid design becomes even more critical. Low power SoC design techniques illustrated in this paper is very helpful for power management in SoC. The below table give the idea of different power component should be optimize by particular techniques for Soc design.

Low Power Techniques	Dynamic Power	Standby Leakage Power	Active Leakage Power
Clock Gating	✓		
Power Gating	✓	✓	
Substrate biasing			✓
Multi-bit Flip-flop	✓		
Multi Vth			✓
Multi Voltage Design	✓		✓

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