Performance Analysis and Comparison of Self-Calibrating Dynamic Comparator and Advanced Double-Tail CMOS Dynamic Comparators

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Abstract—This advanced double-tail dynamic comparator has two extra inverters which are inserted in the conventional double-tail dynamic comparator by which gain of the overall circuit is improved. The additional regenerative part of this helps in increasing the driving current at the output stage of the comparator. These circuits are designed using 180nm Technology and CMOS at a power supply of 1.8V and it performs better in the sensitivity to delay and also the offset voltage is reduced in this circuit as compare to the preamplifier stage based comparator, the area and power consumption used by this circuit is almost comparable.

I. INTRODUCTION

Because of higher input impedance, lower power consumption and delay, dynamic latched comparators are now widely used for many applications such as high-speed ADCs, in data converters etc. But the offset voltage which is introduced due to the threshold voltage V_{th} and parasitic capacitance due to nodes and the capacitance on the output side due to load's mismatches have limited the accuracy of the comparators in[1][2]. The preamplifier stage reduces the input offset voltage and it also helps in reducing the kickback noise and hence a lower input offset voltage can be achieved in case of a preamplifier which is followed by a latched output stage. But this stage based comparator have disadvantage of more power consumption due to the presence of more number of transistors and also the reduction in intrinsic gain due to the reduction of the resistance because of continuous technology scaling[3]. Having so many advantages, the dynamic comparators presented in [4][5] have been widely used. The latched comparator gives higher gain and the positive feedback saturates the output. But due to the presence of tail transistor the current flowing through both of the output branches and the effect of which is a dependency of V_{com} voltage on the speed and offset voltage [4]. To overcome these comparators having different input and output stages was introduced in [6]. By introducing this the comparator have a lower and more stable offset voltage over wide input common-mode voltage (V_{com}) ranges and operate at a lower supply voltage (V_{DD}) as well. Since it requires both *Clk* and *Clkb* signals for its operation, the timing between the two stages should be highly accurate so as the time for detecting the ΔV of the initial stage is not mismatched. When the second stage clock is replaced with the difference output of the first stage the issue of having two different clock pulses is removed but by doing so the signal given to the second input will not be that strong to drive it. As a result, *Clk* load was lessened and the input-referred offset was reduced as well since the gain for the output-latch stage was improved. The slope of the signal is lesser as compare to that was in case of the clkb signal and due to which the delay factor can increase above a value showing a slow exponential decaying shape, and the maximum drive current for each output was reduced to half of the single output tail current comparing to the comparator in [6]. The organization of the rest of the sections of the paper is as follows. In the next section we have the proposed dynamic comparator and we will be comparing its performance with the already existing works, in the section III the optimization of the proposed comparator is described and the conclusion is followed in section IV. The simulation graphs are also being attached along with the schematic of the proposed circuit.

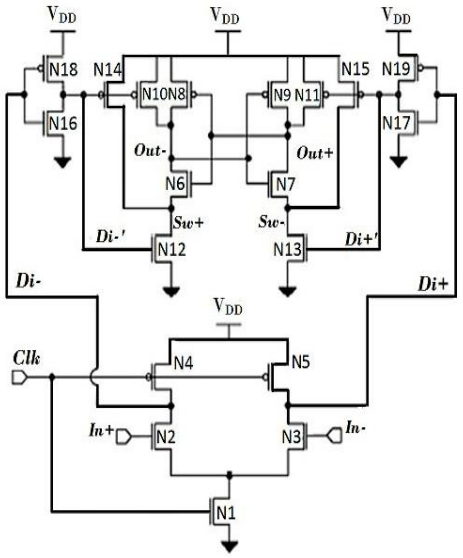

Fig. 1: Proposed Comparator Circuit

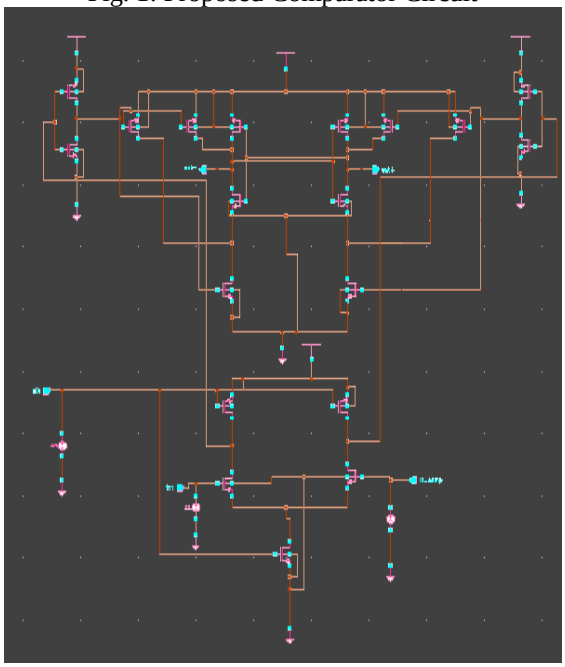

Fig. 2: Schematic made on cadence

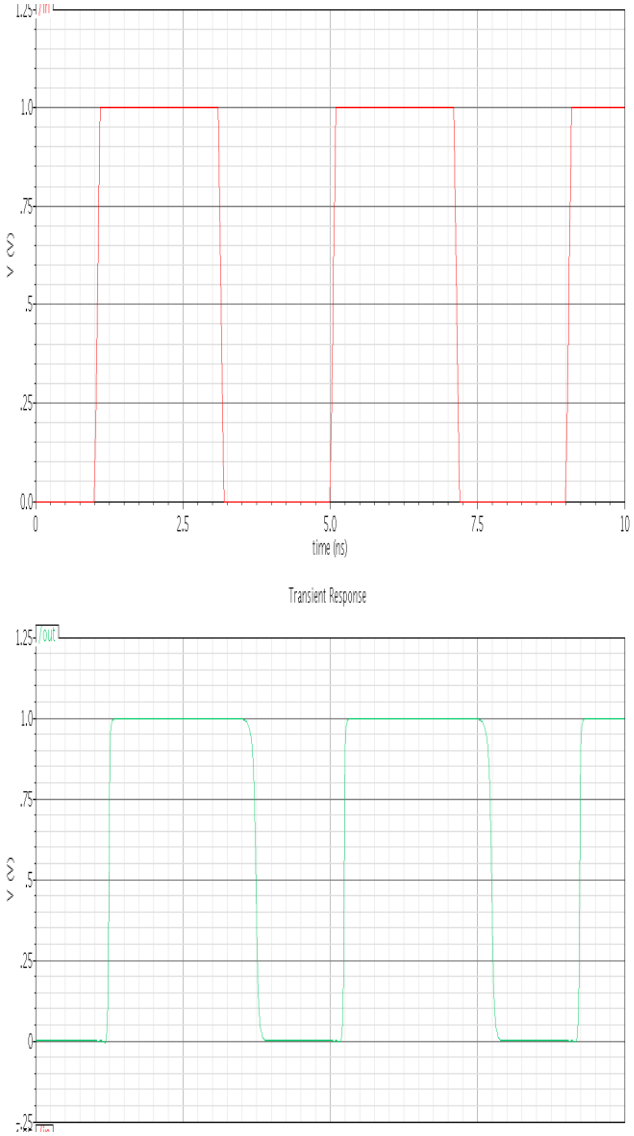

Fig. 3: Signal Behavior of Proposed Comparator

II. Proposed Circuit And Comparison With The Available Work.

The schematic of the proposed comparator is shown in Figure 1 and its cadence mode is shows in the figure 2. The software used for circuit designing and simulation is Cadence Analog Suite (Virtuoso) at 180nm CMOS Technology (VDD=2V and common mode Voltage V_{com}=1.8V). The basic structure of the proposed comparator stems from the comparators from the self calibrating dynamic comparator and the double tailed comparator as given in [6] and [7]. Due to which it has a better input offset characteristic and high speed operation with also having the advantage of the previously used comparators such as less kickback noise, reduced clock load and removal of the timing requirement between *Clk* and *Clkb* over a wide common-mode and supply voltage range. For its operation, during the pre-charge (or reset) phase (*Clk=0V*), both PMOS transistor N4 and N5 are turned on and they charge *Di* nodes' capacitance to *VDD*, which turn both NMOS transistor N16 and N17 of the inverter pair on and *Di'* nodes discharge to ground. Sequentially, PMOS transistor N10, N11, N14 and N15 are turned on and they make *Out* nodes and *Sw* nodes to be charged to *VDD* while both NMOS transistors N12 and N13 are being off. During the evaluation (decision-making) phase (*Clk=VDD*), each *Di* node capacitance is discharged from *VDD* to ground in a different time rate proportionally to the magnitude of each input voltage. Because of which there is a formation of input dependent differential voltage in between *Di+* and *Di-* node. Once either *Di+ or Di-* node voltage drops down below around V_{DD}- $|V_{tp}|$, the additional inverter pairs N18/N16 and N19/N17 invert each *Di* node signal into the regenerated (amplified) *Di'* node signal. Then the regenerated and different phased *Di'* node voltages are amplified again and relayed to the output-latch stage by transistor N10- N13. As the regenerated each *Di'* node voltage is rising from *0V* to *VDD* with a different time interval, transistor N12 and N13 turn on one after another and the final amplification is made between *SW* nodes before the regeneration process. Once either of *SW* node voltages falls below around V_{DD}- *Vtn*, the output latch stage starts to regenerate the small voltage difference at *Out* nodes into a full-scale digital level: *Out+* node will output logic high (V_{DD}) if the voltage difference at *Di'* nodes $\Delta Di'(t)$ is negative *(Di+'(t) < Di-'(t))* and *Out+* will be low (*0V*) otherwise. Once either of *Out* node voltages drops below around V_{DD}- $|V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor N8 or N9 will turn on.

To compare the performances of the comparators from [6][7] with the proposed one in a fair way, each circuit was designed at a same area and designed to have the same transconductance for each input transistor pair (N2 and N3) by sizing their widths to *2µm* and setting $C_{Di}/I_{2,3}$ (D_i node capacitance/drain current of N2 and N3) ratio constant. After setting the widths of the mismatch critical transistors to have relatively large size (*>1µm*), the rest sizes of transistors are optimized for high speed, low offset and less power consumption.

The transistor N16-19 also implies extra delay in the circuit but even then the proposed comparator outputs faster decision over the comparator from [6]. As the size of the load gets larger, the proposed comparator shows better speed in general over the comparator [6] since the proposed comparator can drive more current to the load than the comparator [6] and [7] at the same area of the output-stage.

For comparing the offset voltage of each comparator, random mismatch in threshold voltage V_{th} and current factor β(= $C_{ox}W/L$) for each transistor pair were modeled as follows,

σ_{vth} $A_{vth}/\sqrt{WL}$ where W,L are in µm (1)

σ_{β} $A_{\beta}/\sqrt{WL}$ where W,L are in µm (2)

A_{vth} and A_{β} are process dependent parameters. The overall performance comparison of each comparator is summarized in Table 1. The fifth column in Table 1 shows the resulting total offset voltages (σ_{vos}) for each comparator, which were obtained by applying V_{com}=*1.8V* and V_{DD}=*2V*. The second and third columns show the number of transistors and total channel widths of the transistors, which can be considered as approximate measures of circuit complexity and chip area. The fourth column is the delays (ps) per the input voltage differences (*log (Δ Vin) or decade*) of each comparator. The sixth and last column in Table 1 show that

the proposed comparator consumes even less energy than the comparator [6] while presenting more stable *delay/log(ΔV_{in})* and even less input-referred latch offset voltage at the same area. The working and comparison of our work has been given in this and the result comparison table is given as below.

	No. of transistor	Delay(ps)	Offset voltage(mV)	Energy(fJ)
Comparator(7)	15	45	15.8	59.1
Comparator (6)	14	33	20.1	66.2
Proposed comparator	19	22	17.2	60.08

Table 1: Performance comparison

III. Optimization Of The Proposed Comparator

To further reduce the offset voltage of the proposed comparator, it is necessary to find the most critical mismatch transistor pair first. Since transistor N2 and N3 pair is the input transistors and starts to operate in the saturation region during evaluation phase, they are the most critical mismatch pair for the total offset voltage and the offset voltage caused by the mismatch between them can be expressed as [8] which shows that *VOS2,3* is affected by device mismatches and bias conditions. It implies that the total offset voltage increases directly proportional to the threshold voltage mismatch *Vtn2,3* and also increases with the increase of the common mode voltage *Vcom*, *Di* node capacitance mismatch (which is mostly the gate capacitance mismatch of the inverter pair), and the current factor *β2,3* mismatch. From (1) and (2), it is clear that the offset voltage can be reduced by increasing transistor size.

In addition, to minimize the input-referred offset voltage of the output-latch stage, the gain of the dynamic preamplifier should be maximized. By assuming that $\lambda=\Upsilon=0$ for simplicity, since both transistor N2 and N3 operate in the saturation region between the time *t1* and *t2* (t1: time at which transistor N1 is just turned on at the rising Clk edge and transistor N2 and N3 start to operate in the saturation region, t2: time at which either of transistor N2 or N3 moves out of the saturation region operation and goes into the linear region operation), the drain-to-source currents of N2 and N3 are constant over [*t1*, *t2*]. By integrating both sides of (3) over [*t1*, *t*] and applying the initial condition: *VDi(t1)=VDD*, the following equations are obtained;

$$V_{Di-}(t) = V_{DD} - (I_{D2}/C_{Di-})t$$
$$V_{Di+}(t) = V_{DD} - (I_{D3}/C_{Di+})t \quad (4)$$

By applying the small-signal approximation and assuming that *CDi- = CDi+ = CDi*, the dynamic gain of the differential input stage can be defined as

$$A_{v1}(t) = (\Delta V_{Di}/\Delta V_{in})t\ g_m/C_D \quad (5)$$

Equation (5) shows that as long as transistor N2 and N3 operate in the saturation region, the dynamic gain *AV1(t)* keeps increasing with the increasing time. To maximize the gain *|AV1(t)|*, *|gm/ID2,3|* should be maximized because the integration time *t* is proportional to *CDi/ID2,3* from (6). This can be simply done with reducing the size of transistor N1. However, as equation (6) also indicates, the reduced *ID2,3* increases the discharging time of *Di* node voltages during evaluation phase. Therefore, the higher gain can be achieved at the cost of the increased delay.

Furthermore, by increasing the channel length of the input transistor, for example 180nm to 240nm in 180nm technology, one can get higher gain with the same W2,3/L ratio by reducing short-channel effects such as a dynamic conductance variation due to DIBL. If a negative supply voltage is available, by replacing the ground of the input differential pair with a negative supply voltage and further reducing the size of transistor N1, one can get wider common mode input range. Therefore, this differential input stage can be designed in a different way depending on the requirements such as the speed, offset voltage and common mode input voltage range.

From the simulation results, the dynamic voltage gain up to around *12 V/V* can be easily obtained, where around 1.8 times of the gain is produced by the inverter pairs *(N18/N16 and N19/N17)* followed by *Di* node gain of around *8 V/V*. It means that the offset referred voltage is reduced. Therefore, the output stage of the comparator has become less sensitive to the offset voltage and because of that the size of it can be maintained not to be too large. But the offset voltage of the inverting pairs is a issue for which we have to increase the size so that offset requirement can be achieved.

IV. Conclusion

The paper presents the low power comparator which is having a lower offset voltage and also has lower delay in comparison to the Self-Calibrating Dynamic Comparator. It has approximately 50% delay factor in comparison to the Self-Calibrating Dynamic Comparator and the power consumed in the circuits is comparable.

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