# Performance Analysis of a High Speed and Power Efficient Full Adder at 65nm

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*Abstract*---In this paper presents an 8T full adder is designed to achieve lower average power and delay in comparison to 10T, 11T and 16T full adder designs. This design is carried out by the technique of Gate Diffusion i.e.GDI by reducing number of transistor counts which operates at very low voltage and offers a higher computation speed. The performance of the proposed full adder is evaluated by the comparison of the simulation result obtained in tanner tools using 65nm CMOS process technology with a supply voltage of 1.2V.

**Keywords:** CMOS technology, Gate Diffusion Technique, 8T full adder, 10T full adder, 11T full adder, 16T full adder

## I. INTRODUCTION

Addition is a basic operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is very much influenced by the performance of the resident adders. Adders are also very essential component in digital systems because of their widespread use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would seriously advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analysing its power dissipation, layout area and its operating speed.

In electronics, an adder or summer is a digital circuit that performs addition of binary numbers. In computers and many other kinds of processors, adders are used not only in the arithmetic logic units, but also in calculating addresses, table indices, and similar operations. Full adder is the basic unit in circuits used for performing arithmetic operations such as multiplications, parity checking. So they are also used as compressors, large adders, comparators and parity checkers, multipliers.

## II. RESEARCH BACKGROUND

Several variants of static CMOS logic styles have been used to implement low-power 1-bit adder cells. In general, they can be generally classified into two main categories: the complementary CMOS and the pass-transistor logic circuits. The complementary CMOS full adder based on the regular CMOS structure with PMOS pull-up and NMOS pull-down transistors. The benefit of complementary CMOS method is its robustness against voltage scaling and transistor sizing, which are necessary to present reliable operation at low voltage CMOS circuit is straight forward and area-efficient due the development of cell libraries. They are likely to maintain the ability to further decrease the cost-per-function and enhance the performance of integrated circuits.

### *A. Implementation and Simulation of 16T and 11T Full Adders*

We have discussed the 10T full adder in the review paper and its schematic and power consumption has also been reviewed. The schematic of 16T on tanner tool with 65nm process technology is shown in Figure 1 and it contains PMOS and NMOS and three vpulse is added in it and one vdc supply is connected to the port of inverter in this we take 1.2V voltage supply and we can take pulse width, rise time and fall time of vpulse in different ratio.

### *B. 16T Full adder Implementation*

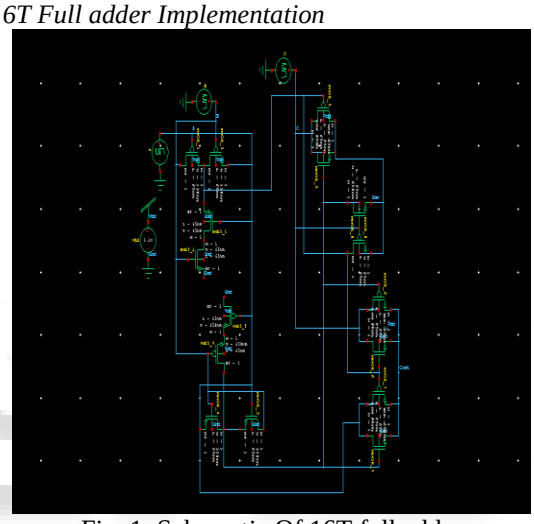

Fig. 1: Schematic Of 16T full adder

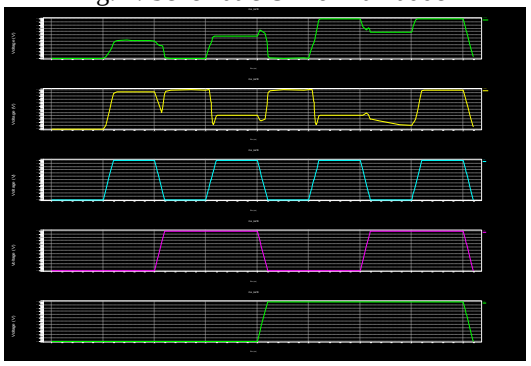

Fig. 2: output Waveform of 16T full adder

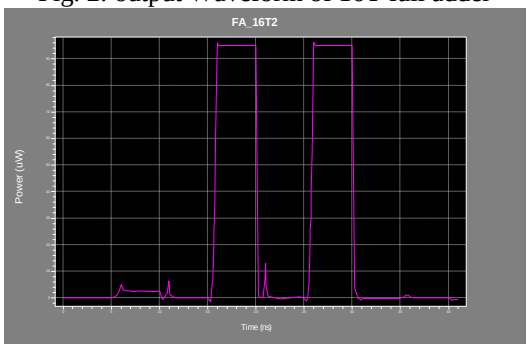


Fig. 3: Leakage power of 16T full adder

 

### *C. 11TFull Adder Implementation*

The schematic of 11T full adder on tanner tool with 65 nm process technology is shown in figure. It contains PMOS and NMOS and three vpulse is added in it and one vdc supply is connected to the port of inverter in this we take 1.2V voltage supply and we can take pulse width , rise time and fall time of vpulse in different ratio.

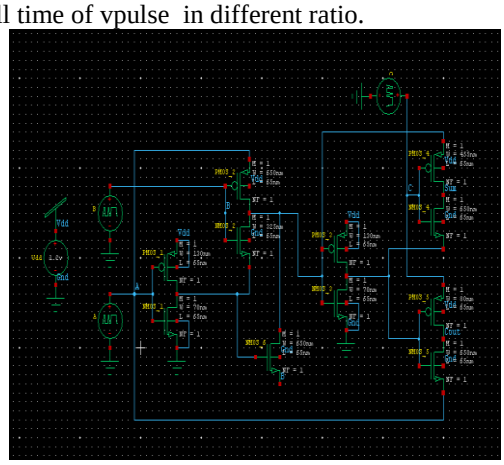

Fig. 4: Schematic of 11T full adder

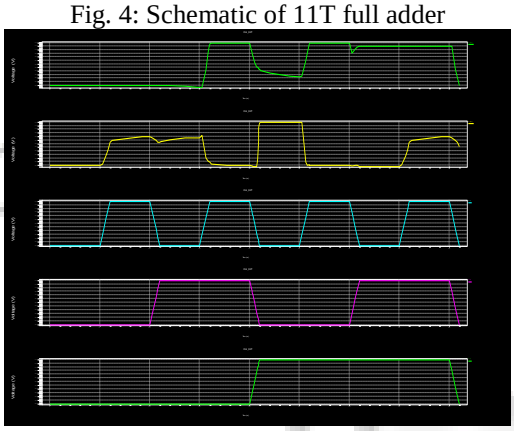

Fig. 5: output waveforms of 11T full adder

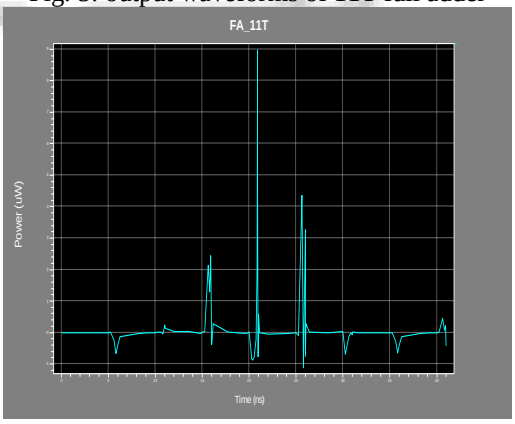


Fig. 6: Leakage power of 11t full adder

## III. RESEARCH WORK

### *A. Specifications of 8t Full Adder*

| | |
|---|---|
| Process Technology | 65nm |
| $V_{dd}$ | 1.2V |
| Average power | 0.0033 µW |
| Delay | $3.5*10^{-10}$ s |
| Leakage power | 3.2 nW |

Table. 1. Specifications of 8T full adder

### *B. IMPLEMENTATION AND SIMULATION OF 8T FULL ADDER*

The schematic of 8T full adder on tanner tool with 65 nm process technology is shown in figure 19. It contains PMOS and NMOS and three vpulse is added in it and one vdc supply is connected to the port of inverter in this we take 1.2V voltage supply and we can take pulse width , rise time and fall time of vpulse in different ratio.

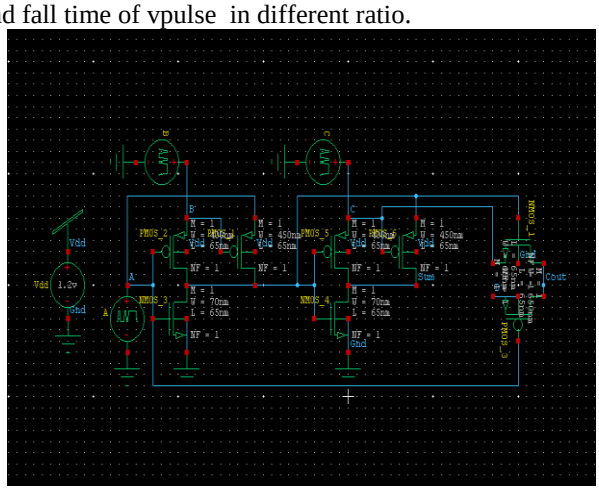

Fig. 10: Schematic of 8T full adder

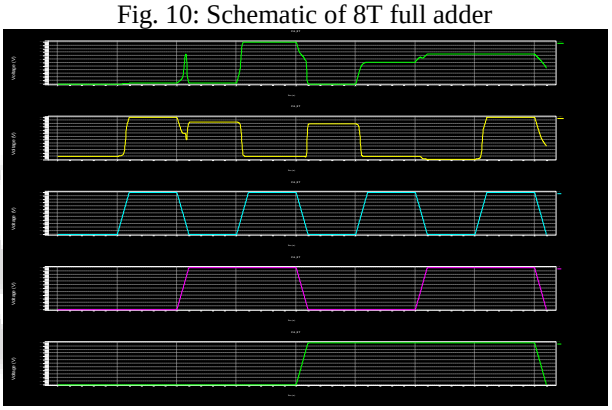

Fig. 11: Output waveforms of 8T full adder

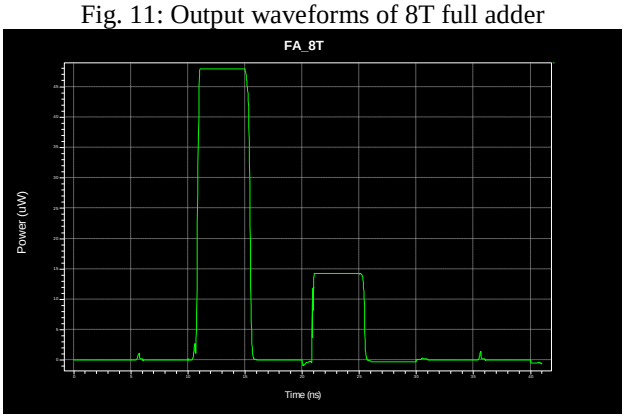


Fig.12: Leakage Power of 8T full adder

## IV. RESULTS AND ANALYSIS

### *A. Comparison Of powers of different full adders*

| Full Adder | 8T | 10T | 11T | 16T |
|---|---|---|---|---|
| Average Power | 0.0033 µW | 0.228 µW | 0.172 µW | 0.0297 µW |

Table. 2. Comparison of powers of different full adders

The leakage power of full adder is given by the following formula: P leakage power = I leakage power * Vdd

| Full Adder | 8T | 10T | 11T | 16T |
|---|---|---|---|---|
| Leakage power | 3.2 nW | 5.1nW | 8nW | 11nW |

Table 3. Comparison of leakage power

*B. Comparison of Delay of Full Adder*

| Full Adder | 8T | 10T | 11T | 16T |
|---|---|---|---|---|
| Delay | $3.5*10^{-10s}$ | $4*10^{-10s}$ | $4.6*10^{-10s}$ | $2.004*10^{-8s}$ |

Table 4. Comparison of delay of full adder

*C. Comparison of Power-Delay Product of Full Adder*

| Full Adder | 8T | 10T | 11T | 16T |
|---|---|---|---|---|
| Power*Delay | $1.15*10^{-18}$ | $9.12*10^{-17}$ | $7.91*10^{-17}$ | $5.95*10^{-16}$ |

Table 5. Comparison of power-delay product of full adder

## V. Conclusion

From the above 16T, 11T, 10T and 8T 1-bit full adder we have concluded that full adder implemented from 8T using GDI(Gate Diffusion Input) technique consumes less average power and delay in comparison with the 16T,11T and 10T and it also has low leakage power consumption and less circuit complexity which provides higher computational speed and lower power consumption .Most of the VLSI applications, such as digital signal processing, image processing, video processing and microprocessors, extensively use arithmetic operations. Binary addition is considered as the most crucial part of the arithmetic unit because all other arithmetic operations usually involve addition. That's why, building low-power, high performance adder cells are of great interest and any modifications made to the full adder would affect the system as a whole. In DSP applications, proposed technique will reduce the delay of the circuit as latency and throughput are the two major constraints from delay perspective.

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