Study of a 3-bit CMOS flash ADC utilizing Threshold Inverter Quantization technique

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Abstract---This paper presents a 3-bit ADC which is considered as the most essential part of a system-on-chip device as it minimizes the gap between analog and digital world. In digital circuits low power and low operating voltage are given first priority as the channel length of the MOSFET shrinks below 0.25 sub-micron values. In this paper a high speed, low power and low voltage CMOS flash ADC for SoC applications is proposed. The proposed ADC utilizes the Threshold Inverter Quantization (TIQ) technique that uses two cascaded CMOS inverters as a comparator. The TIQ technique proposed here has been developed for better implementation in SoC applications using flash ADC.

I. Introduction

Signal processing is very important in many of the system on-a-chip applications. With the advancement in technology, digital signal processing has gained significant importance in the field of telecommunication, biomedical, control systems and so on. This has necessitated the need for design of high precision data converters thereby attracting immense research in this field. Analog to digital converters (ADCs) is a mixed signal device that converts analog signals which are real world signals to digital signals for processing the information. In the recent years, the need to design a low voltage, low power, high speed and wide bandwidth analog-to-digital converter has increased tremendously. Therefore the focus of this research is to design efficient low voltage ADCs that operate at high speed.

Feature size of transistor is now approaching 100 nanometer in semiconductor technology and very soon it will be less than 100 nanometer. And because of this trend of technology there are some challenges in the circuit designing of analog-digital mixed signal devices. To manufacture a system on chip there must be a mixed signal circuitry integrated on a single chip with memory and logic circuits. And this whole system of mixed signal circuitry along with memory & logic circuits must operates at fast speed otherwise it could become a major bottleneck to the whole system. Since the ADC is one of the IC in the mixed signal family, it has to follow this complete system on chip trend. Further this chapter will introduce the challenges in the ADC designing & some solid state technologies for complete system on chip.

II. Overview Of ADC Architecture

There are several different types of ADCs available, depending on the type of application. They are usually classified into three main categories depending on their speed of operation. The three types of ADCs are low speed /serial ADC, medium speed ADC and high speed ADC. Typically the serial ADCs have very high resolution which means they support high accuracy whereas high speed ADCs operate at very high frequencies but have relatively low resolution .These ADC's are used in different applications - from mobile communication devices to measure equipment, according to the characteristics of ADCs. Since the performance – sampling rate, resolution, and power consumption - of an ADC is basically determined by its architecture, one single ADC type cannot cover all applications. For instance, flash (parallel) ADCs can be used in high speed and low resolution applications. Because of its parallel architecture, all conversions are done in one cycle with many comparators. On the other hand, a successive approximation ADC can be used in low-speed and high-resolution applications since the conversions are done in many cycles with only one comparator. Therefore, it is important to properly choose an ADC for each application. Among the variety of ADC architectures, there are four most popular ADC architectures presently used. These are as follows:

A. *Flash:* The flash ADC operates at very high speed with lower resolution. It is also called a parallel ADC due to its parallel operation.

B. *Pipelined:* The pipelined ADC can operate at a high speed, but it is slower than the flash. It covers a wide range of applications because of its flexible resolution and speed.

C. *Successive Approximation Register (SAR):* The SAR ADC is suitable for low power and medium-to-high resolution applications with medium speed.

D. *Sigma-Delta (ΣΔ):* The ΣΔ ADCs are used for high resolution and low speed applications.

Conversion rate	Resolution	ADC Architecture
Slow	>14bits	Integrating Oversampling
Medium	>10bits	Successive approximation
Fast	>6bits	Flash Pipeline Folding and Interpolating

Table. 1: Classification of ADC architecture

III. TIQ Flash ADC

The proposed flash ADC characterizes the threshold inverter quantization technique for achieving high speed and low power by using standard CMOS cell technology. Figure 2 shows the block diagram of Threshold inverter quantization based ADC. The name of the technique is based on the logic of using two cascading inverters as voltage comparators. By using this technique there will be no need of voltage comparator, which compare the input voltage with the reference voltage. Thus there is no need of resistor ladder circuit used in a conventional flash ADC. The gain boosters used in the block diagram below are used to make sharper

thresholds for comparator outputs and provides a full digital output voltage swing. The outputs of the comparator i.e. thermometer code are converted into binary codes through '01' generator and an encoder as shown in the figure 2 below.

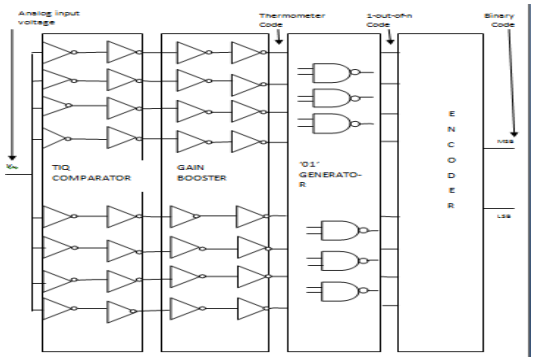

Fig. 1: Block diagram of a TIQ based flash ADC

IV. Proposed Work

In our work we are designing a low power analog to digital converter which operates at low voltage. The implementation is carried out on Tanner EDA tool. The process technology used is 90nm. The main proposed research work is to reduce the power consumption and reduction of operating voltage.

V. Conclusion

An uncomplicated and fast flash ADC has been implemented which consists of two cascaded inverters as comparators, called as threshold inverter quantization (TIQ) technique. The TIQ flash ADC provides higher data sampling rate and operates at low voltage and also low power consumption. It is highly suitable for the complete SoC integration using the standard CMOS digital process. As a future work we will improve the design in many ways. For low power design it is required to generate the MOSFET width automatically so that the power consumption of TIQ comparator block can be more reduced. Moreover the time interleaved conception can be used to increase speed.

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