High Speed and Low Power Carry Select Adder Design by using 180 nm Technology

Dhaivat Vasoya[1] Punit Lathiya[2]
[1]VLSI Student [2]Assistant Professor
[1, 2]School of engineering, R K University, Rajkot, India

Abstract—Speed and Power are the most important parameters of any integrated circuits. Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. This paper presents performance analysis of Carry Select Adders. The comparative analysis is done on the basis of performance parameters like Speed, Power and Power Delay product in 180nm CMOS technology. We present a modified carry select adder design. Proposed carry select adders shows better performance in speed and power consumption than regular CSA.

Key words: Carry Select Adder (CSA), Ripple Carry Adder (RCA), Full-adder, Mux, Speed, Low Power, and Power Delay Product.

I. INTRODUCTION

For every microprocessor and Arithmetic Logical Unit (ALU) data path is the very important core part of that. It is also the crucial component as far as die area, power dissipation, and especially speed of operation is concern. By using data-path and addressing units result into arithmetic units like comparators, adders, and multipliers. Most basic operation performed arithmetic operation is the binary addition. Apart from the addition, adders are also used in often complex operations like multiplication and division. But also used in operations like incrimination and magnitude comparison based on binary addition. Therefore, binary addition is the most important part of any arithmetic operation. That's why the adder circuit is very important part in almost all integrated Processor.

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. The Processor speed highly depends on the speed of the adder circuit that the processor contains.

Any 1-bit adder circuit contains 2 output bits. One is the sum bit and the other is carry bit. That means N^{th} bit has to wait until N-1 carry bits are generated. That means in N-bit adder circuit carry will propagate from first bit to last bit. This is the simplest form of adder circuit, but delay will increase. Different adder circuits are used to minimize this delay. Various different circuits have been proposed to improve the performance in terms of speed and power i.e. ripple carry adder, carry look ahead adder, carry save adder, conditional sum adder, conditional carry adder etc.

The carry-select adder generally consists of two ripple carry adders and a multiplexer. To perform the addition of with a proposed carry-select adder is done with one RCA adder and one Excess-1 converter.

A. SPEED AND POWER OPTIMIZATION

The design of high-speed and low-power VLSI architectures needs efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and power consumption. Power defines as number of Joules consumed over a certain amount of time whereas energy define as total number of Joules consumed by a circuit. As far as CMOS design is concern the power-delay product is frequently used to assess the merits of system designs. In a sense, this can be shown as power × delay = (energy/delay) × delay = energy, which implies delay is irrelevant [5].

There are three major sources of power consumption in digital CMOS circuits, which are summarized in the following equation.

$$P_{total} = P_{switching} + P_{short\text{-}circuit} + P_{leakage}$$
$$= (\alpha_{0\rightarrow1} \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd})$$

The first term represents the switching component of power, where *C* is the load capacitance, *fclk* is the clock frequency and $\alpha 0\rightarrow 1$ is the node transition activity factor. The second term is due to the direct path short circuit currents, *Isc*, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, *Ileakage*, which can arise from substrate injection and sub threshold effects, is primarily determined by fabrication technology considerations. However, while supply voltage reduction is the most effective way to reduce the power consumption, such a reduction require new design methods for low-voltage and low power integrated circuits. Since an average of 15-20% of the total power is dissipated in glitching, low power can also be achieved by reducing the glitches of the circuit [2].

The rest of the paper is organized as follows. In section 2, is a brief introduction about regular carry select adder using two ripples carry adder (RCA), Section 3 is about a proposed carry select adder using RCA and Excess-1 converter. Section 4 is to about introduce excess-1 converter instead of RCA. Section 5 provides the results obtained. Section 6 concludes the paper.

II. CARRY SELECT ADDER

The carry-ripple adder is composed of many cascaded single-bit full-adders. The circuit architecture is simple and area-efficient. However, the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready. In the carry select adder, N bits adder is divided into M parts. Each part of adder is composed two carry ripple adders with Cin=0 and Cin=1, respectively. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal. The carry-select adder can compute faster because

the current adder stage does not need to wait the previous stage's carry-out signal. The summation result is ready before the carry-in signal arrives; therefore, we can get the correct computation result by only waiting for one multiplexer delay in each single bit adder. [2]

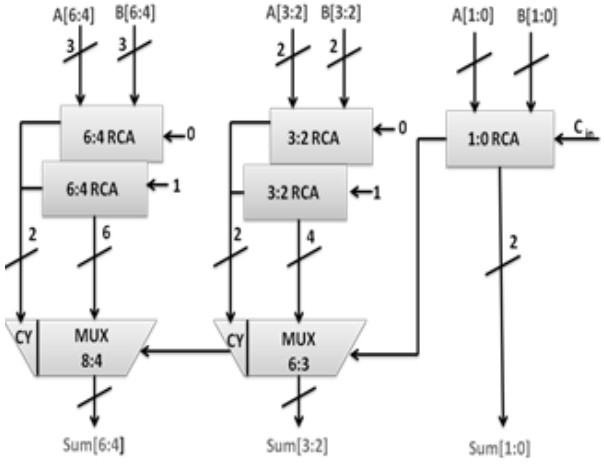

Fig. 1: Block diagram of conventional CSA

In carry select adder Sum and carry are calculated or generated in advance by assuming input carry as 1 and 0 prior to input carry from the previous stage come. Whenever actual carry input comes from previous stage, the actual performed results of sum and carry are selected using a multiplexer. In MSB adders one is RCA adder by considering carry input as zero for performing addition while other one is Excess-1 converter which performs the operation by assuming the result of RCA adder as an input to the Excess-1 converter. This operation will be seems like RCA adder by assuming carry input with one. Ultimately which result into increase the area utilization and speed at the same time reduced the number of hardware component which result into low power consumption. The carry generated from the last stage i.e. least significant bit stage is used to select proper output of carry and sum.

III. PROPOSED CARRY SELECT ADDER

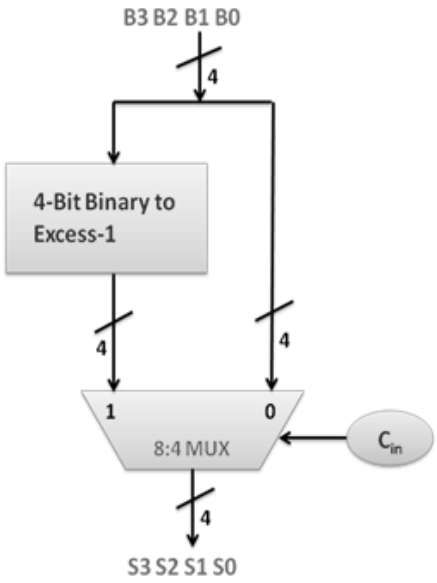

Fig. 2: Block diagram proposed adder cell

In proposed carry select adder RCA by assuming carry one is replaced with the converter. Proposed CSA perform the operation by assuming carry with zero while Excess-1 converter perform the operation by considering data which is result of RCA with carry zero as a input of Excess-1 converter. Output of Excess-1 converter will remain same as outputs of RCA with carry one. Once the calculation is performed with RCA and Excess-1 converter, appropriate sum and carry will be selected by the multiplexer.

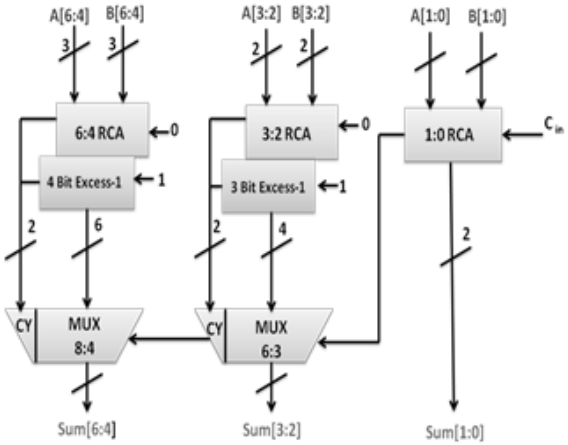

Fig. 3: Block diagram of proposed CSA

IV. EXCESS-1 CONVERTER

Excess-1 converter is used instead of ripple carry adder which perform the addition by assuming with carry one. In order to increase the speed and reduce power consumption converter is used. Because Excess-1 has less number of gates compare to RCA. So ultimately reduce the delay and power consumption.

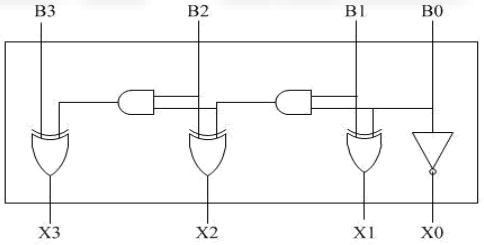

Fig. 4: Excess-1 converter

The Boolean expressions of 4-bit Excess-1can are defined as below.

X0=~B0
X1=B0^B1
X2=B2 ^ (B0&B1)
X3=B3 ^ (B0&B1&B2

Binary	Excess-1
0000	0001
0001	0010
|	|
|	|
1111	0000

Table. 1: Truth Table of Converter

V. SIMULATION RESULTS

We have simulations performed using NGSPICE in a 180 nanometer (*nm*) standard CMOS technology for 28 T 1-bit full adder at room temperature; with supply voltage of 2v.

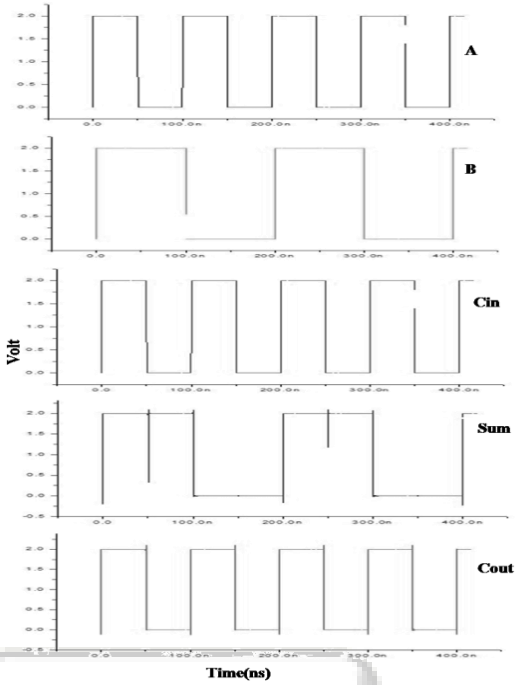

Fig. 5: Simulation result proposed CSA

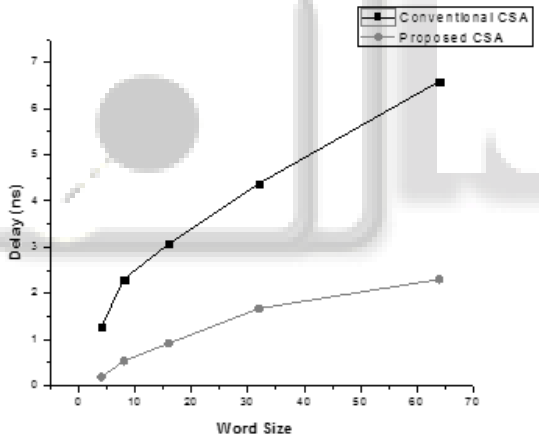

Fig. 6: Simulation result Delay curves.

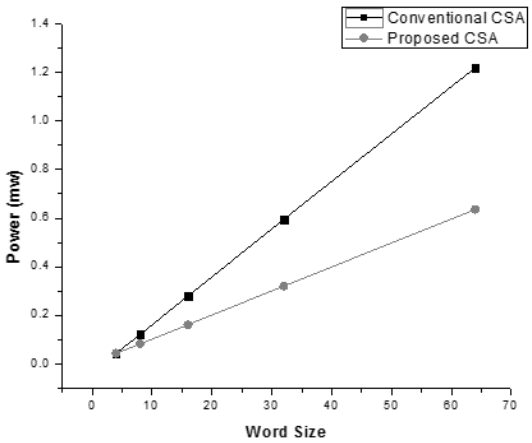

Fig. 6: Simulation result Power delay product (PDP) curves

Word Size	Delay (ns)		Power (mw)	
	Conventional CSA	Proposed CSA	Conventional CSA	Proposed CSA
4	1.27	0.18	0.0428	0.0428
8	2.305	0.535	0.121	0.0825
16	3.075	0.915	0.279	0.161
32	4.38	1.67	0.595	0.320
64	6.59	1.98	1.22	0.636

Table. 2: DELAY AND POWER ANALYSIS

Word Size	Power Delay Product	
	Conventional CSA	Proposed CSA
4	0.054×10^{-12}	0.0077×10^{-12}
8	0.278×10^{-12}	0.0441×10^{-12}
16	0.857×10^{-12}	0.147×10^{-12}
32	2.60×10^{-12}	0.534×10^{-12}
64	8.039×10^{-12}	1.25×10^{-12}

Table. 3: PDP COMPARISION

VI. CONCLUSION

In this paper, high speed and low power carry select adder is proposed. The proposed adder shows better performance in delay as compared to conventional CMOS adder. By using converter instead of parallel RCA, we can overcome the RCA adder cells in the conventional carry select adder. In this using converter circuit which is used to reduce power, area and delay. It requires less area and it is faster than conventional CSA and ripple carry adder. We can find out that the delay, power and PDP of our proposed design is smaller as compare with the conventional carry select adder. The simulation results show that the delay and power consumption increases with increasing word size of adder. Therefore, proposed CSA architecture is high speed, low area, and low power, simple and efficient for VLSI hardware implementation. In future, the design can be further extend for higher number of bits.

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