Low Power Pipeline ADC for Wireless Communication Applications

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Abstract--- Wireless communication applications have driven the development of high-resolution A/D converters (ADCs) with high sample rates, good AC performance and IF sampling capability to enable wider cellular coverage, more carriers, and to simplify the system design. Further, many of the modern IF-sampling super-heterodyne communication systems require the ADC to sample input signals up to 300 MHz in order to reduce receiver complexity and lower overall system cost. Pipeline ADCs are the architecture of choice for ADCs used in such wireless communication systems, and are ideally suited for realizing 12–16 bits of resolution, 70–80 dB of SNR, while dissipating less than 1Wof power

Keywords: Pipeline ADC, Analog to Digital Converter (ADC)

I. INTRODUCTION

Pipeline analog-to-digital (A/D) conversion technique has been used to realized high-speed high-resolution Nyquist-rate analog-to-digital converters (ADCs). The performances of a pipelined ADC, such as resolution, sampling rate, and power consumption, are mainly determined by its internal multiplying digital-to-analog converters (MDACs). A MDAC is usually a switched-capacitor circuit comprising an opamp, analog switches, and capacitors. Thus, the specifications of the opamps, such as dc gain, speed, and power consumption, are crucial [1], [2].

At the same time wireless communication standards, like the Universal Mobile Telecommunication System (UMTS), Wireless Local Area Network (WLAN), Wireless Local Loop (WLL) or Local Multipoint Distribution Services (LMDS), are evolving towards higher data rates, thus allowing more services to be provided. These characteristics are also evolving to the base station side, where the design is still mostly performance oriented. High data rates imply wide bandwidths, while a continuously growing complexity of the modulation schemes and the desire for more flexible receivers push the boundary between analog and digital signal processing closer to the antenna, thus aiming for a software defined radio. These two trends set the specifications of the analog-to-digital converter (ADC) in a radio receiver, the ultimate goal being a receiver with an A/D converter directly sampling signals from the radio frequency (RF), depicted in Fig. 1

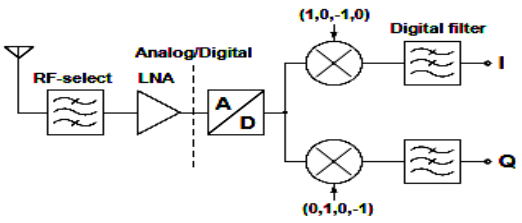

Fig. 1: Direct conversion of the RF signal.

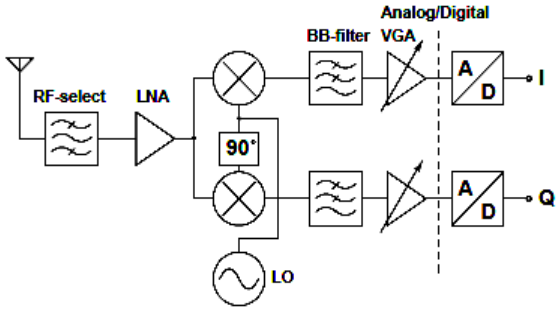

Fig. 2: Direct conversion architecture.

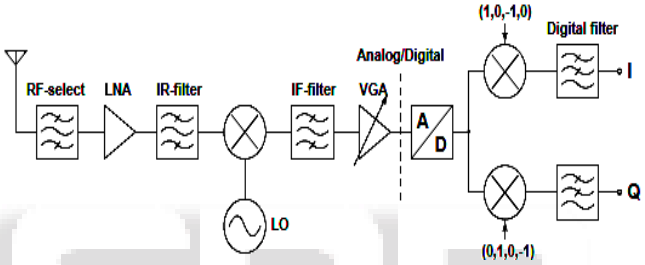

Fig. 3: Super heterodyne architecture employing IF sampling.

To attain higher levels of integration, two realistic receiver architectures are widely developed: the direct conversion receiver, shown in Fig. 2 and the super heterodyne receiver where the analog-to-digital boundary is at the intermediate frequency (IF), shown in Fig. 3. The specifications of the A/D converters differ considerably from each other in these two architectures. In the direct conversion receivers, analog channel selection filtering and variable gain amplifiers relax the dynamic range requirement, and thus the resolution, of the ADCs. The desired channel is also around zero frequency, which indicates a small sampling linearity requirement and low sample rate. In the receivers, where even several signal bands are digitized directly from the intermediate frequency, a very high linearity and sample rate are required in addition to high resolution, giving a large dynamic range. As the first architecture is almost solely used on the mobile side, the power dissipation is an important design constraint, while the second architecture is applied in base stations, making the overall performance essential. Depending on the receiver architecture, analog filtering and gain control range, for A/D converters of such receivers a resolution of 6-14 bits and a sample rate between 10 and 300 MS/s are required. Furthermore, the A/D converter can be integrated with either analog or digital parts of a receiver, which dictate the technology of the ADC. The leading technology of the former domain is the BiCMOS, while the pure CMOS technology, which out performs in the digital domain, is spreading to the analog side as well [4]. The most promising wide-band A/D converter architecture, covering a wide

resolution and sample rate range, that can be applied in radio receivers with a high integration level is the pipelined topology, in which several low-resolution stages operating concurrently on different samples are cascaded. Other possible architectures are the two-step flash, sub-ranging, and folding and interpolating ADC topologies. Pipeline A/D converters can operate with supply voltages below 1 V, have potential for low power, are easily calibrated to obtain a higher resolution, and can be fabricated with CMOS, BiCMOS or bipolar processes. In single-chip direct conversion receivers, power dissipation and area minimization are the most essential design constraints. The mixed-signal processing issues are especially challenging the A/D converter design: very sensitive analog blocks, like, for example, the low-noise amplifier (LNA), must not be disturbed by the digital rail-to-rail signals. Coexistence of several communication systems requires multi-mode receivers, in which ADCs with variable resolution and sample rate are needed. In a multi-carrier wide-band IF-sampling super heterodyne receiver, the linearity and jitter of the sampling across the signal band, together with a large dynamic range, are required. Specific techniques, like, for example, bootstrapping, have to be applied in the sampling switches to attain high linearity when digitizing the signal directly from the IF of several hundreds of mega hertz. To achieve higher sample rates, parallelism can be introduced to a pipeline A/D converter. Mismatches in the parallel processing of analog signals create unwanted side bands that have to be avoided or compensated. Furthermore, some kind of calibration has to be employed to achieve a resolution greater than 10-12 bits, a limitation set by the accuracy of the integrated circuit (IC) processes, with a pipeline ADC. The calibration should be to as small an excess in the area and power as possible and it should have a minimal effect on the normal operation**.** Pipelined ADCs are used in a variety of applications such as sensors, mobile systems, CCD imaging, digital video, PDA, digital receivers, fast Ethernet, etc.

II. ADC FUNDAMENTALS & ARCHITECTURE

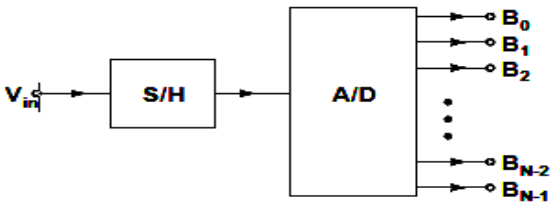

Fig. 4: General block diagram of an A/D converter.

An analog-to-digital converter quantizes an analog signal into a digital code at discrete time points. According to the sampling theorem, the input signal band is limited to half of the sampling frequency to avoid aliasing with the sample rate repeated spectra. The so-called Nyquist rate A/D converters can digitize frequencies up to this frequency and thus have great potential for wide-band wireless communication applications. [3]

A. Ideal A/D Converter

An analog-to-digital converter performs the quantization of analog signals into a number of amplitude-discrete levels at discrete time points. A basic block diagram of an A/D converter is shown in fig. 4. A sample-and-hold (S/H) amplifier is added to the input to sample the analog input and to hold the signal information at the sampled value during the time needed for the conversion into a digital number. The analog input value V_{in} is converted into an N-bit digital value using the equation,

$$(V_{in}/R_{ref}) = D_{out} + e_q = \sum_{m=0}^{N-1} Bm * (2^m) + e_q \quad (2.1)$$

In the equation, R_{ref} represents a reference value, which may be a reference voltage, current or charge. B_{N-1} is the most significant bit (MSB) and B_0 is the least significant bit (LSB) of the converter. The quantization error e_q represents the difference between the analog input signal V_{in} divided by R_{ref} and the quantized digital signal D_{out} when a finite number of quantization levels is used. Eq. 2.1 can be partly rewritten as,

$$D_{out} = \sum_{m=0}^{N-1} Bm * (2^m) \quad (2.2)$$

The sampling operation of analog signals introduces a repetition of input signal spectra at the sampling frequency and multiples of the sampling frequency. To avoid aliasing of the spectra, the input bandwidth must be limited to not more than half the sampling frequency (Nyquist criterion) [5], [6].

B. A/D Converter Specifications

It is essential to understand analog-to-digital converter specifications to get an insight into the design criteria for converters. The DC-specifications for the static linearity are widely known. Dynamic specifications of A/D converters give a better insight into the applicability of a converter in a telecommunications system, where linearity and spectral purity are essential.

1) Static Specifications

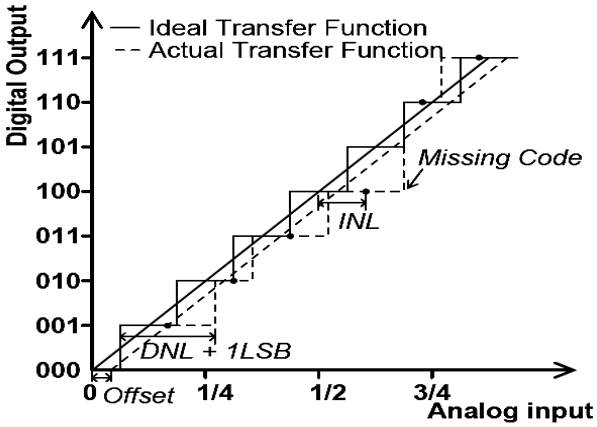

Fig. 5: Transfer function of a 3-bit A/D converter.

The most important measures of static or DC-linearity of A/D converters are integral nonlinearity (INL) and differential nonlinearity (DNL). These properties actually indicate the accuracy of a converter and include the errors of quantization, nonlinearities, short term drift, offset and noise. The definitions of static linearity of A/D converters are indicated in the transfer curve of a converter. An example of a transfer curve of a 3-bit A/D converter can be seen in Fig. 2.2. An ideal N-bit analog-to-digital converter converts a continuous, analog input signal into a time discrete, quantized digital word. If the input signal amplitude scale is from zero to the full-scale voltage VFS the ideal step corresponding to the least significant bit of a converter is VLSB,

$$V_{LSB} = (V_{FS} / 2^N) \quad (2.3)$$

Integral nonlinearity (INL), sometimes called relative accuracy, is defined as the deviation of the output code of a converter from the straight line drawn through zero and full-scale excluding a possible zero offset. The nonlinearity should not deviate more than ±1/2 LSB of the straight line drawn. This INL boundary implies a monotonic behavior of the converter. Monotonicity of an analog-to-digital converter means that no missing codes can occur. Differential nonlinearity (DNL) error gives the difference between two adjacent analog signal values compared to the step size of a converter generated by transitions between adjacent pairs of digital code numbers over the whole range of the converter. The DNL of ADC output *Di* can be written as,

$$DNL\ (D_i) = [V_{in}\ (D_i) - V_{in}(D_{i-1}) - V_{LSB}]/(V_{LSB}) \quad (2.4)$$

Where Di and $D_{(i-1)}$ are two adjacent digital output codes. There is a direct connection between the INL and DNL. The INL for output Dm can be obtained by integrating the DNL until code m.

$$INL(D_m) = \sum_{i=1}^{m} DNL\ (Di) \quad (2.5)$$

DNL and INL are determined with a high-frequency input signal using the code density test (CDT) [7].

2) Dynamic Specifications

a) Signal-to-Noise Ratio

The quantization process introduces an irreversible error, which sets the limit for the dynamic range of an A/D converter. Assuming that the quantization error of an ADC is evenly distributed, the power of the generated noise is given by,

$$e_q^2 = (V_{LSB}^2/12) \quad (2.6)$$

Where V_{LSB} is the quantization step. If a single-tone sine wave signal with a maximum amplitude is adopted for a converter with a large number of bits (N≥5), the signal rms power is given by,

$$S_p = (V_{FS}^2/4.2) \quad (2.7)$$

Substituting Eq. 2.3 into Eq. 2.6 the signal-to-noise ratio (SNR) for a single-tone sinusoidal signal can be obtained to be,

$$SNR = 2^N * \sqrt{(3/2)} = (6.02*N + 1.76)\ Db \quad (2.8)$$

Eq. 2.8 indicates that each additional bit, *N*, gives an enhancement of 6.02 dB to the SNR. If oversampling is used, which means that the sample rate f_S is much larger than the signal bandwidth *fsig*, the quantization noise is averaged over a larger bandwidth and the signal-to-noise ratio becomes larger, written as

$$SNR = 2^N * \sqrt{(3/2)} * \sqrt{(OSR)} = (6.02*N + 1.76 + 10 * \log (OSR))\ dB \quad (2.9)$$

Where the oversampling ratio OSR is given by,

$$OSR = (f_S/(2*f_{sig})) \quad (2.10)$$

b) Total Harmonic Distortion

Any nonlinearity in an A/D converter creates harmonic distortion. In differential implementations, the even order distortion components are ideally canceled. However, the cancellation is not perfect if any mismatch or asymmetry is present. The total harmonic distortion (THD) describes the degradation of the signal-to-distortion ratio caused by the harmonic distortion. By definition, it can be expressed as an absolute value with,

$$thd=(\sqrt{\sum_{j=2}^{NH+1}(V^2)(j * (fsig))}\ )/V(f_{sig}) \quad (2.11)$$

Where *NH* is the number of harmonics to be considered, *V*(*fsig*) and *V*(*j fsig*) is the amplitude of the fundamental and the *jth* harmonic, respectively.

c) Signal-to-Noise and Distortion Ratio

A more realistic figure of merit for an ADC is the signal-to-noise and distortion ratio (SNDR), which is the ratio of the signal energy to the total error energy including all spurs and harmonics. SNDR is determined by employing the sine-fit test, in which a sinusoidal signal is fitted to a measured data and the errors between the ideal and real signal are integrated to get the total power of noise and distortion. If all tones and spurs other than the harmonic distortion are considered as noise, the signal-to-noise ratio can be obtained from the SNDR by subtracting the total harmonic distortion from it which is given as,

$$snr_{real} = snr - thd \quad (2.12)$$

Where *sndr* and *thd* are given in absolute values.

d) Spurious Free Dynamic Range

In wireless telecommunication applications, large oversampling ratios are often used and the spectral purity of the A/D converter is important. For such situations, a proper specification is the ratio between the powers of the signal component and the largest spurious component within a certain frequency band, called spurious free dynamic range (SFDR). The SFDR is usually expressed in dBc as,

$$SFDR(dBc) = 10*\log((V^2(f_{sig}))/(V^2(f_{spur}))) \quad (2.13)$$

$V(f_{sig})$ is the rms value of the fundamental and V(fspur) the rms value of the largest spurious. For an exact SFDR definition, the power level of the fundamental signal relative to the full-scale must also be given. Normally the limiting factor of the SFDR in ADCs is harmonic distortion. In most situations, the SFDR should be larger than the signal-to-noise ratio of the converter.

e) Effective Number of Bits

The effective resolution bandwidth (ERB) is defined as the maximum analog frequency for which the signal-to-noise ratio of the system is decreased by 3 dB or 1/2 LSB with respect to the theoretical value. The number of bits obtained in this way for a single-tone full-scale sinusoidal test signal is called the effective number of bits (ENOB).

$$ENOB = (SNDR - 1.76dB) / 6.02dB \quad (2.14)$$

III. THE PIPELINED ADC

The pipelined ADC has become increasingly popular because of its lower power consumption and reasonably fast conversion rate as compared to other ADC architectures of similar resolution and speed performance. The pipelined ADC accomplishes this by a major reduction in the amount of circuitry required in the conversion process. For example,

a flash ADC requires $2^N - 1$ comparators; the sub-ranging ADC requires $(2^M - 1) + (2^{N-M} - 1)$ comparators; while an N-bit pipelined ADC implemented using the 1.5-bit per stage architecture requires only two comparators per stage and N-1 stages. Therefore, for an 8-bit implementation, the flash requires 255 comparators, the sub-ranging 30 (for M = N – M = 4), and the pipeline only 14. Not only does this pipelined architecture require fewer comparators, another benefit is that the accuracy requirement of the comparators is greatly reduced as well. In addition to the reduced comparator requirements, the gain-bandwidth required for the residue amplifier is also reduced. For example, in a sub-ranging architecture with a 4-bit coarse ADC the residue amplifier has a gain of 16 where each stage of a 1.5-bit per stage pipelined ADC only requires a gain of 2. This allows the pipelined ADC to work at higher conversion rates in a given process. However, it should be noted that due to the pipeline process in which a sampled signal is worked on serially by each stage of the pipeline, a significant input to output latency is introduced where the digital output may require several clock cycles to appear after the given analog input has been sampled by the converter. This latency may not be tolerable by all potential applications, such as in some control systems in which the control loop requires nearly instantaneous feedback [8].

A. One Bit per Stage Pipelined ADC

Depending on the desired characteristics of the ADC being designed, the pipelined ADC can be realized using several different architectures. In most cases a particular ENOB, conversion rate, power requirement, conversion latency, or combination thereof, must be met by the design. For example, if latency is of significant concern, then the pipeline may be designed with fewer stages with more bits-per-stage, at the expense of conversion rate. However, if a high conversion rate is desired, the 1-bit and 1.5-bit per stage pipelines are the fastest due to the lowest possible gain requirement per stage (gain = 2). Depending on which design characteristics are most important, an optimum number of bits per stage is established, and the accuracy required for each stage is determined. One of the most simplistic pipelined implementations, and one that is often used to demonstrate the pipelined ADC concept, is the 1-bit per stage pipelined ADC. An 8-bit version would require eight, 1-bit stages.

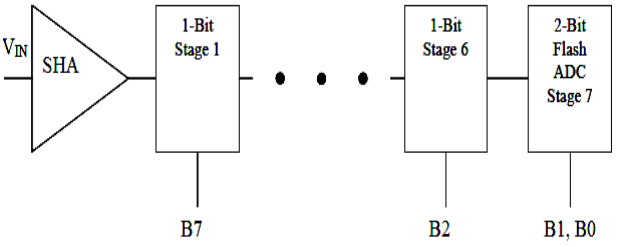

Fig. 6: The 1-Bit per Stage Pipelined ADC.

In the 1-bit per stage design shown in Fig. 6, as is the case with all pipelined ADCs, the first stage must be the most accurate as any error in this stage will ripple through out all subsequent stages. In an N-bit implementation, the first stage at a very minimum must be at least N-bit accurate (accurate to within ½-LSB where 1-LSB = $V_{FS}/2^N$); the second stage (N-1)-bit accurate, and so on. In the case in which the design objective is to minimize power consumption, subsequent stages of the pipeline may be scaled down to be only as accurate as they need to be. However, if the design objective is to minimize noise or design time, then subsequent stages may not be scaled, or not scaled as aggressively.

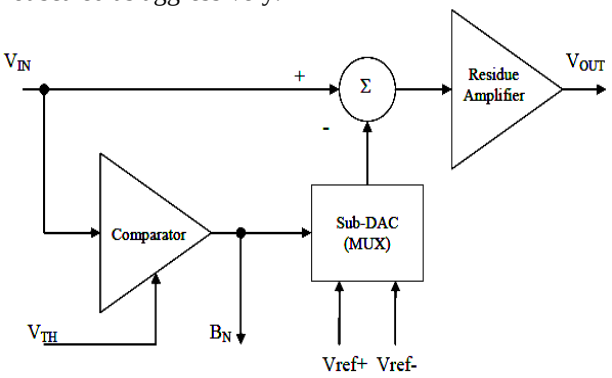

Fig. 7: Residue Stage Architecture for the 1-Bit per Stage Pipelined ADC.

An analog input signal, V_{IN}, is applied to a comparator referenced with a threshold voltage, V_{TH}. In this case, V_{IN} can be any value between Vref- and Vref+, while V_{TH} is 0 Volts. B_N is the resultant digital output bit for the stage. The 1-bit stage transfer characteristics are given in Table 1.

Condition	B_N	V_{OUT}
VIN < = 0	0 (Low State)	VOUT = 2 * VIN + Vref
VIN > 0	1 (High State)	VOUT = 2 * VIN + Vref

Table. 1: 1-Bit Stage Transfer Function.

The 1-bit per stage residue plot is shown graphically in Fig. below, with the voltages normalized to VREF.

The drawback of the 1-bit per stage architecture as described is that there is no way to correct for any significant comparator offset. That is to say, the comparator, without an error correction mechanism, must be at least as accurate as the entire stage. As a result, the design of the comparator becomes a significant challenge, especially in higher resolution applications. Comparator offsets can result in an over-range condition as shown in the normalized residue plot of fig. , resulting in distortion. This over-range condition is amplified by the subsequent stages in the pipeline.

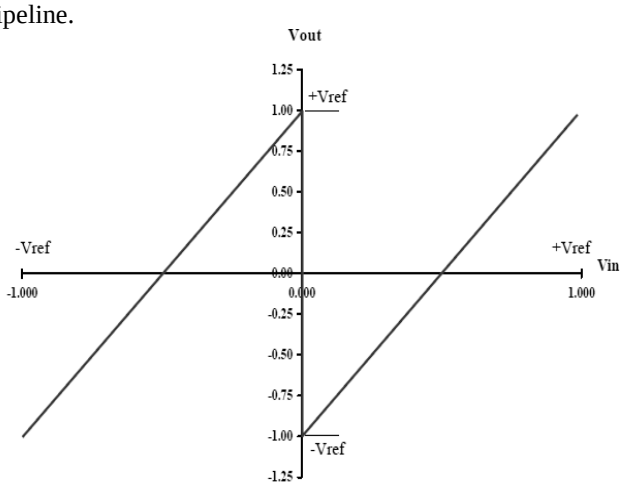

Fig. 8: 1-Bit per Stage Residue Plot (Normalized to VREF).

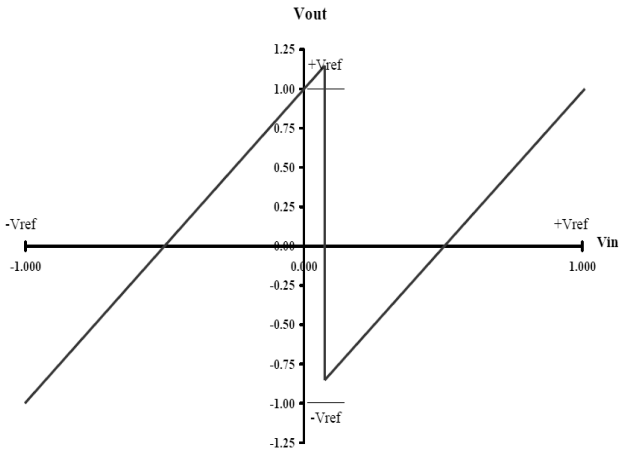

Fig. 9 : 1-Bit per Stage Normalized Residue Plot with Comparator Offset Effect.

IV. CONCLUSION

There are many different types of ADC architectures to consider when meeting a design specification; and that even within the family of pipelined ADCs, available die area, power, speed, accuracy, and resolution all play a role in the decision process when selecting a particular type of pipelined ADC. Capacitor mismatch is one of the major problems in the high resolution ADC design.

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