Power Reduction in the VLSI Architecture of FM0 and Manchester Encoding

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Abstract— Power is a major problem faced by all electronic and electrical circuits designed in these days. The main objective of this work is to combine the VLSI architecture of FM0 and Manchester encoding so that it reduces the power used, by reducing the number of components used and improves the performance of the FM0 and Manchester encoding. These results are observed using spice. The power consumed is 0.72 mw for Manchester encoding. The power consumption is 0.14 mw for FM0 encoding. The FM0 and Manchester encoding is used widely in dedicated short range communication. Signal reliability could be achieved in dedicated short range communications by adopting FM0 and Manchester encoding. The transportation system in these days relies upon dedicated short range communication (DSRC). Many countries around the world depend on DSRC standards. Europe, Japan is the major countries which rely upon dedicated short range communication.

Key words: DSRC, VLSI architecture, FM0 Encoding

I. INTRODUCTION

The protocol which plays a vital role in these days is a dedicated short-range communication. The dedicated short range communication could be widely classified into two categories namely automobile-to-roadside and automobile to automobile. Blind-spot, intersection warning, inter cars distance and collision alarm is the major safety issues in automobile-to-automobile for which DSRC enables the message sending facility.

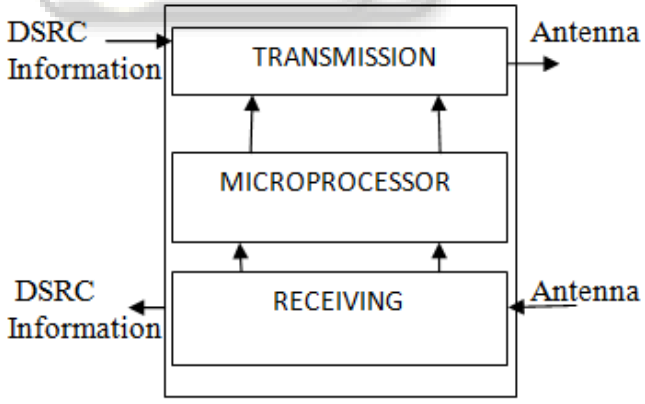


Fig. 1: Architecture of DSRC transceiver

The automobile to-roadside focuses transportation service, such as the payment for parking-service and gas-refueling. The purpose of FM0 and Manchester encoding is to provide dc-balance for transmitted signal. Thus, the DSRC system plays an important role in modern automobile industry.

A. Review of VLSI Architecture for the Encoding Technique:

The literature [3] proposes VLSI architecture of encoder for communication purpose. The CMOS inverter acts as a switch in order to construct Manchester encoder. It is implemented by the 0.35-µm CMOS technology and it operates in the frequency range of up to 1GHZ. The literature [4] replaces the switch in [5] by the nMOS device. The technology used in this 90-nm CMOS, technology and the frequency of operation is given by up to a maximum of 4GHZ. The literature [6] proposes a fully reused VLSI architecture of Manchester encodings for many applications like radio frequency identification (RFID). The technology used here is 0.35-µm CMOS technology and the maximum frequency used for operation is 190MHZ. The literature [7] also deals with the study of Manchester encoding for the purpose of ultra high frequency (UHF) RFID emulator. The finite state machine of Manchester coding plays a vital role in the construction of hardware architecture of Manchester encoding. It is realised using the field- programmable gate array (FPGA) prototyping system. The maximum operation frequency is about 200MHZ.

B. Features of This Paper:

The similarity oriented logic simplification consists of two methods namely balance logic sharing and area-compact retiming. The relocation of hardware components is performed using the area re-compact retiming. The separate architectures are combined together by the use of balance logic sharing.

C. Organization:

The remainder of this paper is organized as follows. Section II describes the principles of FM0 and Manchester codes. Section III gives the procedure for the construction of hardware architecture of FM0 and Manchester encoding. Section IV focuses on results and discussion. Finally Section v focuses on conclusion.

II. PRINCIPLES OF FM0 AND MANCHESTER CODE

The inputs are CLK and X. The coding principles of FM0 and Manchester coding are as follows.

A. FM0 Encoding:

As seen in Fig. 2, for each input X, the FM0 consists of two parts namely first half cycle, A and the other one for second half cycle of CLK, B. The coding principle of FM0 is listed as follows

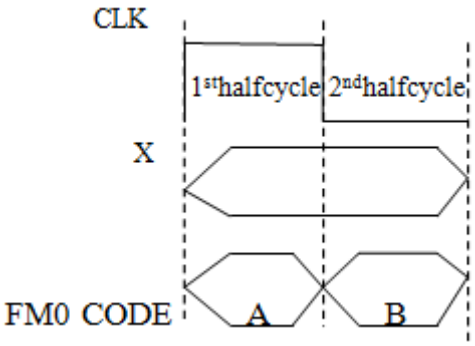


Fig. 2: Codeword structure of FM0

1) Whenever the given input is logic 1, transition occurs for every full cycle.
2) Whenever the given input is logic 0, transition occurs for every half cycle.

B. Operation of Manchester Encoding:

The XOR operation of logical input X and CLK gives the Manchester encoding realization.

$$X \oplus CLK.$$

III. CONSTRUCTION OF HARDWARE ARCHITECTURE OF FM0 AND MANCHESTER ENCODING

Before the construction of FM0 and Manchester encoding architecture using similarity oriented logic simplification is performed, we first study about the ways to construct the VLSI architecture of FM0 and Manchester encoding without using similarity oriented logic simplification. The Manchester encoding is constructed by performing the XOR operation between the CLK and X. The steps used to design the VLSI architecture of FM0 and Manchester encoding is as follows.

A. Illustration of FM0 and Manchester Encoding Waveform:

For Example

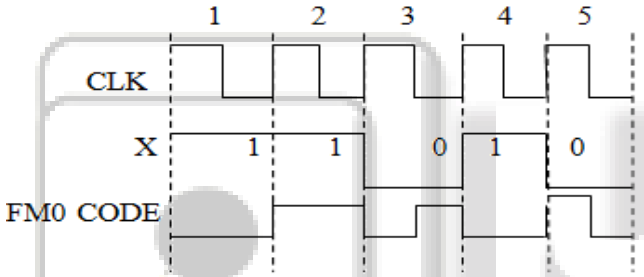


Fig. 3: Illustration of FM0 coding example.

B. Manchester Encoding Is Realized With A XOR Operation For CLK And X. The Expression Is As Follows X ⊕ CLK:

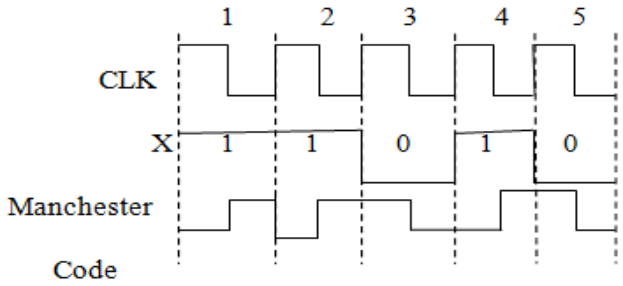


Fig. 4: Illustration of MANCHESTER coding example

C. State Machine Representation of the FM0 and Manchester Encoding Waveforms:

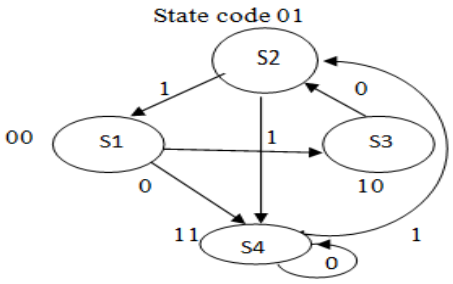


Fig. 5: Illustration of FSM for FM0.

D. Transition Table Representation of State Machine:

PREVIOUS STATE		CURRENT STATE	
		A (t)	
A (t-1)	B (t-1)	X=0	X=1
0	0	0	1
0	1	1	0
1	0	0	1
1	1	1	0

Table 3: Transition Table of FM0

K-map representation of the transition table.

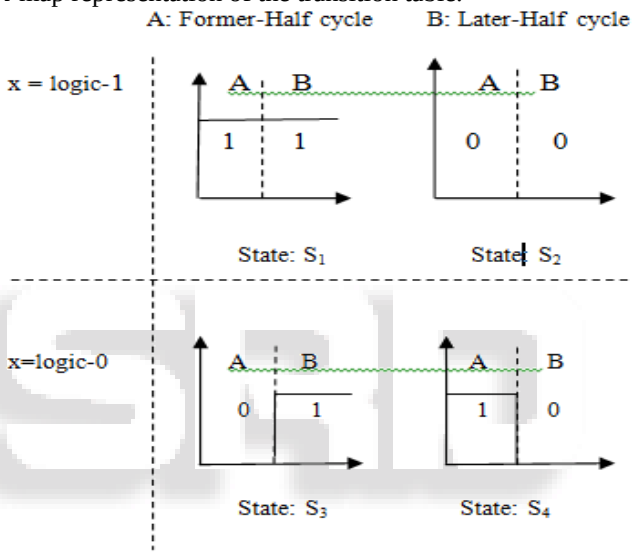


Fig. 6: Illustration of k-map for FSM of FM0.

E. With This K-Map, the Boolean Expression Is Found:

$$A(t) = \overline{B(t-1)}$$

$$B(t) = X \oplus B(t-1)$$

F. With The Help of Boolean Expression the Hardware Architecture Of FM0 And Manchester Encoding Is Drawn:

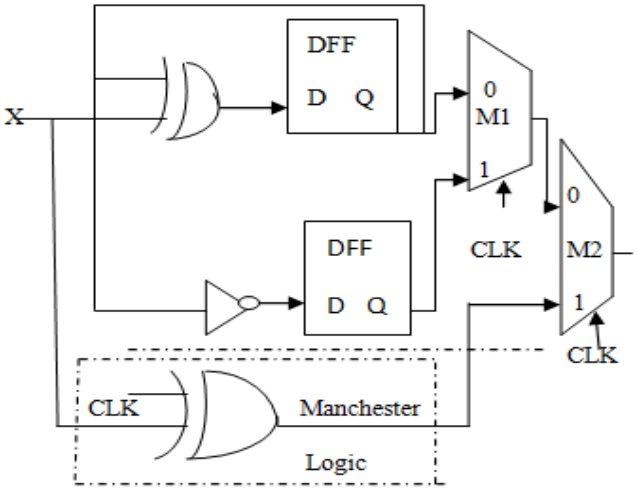


Fig. 7: Hardware architecture of FM0 and Manchester code

G. Area Re-Compact Timing Is Used Relocate The Hardware Components To Redraw The Hardware Architecture In Order To Reduce The Power Consumption:

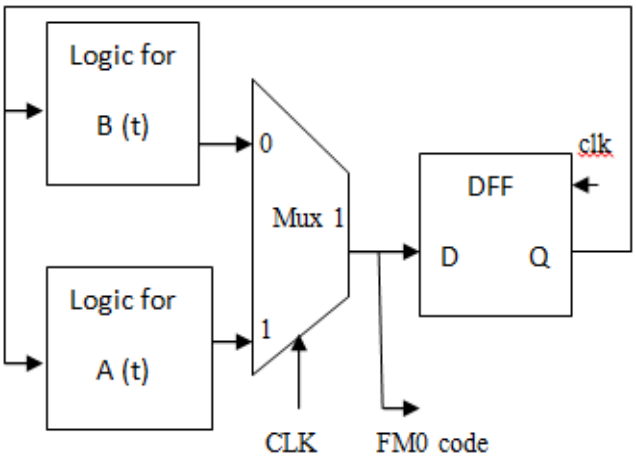
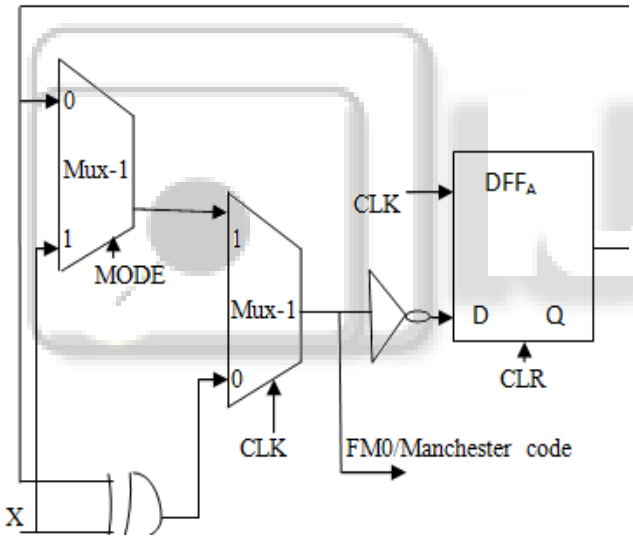


Fig. 8: Area re-compact timing applied for FM0 code.

Hence the hardware architecture of FM0 and Manchester encoding could be redrawn using area re-compact timing. Due to which the power minimization is achieved with the reduced number of components and delay. The hardware architecture of FM0 and Manchester encoding using similarity oriented logic simplification is drawn as follow



FM0 CODE: Mode = 0 and CLR = 1
Manchester code: Mode =1 and CLR=0

Fig. 9: VLSI architecture of FM0 and Manchester encoding using similarity oriented logic simplification

IV. Experiment Results and Discussion

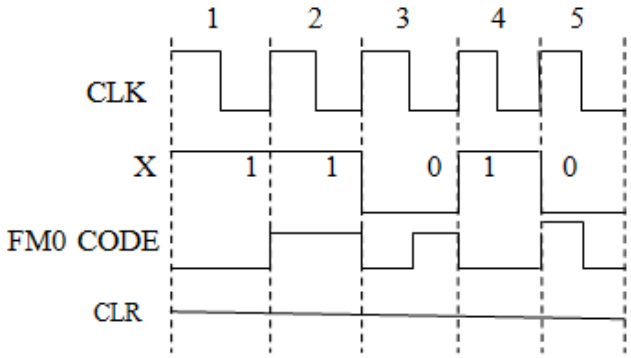


Fig. 10: Waveform of FM0 and Manchester encoding.

The architecture of FM0 and Manchester encoding is combined together using similarity oriented logic simplification. Hence it reduces the number of components, area, power, and delay of the FM0 and Manchester encoding architecture. Hence cost used for power consumption also reduces with reduced consumption of power. Spice tool is used to view the results.

The results could also be viewed using the FPGA . The number of modes used here is two namely FM0 and Manchester encodings. FPGA consists of LUTs, Flop-Flip. The performance evaluation is also classified into two categories namely FM0 and Manchester encodings. The waveform verification could be done as shown in Fig. 10.For FM0 encoding, [6] uses FPGA software for finite state machine. The FM0 dissipates more power than Manchester encoding. Both FM0 and Manchester encoding operate at the same frequency. During the switching activity FM0 utilises all the components of DFF but Manchester encoding has lower switching activity and hence utilises only fewer components. As a result Manchester encoding dissipates less power compared to FM0 encoding. The coding procedure of Manchester encoding is less complex when compared to FM0 encoding.

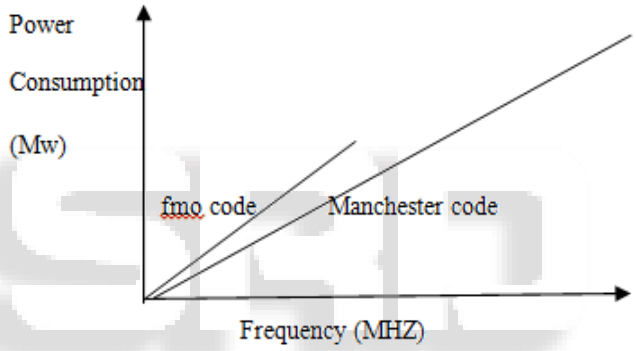


Fig. 11: Power profiling of proposed work for FM0 and Manchester encodings.

Hence from the Fig.11.It is clearly understood that Manchester encoding consumes much power compared to FM0 encoding.

V. Conclusion

In this paper, the VLSI architecture of FM0 and MANCHESTER encoding is implemented using similarity oriented logic simplification technique. The power, delay, and number of transistor used is determined. Minimization of area, number of transistor is achieved by the reduced power utilization. My future work is to design the VLSI architecture of FM0 and MANCHESTER encoding using various logic such as transmission gate logic, pass transistor logic, dynamic logic and compare the power utilization. Spice tool plays a vital role in observing the results obtained. This paper not only reduces the power consumption but also exhibits good performance compared to the existing works. This paper could also be realised using TSMC 0.18-µm 1P6M CMOS technology with good efficiency and performance.

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