Novel Low Power and High Performance 6T Full Adder Design and its Application using Deep Submicron Technology

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Abstract— Full adder is one of the major components in the design of many sophisticated hardware design. In this paper the 6T full adder has been designed using a new efficient design with less number of transistors. A 2 transistor EX-NOR has been proposed with the help of two NMOS (negative Metal Oxide Semiconductor) transistors. By using this 2T (EX-NOR and 2:1 MUX) A gate the size of the full adder has been reduced to a large extent which can be implemented with only 6 transistors and applied this design in 4:2 compressor. The proposed full adder has a significant improvement in silicon area and power delay product when compared to the previous 8T full adder design. Further the proposed full adder requires a less area to perform a required logic operation. Further, the proposed full adder and 4:2 compressor has less power dissipation which makes it suitable for many of the low power applications and because of less area requirement the proposed design can be used in more of the portable applications also. It uses 45nm and 90nm in deep submicron technology.

Key words: Full Adder, Ex-Nor, Nano meter, Deep Submicron Technology, 4:2 comparator

I. INTRODUCTION

This paper proposed a 10 transistor per bit compared with other low gate count of full adder using pass transistor. And they used 4 transistor based Xor in the system, has reduced pdp 50% [1]. In this model a one bit full adder is proposed for a low power and high performances generated using the 8T full adder technique and 12 state of the 1-bit full adder are simulated with HISPICE using 0.18µm CMOS technology the power and delay are minimized by reducing the transistor size. the power delay and power producing delay were reduced using this technique [2] .In this system a one bit full adder 12T is design, a full adder design consisting of 6 identical multiplexer and 12 transistor, it has very low short circuit current and consume less power than the CMOS adder this adder using software HISPICE simulation [3]. A full adder designed with multiple pass transistor logic is proposed. They used multiple numbers of half adder & full adder and its designed using generic process design kit 45nm technology and they are simulated using cadence software. A 25% of power saving and improved a switching speed of transistor [4] In this paper 6T full adder based and compare a performances 45nm ,90nm,120nm in submicron technology is proposed and then 6T used to design the 4:2 compressor is a application of this system and it's reduced a size of the compressor and improve the performance

II. METHODOLOGY

A full adder is used in many low power applications. The Full adder is implemented using XOR, AND and OR gates has basic function a system. A simple and efficient full adder is designed using the transistors. The number of transistors may vary. The full adder can be designed using 6T transistors, EX-NOR and 2:1 MUX. The number of transistors required to design mux and EX-NOR is reduced to 2T.

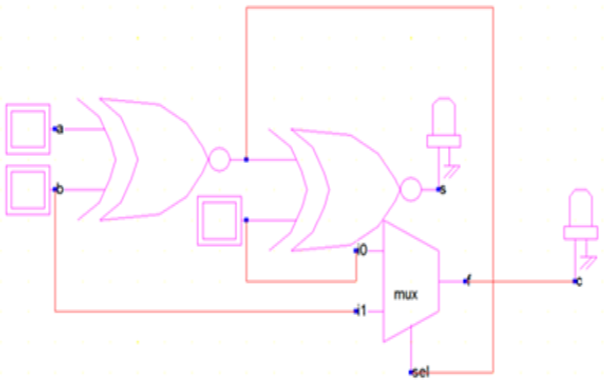

Fig. 1: Circuit for Full Adder Proposed System

A. EX-NOR:

The EX-NOR gate is designed using two transistors only which use two NMOS transistors. The circuit diagram of the EX-NOR is given in fig2.

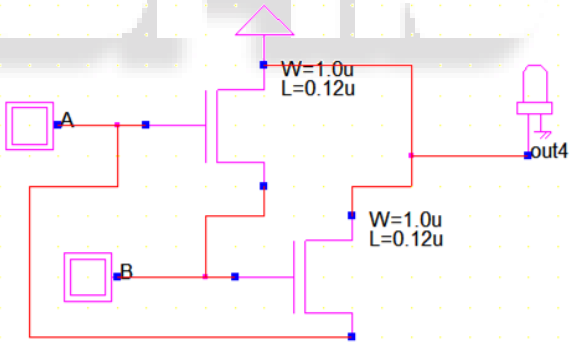

Fig. 2: 2T EX-NOR

The basic operation of the EX-NOR is that when A=B=1, then the transistor output will be high. When A=1andB=0 the transistor output will be low. When A=0, B=1 the output will be low. When A=B=0 the transistor output is high. The truth table of the EX-NOR gate is given in bellow. The use of the2T transistor EX-NOR reduces the size of the full adder and by reducing the size large number of devices can be integrated into a single silicon device to reduce the size and increase the speed of operation.

1) Truth table 1: EX-NOR

A	B	EXNOR
0	0	1
0	1	0
1	0	0
1	1	1

Table 1: EX-NOR

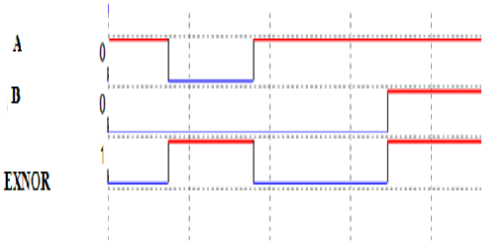

Fig. 3: waveform of 2T EX-NOR

B. 2:1 Mux:

To reduce the size and power dissipation the 2:1MUX is designed with 2Transistor in deep submicron technology. The circuit diagram of the 2:1MUX is given in fig.4

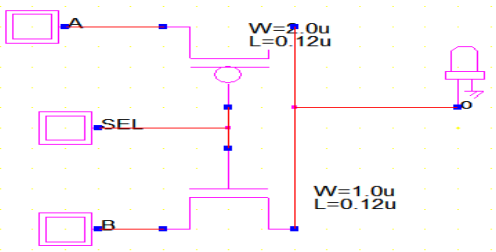

Fig. 4: 2T 2:1 MUX

The 2:1Mux has selection lines which plays an important role in the output. The selection line determines the output. If the selection line is 0 the value of A will be the output. If the selection line is 1 the output depends on the value of B. The Truth table (2) and wave form of 2T 2:1 MUX is given in fig.4

1) Truth table 2: 2:1 MUX

SEL	A	B	OUT
0	0	0	0
	0	1	0
	1	0	1
	1	1	1
1	0	0	0
	0	1	1
	1	0	0
	1	1	1

Table 2: 2:1 MUX

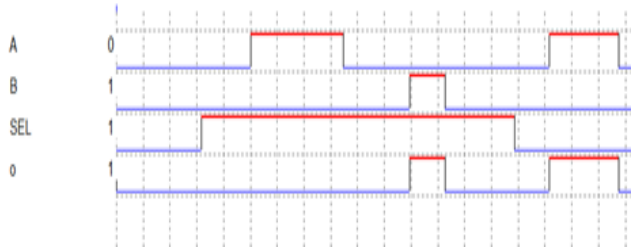

Fig. 5: Wave form 2T 2:1 MUX

C. 6T Full Adder

Full adder is the basic element of many VLSI low power devices and is widely used in arithmetic operations. The full adder has three inputs and two output which are sum and carry. The full adder is designed using PMOS and NMOS transistor in deep submicron technology. There are two EX-NOR, one 2:1MUX are used to design the full adder. The proposed full adder has one PMOS and five NMOS transistors. The circuit diagram of the 6T full adder is given below.

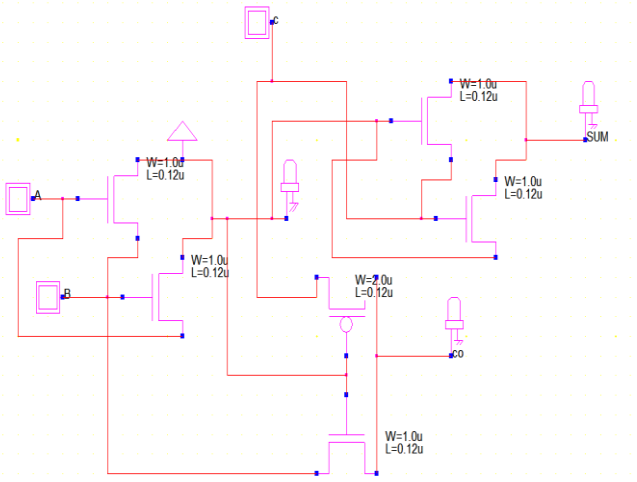

Fig. 6: 6T Full Adder Design

D. 4:2 Compressors:

The 4:2 Compressor are designed using the developed 6T full adder. There are five inputs and three output, and which has one sum and two carry. In this basic 4:2 compressor there are five half adder, 2 OR gate and more transistors are used and it has more power dissipation.

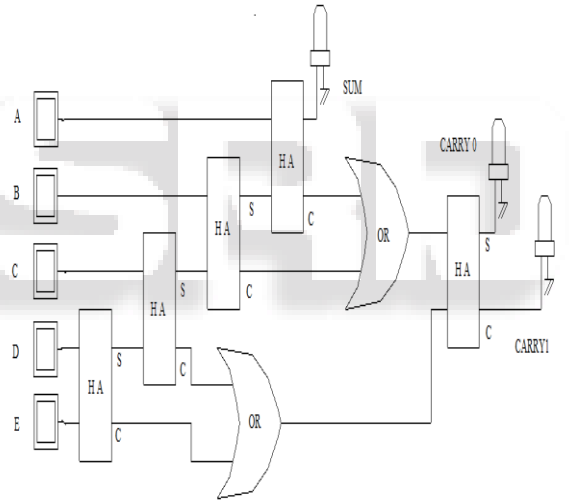

Fig. 7: basic 4:2 Compressor

The 4:2 compressors have two full adder and one half adder and the number of transistor is reduced and power consumption is minimized. The circuit diagram of the 4:2 Compressor is shown in fig7

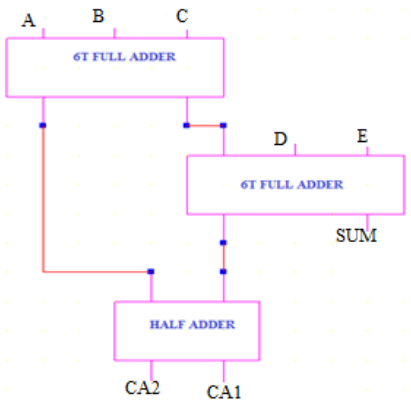

Fig. 8: Proposed 6T Full Adder Based 4:2 Compressor

1) Truth Table.3: 4:2 Compressor

INPUT	OUTPUTS		
NO OF INPUTS HIGH	CARRY 1	CARRY 0	SUM
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

Table 3: 4:2 Compressor

III. RESULT AND DISCUSSION

The EX-NOR and 2:1 MUX is designed using microwind 3.1 and cadence and they are used to design the 6T full adder. The full adder output wave form is given in fig.10. The performance comparison table is given in table.

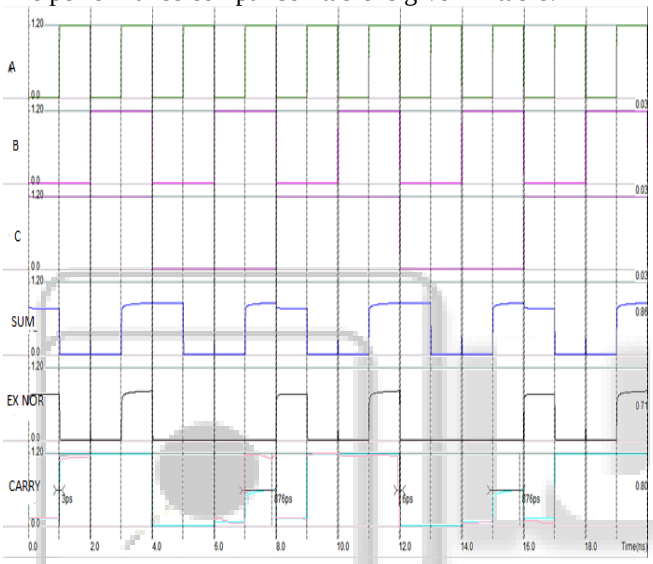

Fig. 9: 6T Full Adder Wave Form

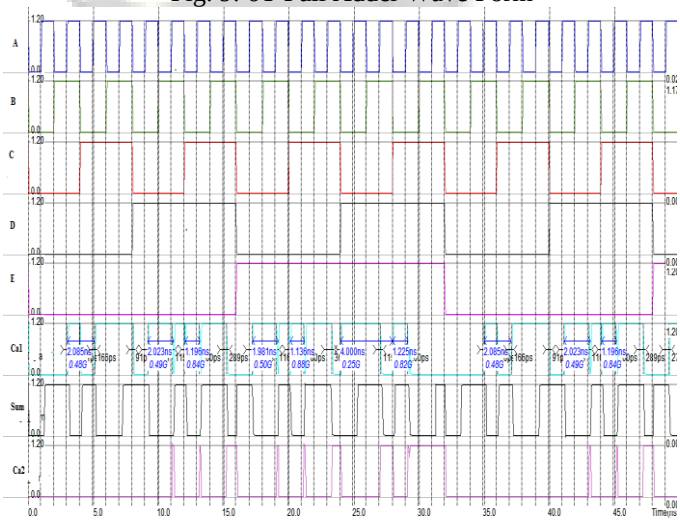

Fig. 10: Wave Form Proposed 6T Full Adder Based 4:2 Compressor

Structure	No. Transistors	Power (µw)	Delay (ns)	PDP (aj)
14T	14	6.4	-	126.54
10T	10	1.83	73.5	83.05
8T	8	1.22	185.9	40
6T	6	0.864	200.124	36

Table 4: 6T Full Adder Performance

IV. CONCLUSION

The 6T transistor is designed using deep submicron technology and the full adder is used to design the 4:2 compressor the output waveforms are obtained. The developed technique has low power dissipation and acquires least area

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