Power and Area Efficient Full Adder Design using High Performance CMOS Technology

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Abstract— This paper presents the realization of full adder designs using Complimentary CMOS Design, Complimentary Pass Transistor Logic Design. The main motive of this paper is to determine the comparative study of power, surface area and complexity of Full adder designs using CMOS Logic Styles. The conventional design consists of 28 transistors and proposed design consists of 10 transistors. Simulations results clearly determine that proposed Full adder Design is better compared to conventional design. Transistor Design with respect to power, delay, Power Delay Product Comparison.

Key words: Full adder, CMOS gates, Transistor logics, Sum, Carry

I. INTRODUCTION

In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers .In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require a more complex adder.

Power and area consumption are two important considerations for VLSI system designer engineers. Our prime motive is to reduce the power and surface area to get less delay that is nothing but the high speed for any design. Adder is one of the fundamental blocks present in arithmetic logic unit (ALU), floating point unit. In present arena we need fast arithmetic computation cells like adder and multipliers in the very large scale integration (VLSI) designs. Moreover, adders are very important components in some other applications such as microprocessor and digital signal processing (DSP) architectures. Digital signal processors and Microprocessors mainly rely on highly efficient implementations of generic floating point units and arithmetic logic units (ALU). So working on adder designs is very helpful for high level applications.

Although substantially increasing design productivity, such tools require the employment of a long chain of automatic synpaper algorithms, from register transfer level (RTL) down to gate level and net list.

A. CMOS Technology:

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication.

CMOS is also sometimes referred to as complementary-symmetrymetal–oxidesemiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor

Material Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond.

"CMOS" refers to both a particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes.[3] As of 2010, CPUs with the best performance per watt each year have been CMOS static logic since 1976. CMOS circuits use a combination of p-type and n-type metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates and other digital circuits found in computers, telecommunications equipment, and signal processing equipment. Although CMOS logic can be implemented with discrete devices (e.g., for instructional purposes in an introductory circuits class), typical commercial CMOS products are integrated circuits composed of millions of transistors of both types on a rectangular piece of silicon of between 10 & 400mm2. These devices are commonly called "chips", although within the industry they are also referred to as "die" (singular) or "dice", or "dies" (plural).

B. CMOS Process Enhancements:

1) Silicon on Insulator:

As the name suggests transistors are fabricated on an insulator (SiO2 or sapphire) Insulating substrate eliminates capacitance between the source/drain and body, higher speed devices and low leakage currents.

2) Transistors:

Multiple threshold voltages and oxide thicknesses Processes offer multiple threshold voltages Low threshold devices: faster, higher leakage. High threshold devices: opposite Thin oxides: provide high ON currents but cannot handle high voltages. dielectrics Transistors need high gate capacitance to channel Thin gates and therefore high gate leakages Thicker gates that leak less can be made with high-k materials e.g. hafnium oxide (k=20), zirconium oxide (k=23), silicon nitride (k=6.5-7.5) Applied using ALD, MOCVD (metallo –organic CVD) or sputtering.

C. Design and Architecture of Full Adder:

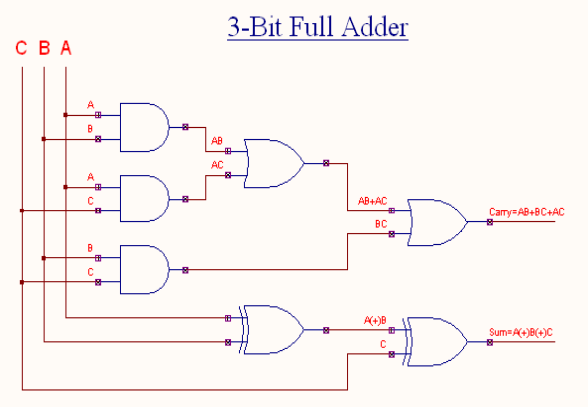

Fig. 1: Full adder design

The ultimate goal of a binary full-adder (BFA) is to implement the following truth table for each bit:

C in	A	B	Sum	C out
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth table adder design

Logically, carry = AB+BC+CA and Sum = C⊕B⊕A, where k is an integer 0 to n for an n-bit adder. Generally, adders of n-bits are created by chaining together n of these 1-bit adder slices.

II. EXISTING SYSTEM DESIGN

A. Simulation for existing system:

Digital schematic is designed using DSCH for full adder using 28 transistors which occupies a lot of surface area and power consumed is also high which can be reduced by reducing number of transistors. The complexity can be decreased by modifying this existing full adder design.

Step 1: Starting with designing of full adder using 28 transistors open the DSCH window. Open the project from file.

Step 2: Choose the project name from the location where schematic design is save or design the circuit using transistors and other components from library.

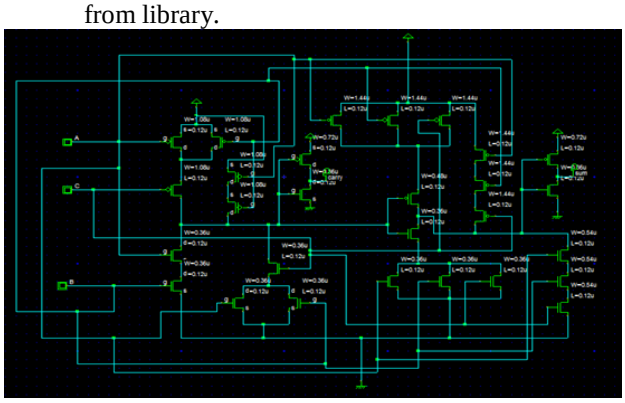

Fig. 2: Circuit Design for Existing System

The twenty eight bit transistor based on regular CMOS structure i.e. pull-up and pull-down network. One of the most significant advantages of this full adder waists high noise margins and thus reliable operation at low voltages. The layout of CMOS gates was also simplified due to the complementary transistor pairs. But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area.

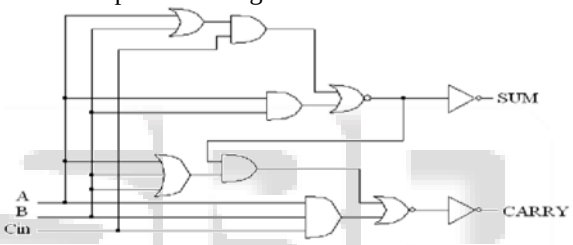

Fig. 3: This is the gate level implementation for explanation of full adder using 28 transistors.

Here implementation of the full adder circuit is designed by taking the logic equations and translate them directly into complementary CMOS circuit in fig. . Some logic manipulations can help to reduce the transistor count. For instance, it is advantageous to share some logic between the sum and carry – generation sub circuits, as long as this does not slow down the carry generation, Which is the most critical part as stated previously. The following is an example of Such as reorganized equation set:

$$CARRY = A.B + B.C_{in} + A.C_{in}$$

$$SUM = A.B.C_{in} + CARRY\ (A + B + C_{in})$$

The equivalence with the original equations is easily verified. The corresponding adder design, using complementary static CMOS, is shown in figure and the gate level implementation is shown in figure . It requires 28 transistors.

The first 12 transistors of the circuit produce the C_{out} and the remaining transistors produce the Sum outputs. Therefore the delay for computing C_{out} is added to the total propagation delay of the Sum output. The structure of this adder circuit is huge and thereby consumes large on-chip area.

Step 3: Simulation is firstly done in DSCH by verifying the truth table of 3 bit full adder. All the combinations are checked for sum and carry on applying inputs at a b and c.

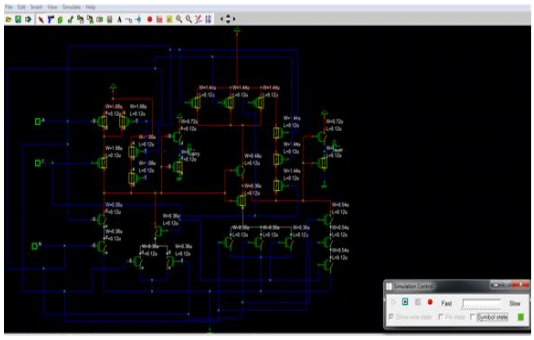

Fig. 4: Simulation Results for sum and carry from DSCH

Step 4: Generate VERILOG File through DSCH for sum and carry. This VERILOG file is further used in MICROWIND for generation of stick diagram which will further analyze the power parameters for design.

Step 5: Open the MICROWIND for layout design, area and power analysis. Here we can directly compile the VERILOG file generated by DSCH design of full adder.

Step 6: Compile VERILOG File in microwind.

VERILOG file once compiled the software will generate a layout for sum and carry logics.

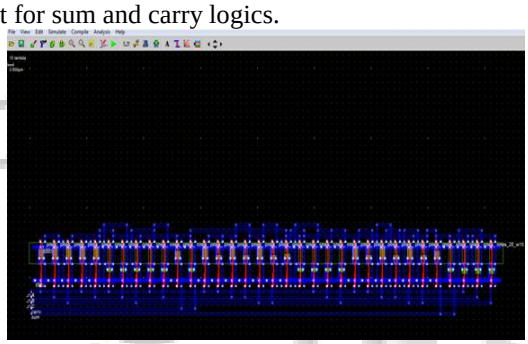

Fig. 5: Layout of full adder in MICROWIND

Step 7: Run Simulation for checking parameters that are surface area and power.

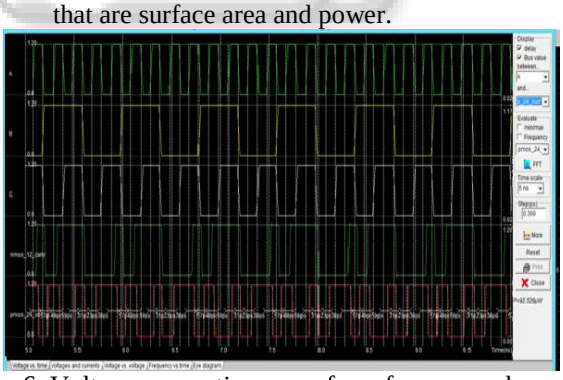

Fig. 6: Voltage versus time waveform for sum and carry logic

III. Results for Full Adder Proposed System

Same steps are followed for proposed system in our paper which will consume less area and low power in practical applications.

Step 1: Starting with designing of full adder using 10 transistors open the DSCH window. Open the project from file.

Step 2: Choose the project name from the location where schematic design is save or design the circuit using transistors and other components from library.

A. Proposed Circuit is designed for sum & carry in DSCH:

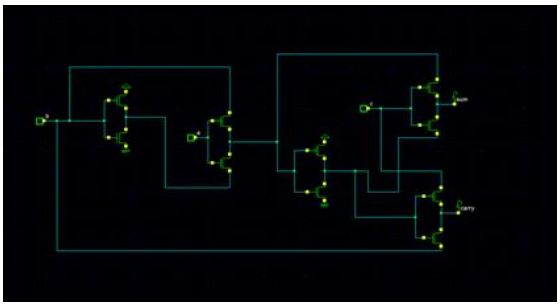

Fig. 7: Circuit design for sum and carry logic of full adder using 10 transistors

In this type of full adder the energy recovering logic reuses charge and therefore consumes less power than other adder. The circuit consists of two XNORs realized by 4 transistors. Sum is generated from the output of the second stage XNOR circuit. The c_{out} is calculated by the use of multiplexing a and cin controlled by (a $\otimes$ b). Let us consider that there is a capacitor at the output node of the first XNOR module. To illustrate static energy recovery let us consider an example where initially a=b=0 and then a changes to 1. When a and b both equals to zero the capacitor is charged by VDD. In the next stage when b reaches a high voltage level keeping a fixed at a low voltage level, the capacitor discharges through a. Some charge is retained in a. Hence when a reaches a high voltage level we do not have to charge it fully. So the energy consumption is low here. It should be noted that the new full adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption. The charge stored at the load capacitance is reapplied to the control gates. There is no combination of having a direct path to ground and the re-usage of the load charge to the control gate makes the energy-recovering full adder an energy efficient design. It uses 10 transistors and does not require any inverter. In non-energy recovery design the charge applied to load capacitance during logic level high is drained to the grounded during the logic level low.

Step 3: Simulation is firstly done in DSCH by verifying the truth table of 3 bit full adder. All the combinations are checked for sum and carry on applying inputs at a b and c.

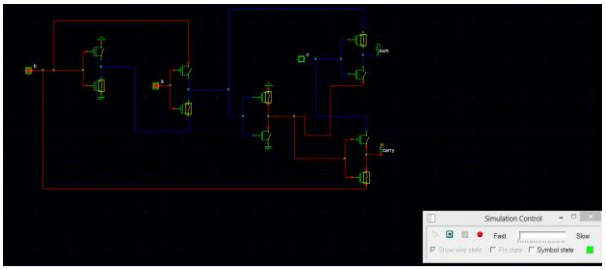

Fig. 8: Simulation Result for Proposed System

Step 4: Generate VERILOG File through DSCH for sum and carry. This VERILOG file is further used in MICROWIND for generation of stick diagram which will further analyze the power parameters for design.

Step 5: Open the MICROWIND for layout design, area and power analysis. Here we can directly compile the VERILOG file generated by DSCH design of full adder.

Step 6: Compile VERILOG File in microwind

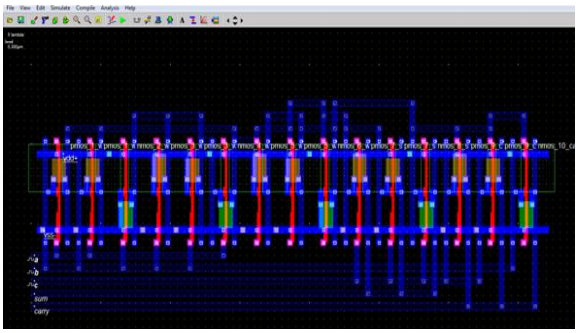

Fig. 9: Layout Design in MICROWIND

Step 7: Run Simulation for checking parameters that are surface area and power.

Simulation Waveforms from MICROWIND are obtained for voltage versus time and verification of full adder working using truth table can be verified.

Fig. 10: Voltage versus time waveform for sum and carry logic

B. Comparison:

System ⇨ parameters ⇩	Existing design	Proposed design
Surface area	396.3µm^2	179.6µm^2
Power consumptions	92.526microW	62.313microW
Number of transistors used	28	10

Table 2: Comparison of both designs

The simulation results and analysis is compared in the table for various parameters and it can be seen that work carried out in this paper is more efficient in terms of surface area and power consumption.

IV. Conclusion and Future Work

In this paper a new design for full adder is proposed which is power efficient and less complex. In conventional design full adder with 28 transistors exists and we have proposed a new design which is consuming less power and it is made up of 10 transistors only. This full adder is designed using DSCH software whose simulation and verification is carried out in MICROWIND. Also it has been shown that reducing the supply voltage is the most direct means of reducing dissipated power and operating CMOS devices is considered to be the most energy-efficient solution for low-performance applications. Hence reduced complexity is achieved by using less number of transistors. Also power is reduced up to 30% in comparison to conventional design.

With the increasing demand for battery-operated portable applications such as cell phones, PDAs and laptop computers, as well as low-intensity applications such as distributed sensor networks, the need for power sensitive design has grown significantly. So, for future work we can further change the design to get minimal power. The rapid growth in semiconductor device industry has led to the development of high performance portable systems with enhanced reliability. In such portable applications, it is extremely important to minimize area and current consumption due to the limited availability of battery power. Therefore area utilization power dissipation becomes an important design issue in VLSI circuits.

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