Survey of Double Tail Comparator for High Speed and Low Voltage Successive Approximation Register

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Abstract— Comparator is one of the main building blocks in most analog-to-digital converters. The double tail comparator is a newly proposed that operates with reduced delay and high speed. The study of various architecture of comparator and analog to digital converters is very important. In This paper, dynamic and double tail comparator are discussed .moreover comparison has been made between architecture of ADCs.

***Key words*:** Double tail comparator, dynamic comparator, successive approximation registers ADC

I. INTRODUCTION

Comparators are important elements in modern mixed signal systems. Speed and resolution are two important features which are required for high speed applications. The comparator compares the voltages that appear at their inputs and outputs a voltage representing the sign of the net difference between them. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +, INP, the input of the comparator is at a greater potential than the -, INN, input, the output of the comparator is a logic 1 and vice versa. Developing new circuit is preferable for low voltage operation, especially if they do not increase the circuit complexity. The structure of double tail dynamic comparator first proposed based on designing a separate input and cross coupled stage. This separation helps in fast operation over a wide common mode and supply voltage range.

This paper is organized as follows. The dynamic comparator is discussed in section II. The newly proposed dynamic comparator is in section III. In section IV, discussed successive approximation register and a summary of various analog-to-digitals converter is given. Finally the conclusions are presented in section V.

II. DYNAMIC COMPARATOR

Some comparators are clocked and only provide an output after the transition of the clock. Clocked comparators are often called Dynamic Comparators. Dynamic comparators are widely used in the design of high-speed ADC's. The speed of clocked comparators can be very high and the power dissipation of clocked comparators can be very low. Most of the A/D converters uses the comparator with high input impedance, rail to rail output swing and no static power consumption. The operation of the conventional dynamic comparator occurs in two phases .i.e., reset phase and comparison phase. During the reset phase when the CLK=0, the transistors M7 and M8 is on where Mtail is off. So the output nodes outn and outp are charged to VDD. During the comparison phase when the CLK=1, the transistors M7 and M8 are off condition and Mtail is on. An output voltage which has been precharged to VDD starts discharging according to the input provided (VINN and VINP). If VINP>VINN, outp discharges faster than outn, hence when outp falls down to VDD-|Vth| before outn, the corresponding pmos transistor M5 will turn on initiating the latch regeneration caused by back to back inverters. Thus outn pulls to VDD and outp discharges to ground. If VINP<VINN, the circuits works vice versa.

The delay of load capacitance is given by

To $=CL|VTHP|/I2$

$=2CL|VTHP|/\boldsymbol{Itail}$ (1.1)

Where

$I2=Itail/2+Iin$

$=Itail/2+gm1,2\ Vin$

For small differential input(V_{in}), I_2 can be approximated to be constant and equal to the half of the tail current.

In order to find the delay of the latched (t_{latch}), it is assumed that a voltage swing of $Vout=V_{DD}/2$. Half of the power supply is considered to be the threshold voltage of the comparator.

$tlatch = CL/gm,eff.\ln(\Delta vout/\Delta vo)$

$= CL/,.\ln(VDD/2/\Delta vo)$ (1.2)

Where $g_{m,eff}$ is the effective trans conductance of the back to back inverters.

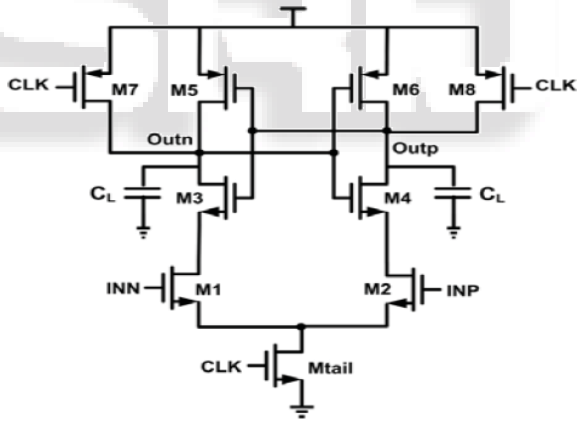

Fig. 1: Schematic Diagram of Dynamic Comparator.

The advantages of the conventional dynamic comparator are high input impedance, rail to rail output swing and no static power consumption. The comparator also suffers from serious disadvantages that stacked transistor consume high supply voltage for proper delay. Also that it consists of only one tail which is the current path Mtail, which defines the current for both differential amplifier and the latch. So it leads to some delay in the passage current from one latch to another latch or from one node to ground.

III. DOUBLE TAIL COMPARATOR

Double tail comparator is designed, where the circuit of a conventional dynamic comparator is modified for low power and fast operation even in small supply voltages. It is based on designing separate input and cross coupled stage. The

double tail comparator architecture is used in low voltage applications because of its better performance in delay reduction. The main idea of the double tail comparator is to increase ΔV0 which will also increase Vfn/fp. So the control transistors Mc1 and Mc2 are added to the first stage in parallel to M3 and M4 but in cross coupled manner.

Figure 2 shows the schematic diagram of double tail comparator. The operation of the double tail comparator occurs in two phase which are reset phase and decision making phase. During reset phase CLK=0, Mtail1 and Mtail2 are in off state, M3 and M4 are in on state which pulls both the nodes fn and fp to VDD. so according to the input suppose Vinp>Vinn, then fn drops faster than fp. As long as fn continues falling, the corresponding pmos control transistor starts to turn on, pulling fp node back to VDD. So another control transistor (Mc2) remains off, allowing fn to be discharged completely. The control transistor Mc1 is on when Mc2 is grounded which results in static power consumption so two more switches(Msw1 and Msw2) are added. During the decision making phase the nodes fn and fp are precharged to VDD and it starts its different discharging. As soon as the comparator detects that one of the fn/fp is discharging faster, control transistor will help to increase the voltage difference. In other words, the operation of the control transistors with the switches emulates the operation of the latches.

Delay of the double tail comparator is low comparator to conventional dynamic comparator. The two major factors that makes the comparator are improvement in the initial output voltage difference(v0) at the initiation of the operation and enhancement in the effective transconductance (gmeff) of the latch.

ΔV0 denotes the initial voltage difference between two latches. It is desirable to have biggerΔV0 results in less regeneration time. The value of output voltage difference is given by

$$\Delta V0 = \Delta V0 = 4Vthn|Vthp| \frac{gmR\ 1{,}2\ gm\ 1{,}2\Delta Vin}{Itail\ 2.Itail\ 1}\exp\left(\frac{Gm\_eff1{,}t0)}{CL,(p)}\right)$$

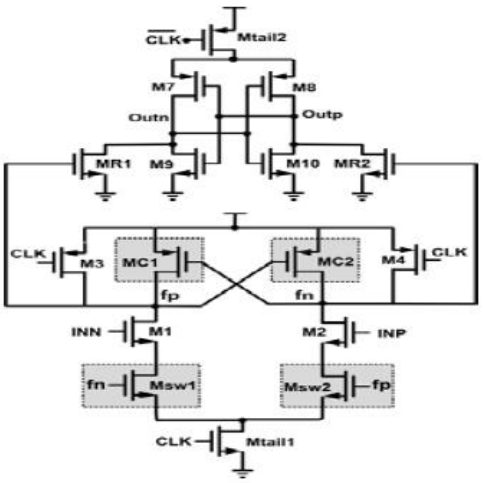

Fig. 2: Schematic Diagram of Double Tail Comparator

IV. ANALOG-TO-DIGITAL CONVERTER

An analog-to-digital converter is an electronic integrated circuit which converts continuous signals to discrete digital numbers. The ADC will translate a continuous analog signal into a series of binary numbers. Each number represents the value of analog signal at the time of conversion.

A. Summary of ADC Architectures

The architecture of ADCs are classified as following

- Flash ADC
- Sigma-delta ADC
- Dual slope converter
- Successive approximation converter

Type	Advantage	Disadvantage
Dual Slope	– Greater noise immunity than other ADC types	– Slow – High precision external components required to achieve accuracy
Flash	– Very Fast	– Needs many parts (255 comparators for 8-bit ADC) – Lower resolution – Expensive – Large power consumption
Successive Appox. Register	– Capable of high speed – Medium accuracy compared to other ADC types – Good tradeoff between speed and cost – High resolution	– Speed limited ~5Msps (medius-fast)
Sigma-Delta	– High resolution	– Slow due to oversampling

Table 1 Classification of Adcs According To Its Performance

B. Successive Approximation Register

A successive approximation ADC is a type of analog to digital converter that converts continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion. The conversion time is maintained constant in SAR type A/D converter, and it is proportional to the number of bits in the digital output, unlike the other converters. The basic principle of this A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value trying one bit at a time, beginning with the MSB. It operates by successively dividing the voltage range by half, as explained in the following steps:

(i) The MSB is initially set to 1 with the remaining three bits 0.The digital equivalent is compared with the unknown analog input voltage.

(ii) If the input voltage is higher than the digital equivalent, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and he second MSB is set to 1.

(iii) Comparison is made as given in step1 to decide whether to retain or reset the second MSB. The third MSB is set to 1 and the operation is repeated down to the

LSB and by this time, the converted digital value is available in SAR.

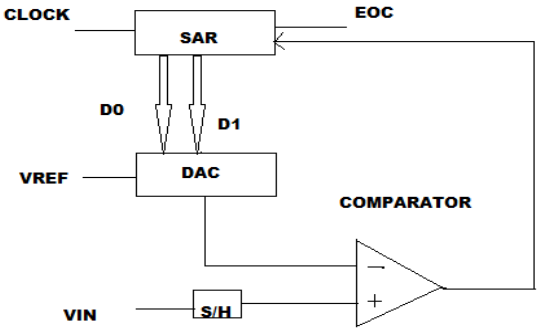

Fig. 3: Successive Approximation Register

V. CONCLUSION

In this paper, dynamic and double tail comparator is studied. A comparison is presented based on various parameters of ADCs. SAR ADC is suitable choice to implement double tail comparator and make its speed faster. So, my objective is to implement double tail comparator for successive approximation register.

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