Design of Vedic Multiplier for DSP Application

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Abstract—this paper presents a delay comparison of two methods multipliers for unsigned data, one uses a simple multiplication and the second one uses a Vedic multiplication. The 64×64 Vedic multiplier module using Urdhva Tiryakbyham Sutra uses 2×2 Vedic multiplier modules. Urdhva tiryakbyham Sutra is most powerful Sutra, giving minimum delay for multiplication of all types of numbers, either small or large. Urdhva Tiryagbhyam– Vedic method for multiplication which strikes a difference in the real process of multiplication itself. It causes parallel generation of intermediate products, removes unwanted multiplication steps with zeroes and scaled to higher bit levels. The paper's main focus is on the speed/delay of the multiplication operation on 64-bit multipliers which are modeled using VHDL, A hardware description language. The 64×64 Vedic multiplier is coded in VHDL, synthesized and simulated using Xilinx ISE 13.4 software. This multiplier is implemented on Spartan 3E FPGA device XC3S1600e-5fg484. The performance evaluation results in terms of speed and delay. The multiplier of Vedic multiplication has shown a less delay over the simple multiplier. The simple multiplier uses time = 153.441ns, while the Vedic multiplier with the uses time = 129.181ns on Spartan 3E device.

*Keywords:*Very high speed integrated circuit (VHSIC); VHSIC hardware description language (VHDL); Vedic Mathematics; Vedic Multiplier; Urdhva –Tiryakbyham (UT).

I. INTRODUCTION

VEDIC mathematics [1] is the ancient Indian method of mathematics which mainly deals with Vedic mathematical formula and their application to various branches of mathematics. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krishna Tirthaji (1884-1960) after his eight years of research on Vedas [1]. According to his research, Vedic mathematics is mainly based on sixteen principles which are termed as Sutras. Formatter will need to create these components, incorporating the applicable criteria that follow.

These Sutras along with their brief meanings are enlisted below alphabetically.

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2) Chalana-Kalanabyham – Differences and Similarities.
3) Ekadhikina Purvena –By one more than the previous one.
4) Ekanyunena Purvena – By one less than the previous one.
5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6) Gunitasamuchyah – The product of the sum is equal to the sum of product.
7) Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10.
8) Paraavartya Yojayet – Transpose and adjust.
9) Puranapuranabyham – By the completion or Non-completion.
10) Sankalana-vyavakalanabhyam – By addition and by subtraction.
11) Shesanyankena Charamena – The remainders by the last digit.
12) Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14) Urdhva-Tiryagbyham – Vertically and crosswise.
15) Vyashtisamanstih – Part and Whole.
16) Yaavadunam – Whatever the extent of its deficiency.

This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

This paper presents simple digital multiplier architecture based on the ancient Vedic mathematics Sutra (formula) called Urdhva Tiryakbyham (Vertically and Cross wise) Sutra is used.In this paper we conclude that Vedic multiplier is faster than the simple multiplier.

II. URDHVA TIRYAKBHYAM SUTRA

Urdhva Tiryakbyham (Vertical & Crosswise) algorithm can be generalized for n x n bit number. This Multiplier has the advantage that has the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed [5]. Since in this multiplier the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Therefore the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. By adopting the Vedic multiplier, structure. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent this power of multiplier. It can easily be increased by increasing the input and output data bus widths since it has a quite a regular problems to avoid catastrophic device failures. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While at higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures.

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A. Steps involved for multiplication using Vedic mathematics

The following is the example of Vedic multiplier for three digit numbers. Both vertical & crosswise multiplications are showed below. The two digit multiplication example of 24 X 43 is given below

Step. 1 :

```
     2     4
           |
×    4     3
-------------
           2
   Carry = 1
```

Step. 2 :

```
     2     4              6
       ><
×    4     3          +  16
-------------        --------
        3  2             23
Next carry = 2
```

Step. 3 :

```
     2     4              2
     |
×    4     3          +   8
-------------        --------
  1  0  3  2             10
```

The multiplication of 24* 43 results 1032. In the above example, the first step is to multiply, the LSB of multiplicand with LSB of multiplier. If the carry is generated than add carry with next result of cross multipliers. If carry is not generated than write the answer of product as a result.

B. 4×4 Vedic multiplication

Let's analyze 4x4 multiplications, say A3A2 A1A0 and B3B2B1B0. Following are the output line for the multiplication result, S7S6S5S4S3S2S1S0. Let's divide A and B into two parts, say A3 A2 & A1 A0 for A and B3B2 & B1B0 for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication.

```
A3A2      A3A2
B3B2        B1B0
---------- ----------
  S7S6S5S4                      S11S10S9S8


A1A0 A1 A0
B3B2 B1 B0
----------- ------------
   S15S14S13S12                 S3S2S1S0
```

Each block as shown above is 2x2 multiplier. First 2x2 multiplier inputs are A1 A0 and B1B0.The last block is 2x2 multiplier with inputs A3 A2 and B3 B2. The middle one shows two, 2x2 multiplier with inputs A3A2 & B1B0 and A1A0 & B3B2. So the final result of multiplication, which is of 8 bit, S7S6S5S4S3S2S1S0, can be interpreted as given below.

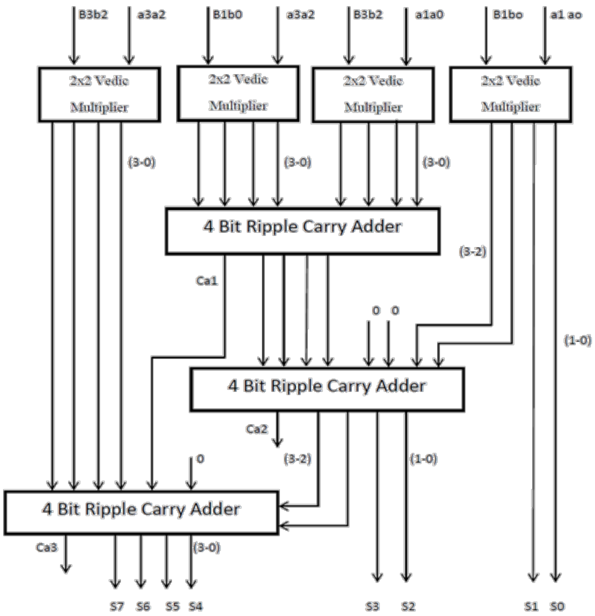

Fig. 1:Diagram of 4x4 bit Vedic Multiplier

Like that using 2*2 multiplication in 4*4 multiplication in structural method get the answer. Till 64*64 bit multiplication reach using 2*2 multiplication method.

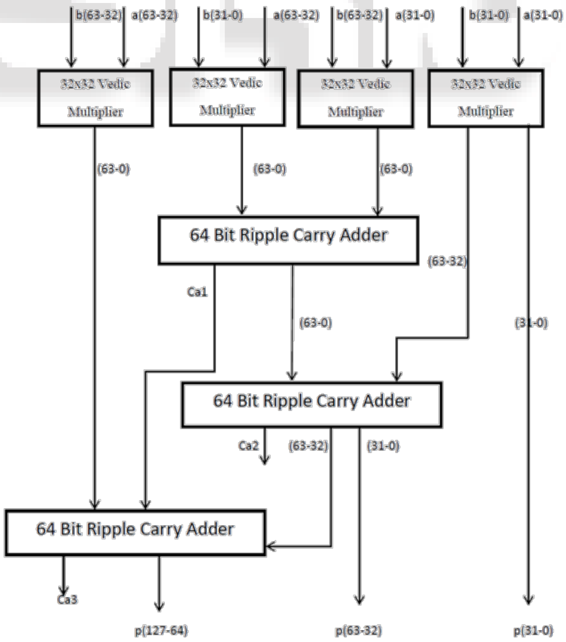

Fig. 2: Diagram of 64x64 bit Vedic Multiplier

III. DESIGN DESCRIPTION

In this project work all the designs are done using VHDL language. VHDL is an acronym for VHSIC (Very High Speed Integrated Circuit) Hardware Description Language. It is intended for documenting and modeling digital systems ranging from a small chip to a large system. VHDL is used

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because of its portability, flexibility, and readability. The design of each block includes the following steps 1.Understanding the functionality of the module and its sub-modules, 2.Developing VHDL codes for the top module and its sub-modules, 3.Design synthesis, 4.Mapping and Routing, 5.Test-bench waveform generation and testing, 6.Error-correction, 7.FPGA Implementation. In this project all the designs have been implemented on an Spartan 3E family FPGA using the Xilinx 13.4 ISETM design tool suite.

FPGA SPECIFICATION	
FAMILY	Spartan 3E
DEVICE NAME	XC3S1600E
PACKAGE	FG484
SPEED GRADE	-5

Table. 1: FPGA Specification

IV. IMPLEMENTATION OF 64×64 MULTIPLIER

In this work, 64x64 bit Vedic multiplier is designed in VHDL (Very High Speed Integrated Circuits Hardware Description Language). Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in XilinxISE13.4i - Project Navigator and ISE simulator integrated in the Xilinx package. The performance of circuit is evaluated on the Xilinx family Spartan3,device XC3S1600,package fg484 and speed grade -5. The RTLschematic of 64x64 bit Vedic multiplier is shown in Fig below.

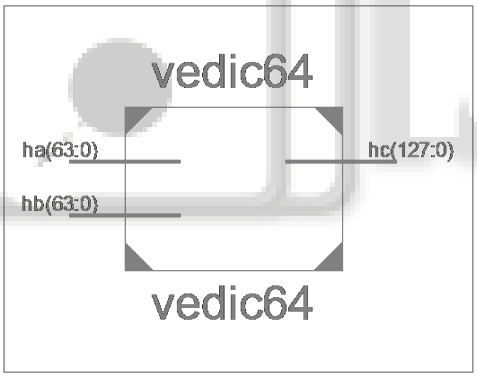

Fig. 3: RTL view of 64*64 Vedic Multiplication

Logic Utilization	Used	Available	Utilization
Number of Slices:	7,342	14,752	49%
Number of 4 input LUTs:	12,070	29,504	40%
Number of bonded IOBs	256	376	68%

Table. 2: Device Utilization Summary of 64x64 bit

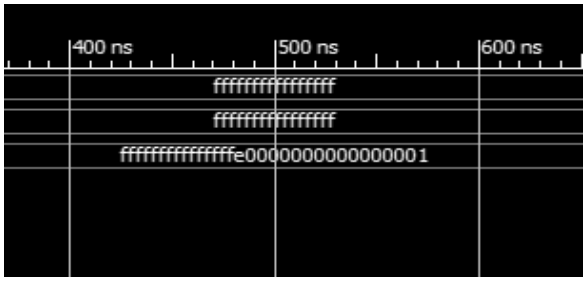

Fig. 4: Test bench Waveform

V. RESULT AND CONCLUSION

Type of Multiplier(64 bit)	Delay(ns)
Simple Multiplication	153.441 ns
Urdhava Multiplication	129.181 ns

Table. 3: Comparison of multipliers in terms of delay.

This paper represents the comparison between 64 bit multiplier with Simple multiplication and Vedic multiplication using the Urdhva-tiryakbyham sutra. The 64×64 Vedic multiplier is coded in VHDL, synthesized and simulated using Xilinx ISE 13.4 software. The synthesis result shows that 64×64 Vedic Multiplier is having less delay or we say that 64×64 Vedic Multiplier is faster than the Simple Multiplier.

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