Review of Low Power Testing Techniques

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Abstract—the circuit consumes more power during test mode compared to functional mode. So test power has been major big concern in large System-on-Chip designs from last decade. In this review paper, the state-of-the-art in low power testing is presented. The paper contains the detailed survey on various power reduction techniques proposed for both the aspects of testing i.e. external testing as well as Built-In-Self-Test. The advances in DFT techniques emphasizing low power are also included in this survey paper.

I. INTRODUCTION

The System-on-Chip (SOC) revolution has brought some new challenges to both design and test engineers. Among these challenges, power dissipation is one of the most important issues. Generally, a circuit may consume more power in the test mode than in the normal mode. It has been shown that the test power can be as high as twice the power consumed in the normal mode. There are several reasons for this increased test power. First, the test efficiency has been shown to have a high correlation with the toggle rate hence in the test mode, the switching activity of all nodes is often several times higher than the activity during normal operations. Secondly, in a SOC, parallel testing is frequently employed to reduce the test application time, which may result in excessive energy and power dissipation. Third, the design-for-testability circuitry embedded in a circuit to reduce the test complexity is often idle during normal operations but may be intensively used in the test mode. Another reason is that successive functional input vectors applied to a given circuit during system mode have a significant correlation, while the correlation between consecutive test patterns can be very low. This can cause significantly larger switching activity in the circuit during test than that during its normal operation. Since power dissipation in CMOS circuits is proportional to switching activity, this excessive switching activity during test may be responsible for cost, reliability, performance verification, autonomy and technology related problems. For example, in battery powered devices, the power consumed during application of power-up or periodical on-line tests, which are often implemented resorting to the Built-In Self-Test (BIST) approach, can dramatically shorten the battery lifetime. Another example of such problems is that increased circuit activity and hence power consumption leads to increased current flows during test, making the use of expensive packages for the removal of excessive heat an imperative need. Increased heat leads also to serious silicon failure mechanisms, such as electro migration, that reduce the reliability of a system operating under such conditions. As a result, the semiconductor industry is looking for low power testing techniques [1].

Various low power testing techniques are very well described in [2]. For this survey, the reference [2] published in 2002 has been taken as a platform. The author has presented the brief overview of techniques described in [2] and then explored the further research activities in the same direction during last decade.

The paper is organized as follows. Section II contains the various low power testing techniques for external testing of SoC using ATE. Various low power testing techniques for BIST are presented in section III. DFT techniques which focus on low power testing are discussed in section IV. Section V concludes the survey and explores the future scope.

II. LOW POWER EXTERNAL TESTING TECHNIQUES

Various techniques described in literature to ensure nondestructive external testing of a SoC using ATE are categorized in following subsections.

A. Low Power ATPG Algorithm

The basic goal of automatic test pattern generation (ATPG) was to decide the test pattern for given design under Test (DUT) which gives maximum fault coverage. The current research in this field focuses on ATPG algorithm which not only gives maximum fault coverage but also ensures the maximum fault coverage at lowest possible power dissipation. In this category first of all Podem algorithm proposed by Wang and Gupta and the method of exploiting the redundancy by fault dropping proposed by Corno et al. has been covered in previous survey paper by P.Girard [2]. Few other methods are also researched in this area. Polian I. et al [3]. Propose a heuristic method to generate test sequences which create worst-case power drop by accumulating the high and low-frequency effects. The generated patterns need to be sequential even for scan designs. They employ a *dynamically constrained* version of the classical D-algorithm for test generation, i.e., the algorithm generates new constraints on-the- fly depending on previous assignments. In an another approach Ho Fai Ko, Nicolici N [4] suggested that scan chain division has been successfully used to control shift power by enabling mutually exclusive flip-flops at different times during the scan cycle. However, to control capture power without losing transition fault coverage during at-speed scan test, the existing automatic test pattern generation (ATPG) flows need to be modified. He presented a novel scan chain division algorithm that analyzes the signal dependencies and creates the circuit partitions such that both shift and capture power can be reduced when using the existing ATPG flows. Whereas Sying-Jyan Wang et al. [5] present a low capture power ATPG and a power-aware test compaction method. Two goals are achieved by the proposed ATPG. (1) The growth of test pattern count is lower than the detection

number *n*. (2) The peak power becomes smaller as the detection number *n* increases. The test compaction algorithm further reduces the number of test patterns as well as the average capture power.

B. Ordering Techniques

The researches have widely explored the test vector reordering techniques to reduce the switching power. The earlier method based on Hamming distance based reordering proposed by P Girard and Debholkar are described in survey paper [2]. Girard's approach of vector ordering is enhanced by Paramasivam K, Gunavathi K, Sathishkumar P They have shown that the switching activity can be reduced up to 35 % [6]. In another method Roy S, Sen Gupta I, Pal a [7] proposed an AI-based approach to order the test vectors in an optimal manner to minimize switching activity during testing. A reordering method containing combination of test vector reordering as well as column wise bit stuffing ring within a given vector is proposed in [].

C. Input Control

Here the idea is to identify an input control pattern such that by applying the pattern to the primary inputs of the circuit during the scan operation, the switching activity in the combinational part can be minimized or even eliminated. Huang and Lee's basic idea of input control technique with existing vector- or latch-ordering techniques that reduces the power consumption has been covered in previous survey paper by P. Girard [2]. In the same area ElShoukry. M et al. [8] presented a technique of gating partial set of scan cells. The subset of scan cells is selected to give maximum reduction in test power within a given area constraint. An alternate formulation of the problem is to treat maximum permitted test power and area overhead as constraints and achieve a test power that is within these limits using the fewest number of gated scan cells, thereby leading to least impact in area overhead. The area overhead is predictable and closely corresponds to the average power reduction.

D. Vector Compaction and Data Compression

ATPG generated uncompact test data contains a large number of don't care bits. There are number of test data compression techniques which explores the don't care filling options to optimize the compression of test data. The next generation compression scheme does not only aims to maximum compression but also explores the don't care bit filling to give minimum switching activity and hence power reduction. Static compaction techniques to control scan vector power dissipation proposed by R. Sankaralingam et al. and a technique of Combining Low-Power Scan Testing and Test Data Compression for System-on-a-Chip proposed by A. Chandra and K. Chakrabarty has been covered in previous survey paper by P Girard [2]. Few other methods are also suggested after that, for Vector Compaction which are based on don't care filling. Among them Sying-Jyan Wang et al. [9] proposed an automatic test pattern generation (ATPG) scheme for low power launch-off-capture (LOC) transition test. Two techniques are explored in the proposed ATPG. A *bidirectional* X-filling and vector replacement scheme. Whereas Kundu S, Chattopadhyay S [10] have used a Genetic Algorithm based heuristic to fill the don't cares. Their approach produces an average percentage improvement in dynamic power and leakage power over 0- fill, 1-fill, and Minimum transition fill (MT-fill) algorithms for don't care filling. In an another approach Z. Chen et al. [11] proposed segment-based X-filling to reduce test power and keep the defect coverage. The scan chain configuration tries to cluster the scan flip-flops with common successors into one scan chain, in order to distribute the specified bits per pattern over a minimum number of chains. Based on the operation of a state machine, Jing-Ling Yang and Qiang Xu [12] elucidates a comprehensive frame for probability-based primary-input dominated X-filling methods to minimize the total weighted switching activity (WSA) during the scan capture operation. Experimental results demonstrate that the proposed approach significantly reduces both average and peak WSAs. Whereas Tapas M and Santanu C [13] describe the effect of don't care filling of the patterns generated via automated test pattern generators, to make the patterns consume lesser power. It presents a trade-off in the dynamic and static power consumption. The effect is expected to be more prominent for technologies beyond 100 nm. A 2D reordering method combined with power efficient don't care filling method is proposed in [ ].

E. Scan Chain Transformation

Here the scan architecture is designed in such a way that it maintains the test time, enables reuse of the conventional scan architecture's test patterns, and avoids decreasing the scan clock rate. Previously L. Whetsel's approach of , Adapting Scan Architectures for Low Power Operation and K.J.Lee's approach of Peak-Power Reduction for Multiple-Scan Circuits during Test Application has been covered in previous survey paper by P Girard [2]. In addition to that Sinanoglu, O, Orailoglu A [14] proposed a scan chain modification methodology that transforms the stimuli to be inserted to the scan chain through logic gate insertion between scan cells, reducing scan chain transitions. Based on this analysis, they developed an algorithms for transforming a set of test vectors into power optimal test stimuli through cost-effective scan chain modifications.

F. Clock Scheme Modification

Giving a clock to a whole circuit will give some unnecessary transition, which affects on power and energy consumption. Here the techniques are described which manages the clock distribution in such a way that overall it consumes less power. Previously Pouya and Crouch's ideas on optimization trade-offs for vector volume and test power , Sankaralingam et al approach on reducing power dissipation during test using Scan chain disable, Bonhomme et al's approach based on a gated clock scheme for low power scan testing of logic ic or embedded cores have are covered in previous survey paper by P Girard [2]. It is found that many STUMPS architectures found in current chip designs allow disabling of individual scan chains for debug and diagnosis, such feature can be used for reducing the power consumption during test. Here Imhof M.E et al. [15] presented an automated generation of a test plan that keeps fault coverage as well as test time, while significantly reducing the amount of wasted energy by disabling of individual scan chains for debug and diagnosis.

III. LOW POWER BIST TECHNIQUES

Various authors reported on techniques to cope with power problems during BIST. In the following, these techniques for low power BIST are presented.

A. Low Power Test Pattern Generators

In this category the BIST architecture is designed in such a way that it decreases the circuits overall activity so that power consumption reduces significantly. Previously BIST strategy, called dual-speed LFSR was suggested by Wang and Gupta, based on two different speed LFSRs. Also Corno et al proposed an approach on low power BIST via non-linear hybrid cellular automata. Then a modified clock scheme for a low power BIST test pattern generator was proposed by P Girard, In addition to that Zhang et al suggested a POWERTEST tool , which is a Tool for Energy Conscious Weighted Random Pattern Testing. Whereas Wang and Gupta proposed LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation. These all have been covered in previous survey paper by P Girard [2]. After that Ahmed N et al. [16]. presented a new low power test pattern generator using a linear feedback shift register (LFSR), called LP-TPG, which inserts intermediate patterns between the random patterns to reduce the transitional activities of primary inputs which eventually reduces the switching activities inside the circuit under test, and hence, power consumption. Hiirevren and Levent [17] proposed a polynomial-time algorithm that converts the test pattern generation problem into combinatorial problem called Minimum *Set* Covering. Solutions to that give the low-power design topology for the test pattern sequence. Youbean K et al. [18] present a new low power BIST TPG scheme. It uses a transition monitoring window (TMW) that comprised of a TMW block and a MUX. The proposed technique represses transitions of patterns using the k-value which is a standard that is obtained from the distribution of TMW to observe over transitive patterns causing high power dissipation in a scan chain. K.Gunavathil et al. [19] proposed TPG based on Read Only Memory (ROM) which is carefully designed to store the test vectors with minimum area over the conventional ROM. This reduces the number of CMOS transistors significantly when compared to that of LFSR/Counter TPG. Bin Z. et al [20] proposed approach to reconfigure the CUT's partial-acting-inputs into a short ring counter (RC), and keep the CUT's partial-freezing-inputs unchanged during testing. S.Wang [21] presents a low hardware overhead test pattern generator (TPG) for scan-based built-in self-test (BIST) that can reduce switching activity in circuits under test (CUTs) during BIST and also achieve very high fault coverage with reasonable lengths of test sequences. The proposed BIST TPG decreases transitions that occur at scan inputs during scan shift operations and hence reduces switching activity in the CUT. M.Nourani et al. [22] proposed low-transition linear feedback shift register (LT-LFSR) technique. Transitions are reduced in two dimensions: 1) between consecutive patterns and 2.) Between consecutive bits. The proposed architecture increases the correlation among the patterns generated by LT-LFSR with negligible impact on test length. Bei Cao et al. [23] presented an efficient algorithm to synthesize a built-in TPG from low power deterministic test patterns without inserting any redundancy test vectors. The structure of TPG is based on the non-uniform cellular automata (CA). And the algorithm is based on the nearest neighborhood model, which can find an optimal non-uniform CA topology to generate given low power test patterns. Li-gang Hou et al. [24] proposed a low power dynamic LFSR (LDLFSR) circuit which achieves comparable performance with less power consumption. Typical LFSR, a DFLSR [I], a LDLFSR are compared on randomness property and inviolability property. Multi-layer perceptron neural networks are used to test these LFSRs' inviolability property. H.-T. Lin J.C.-M. Li. [25] presented ATPG technique, which simultaneously reduces capture and shift power during scan testing. This ATPG performs power reduction during dynamic test compaction so the test length overhead is very small. This method implements several novel techniques, such as parity back trace, confined propagation, dynamic controllability and post-fill test regeneration. T

B. LFSR Tuning

Here this category mainly emphasized on reduction energy consumption without modifying the fault coverage. Various BIST techniques are described here. Earlier Girard et al. address the problem of energy minimization during test application for BIST enabled circuits [2]. In a random testing environment, a significant amount of energy is wasted in the LFSR and in the CUT by useless patterns that do not contribute to fault dropping. In this work, a new built-in self-test scheme for scan-based circuits is proposed by Bhattacharya B.B. et al. [26] for reducing such energy consumption. A mapping logic is designed which modifies the state transitions of the LFSR such that only the useful vectors are generated according to a desired sequence. Experimental results on ISCAS-89 benchmark circuits reveal a significant amount of energy savings in the LFSR during random testing.

C. Vector Filtering BIST

Here main idea is to filter out some non-detecting sequences so that over all switching can be reduced and hence power consumption. Previously Girard et al. proposed a test-vector-inhibiting technique to filter out some non-detecting subsequences of a pseudorandom test set generated by an LFSR. His work was extended by Manich et al. by the filtering action to all the non-detecting subsequences. The authors use a decoding logic to store the first and last vectors of the non-detecting subsequences to be filtered and the same idea was implemented by Gerstendörfer and Wunderlich. These authors combine a pattern-filtering technique with Hertwig and Wunderlich's technique to avoid scan-path activity during scan shifting. These all have been covered in previous survey paper by P Girard [2]. After that S. Hatami et al. [27] proposed a scan cell architecture that decreases power consumption and the total consumed energy. In the method which is based on the data compression, the test vector set is divided into two repeated and unrepeated partitions. The repeated part, which is common among some of the vectors, is not changed during the new scan path where new test vector will be filled. As a result, the test vector is applied to the circuit under test in a fewer number of clock cycle, leading to a lower switching activity in the scan-path during test mode.

D. Circuit Partitioning

Main goal here is to partition the circuit in to sub circuit so that parallel testing can be achieved. Girard et al. propose a novel low-power BIST strategy based on circuit partitioning. This strategy partitions the original circuit into

two structural sub circuits so that two different BIST sessions can successively test each sub circuit. This idea has been covered in previous survey paper by P Girard [2]. To address the power in the scan chain, Swarup B et al [28] propose an efficient scan partitioning technique that reduces both average and peak power in the scan chain during shift and functional cycles. Whereas Qiang Xu et al. [29] proposed a novel low-power virtual test partitioning technique where faults in the glue logic between sub circuits can be detected by patterns with low power dissipation that are applied at the entire circuit level, while the patterns with high power dissipation can be applied within a partitioned sub circuit without loss of fault coverage. Experimental results show that the proposed technique is very effective in reducing test power.

E. Low Power RAM Testing

Various RAM transition reduction technique by reordering read and write access are described for low power consumption. Cheung and Gupta propose a methodology for low-power test of RAMs. The authors base their strategy on RAM transition reduction by reordering the read and write accesses and the address counting scheme. These measures decrease the energy consumption and keep test time the same, so they also minimize the average power [2]. The idea has been covered in previous survey paper by P Girard [2] a row bank-based pre-charge technique based on the divided word line (DWL) architecture is proposed by Shyue-Kung Lu et al. [30] for low-power testing of embedded SRAMs. In low-power test mode, instead of pre-charging the entire memory array, only the current accessed row bank is pre-charged. This will result in significant power saving for the pre-charge circuitry. With the ever increasing number of memories embedded in a system-on-chip (SoC), power dissipation due to test has become a serious concern. Here Yuejian Wu et al. [31] proposed a novel low power memory BIST. Its effectiveness is evaluated on memories in 130 and 90 nm technologies. A significant power reduction can be achieved with virtually zero hardware overhead.

IV. LOW POWER DFT TECHNIQUES

Apart from internal and external techniques here DFT techniques are described for low power testing. Here main goal is to reduce switching activity by adding some hardware during test. Xiaoming Yu and Miron Abramovici [32] introduce two design-for-testability (DFT) techniques based on clock partitioning and clock freezing to ease the test generation process for sequential circuits. In the first DFT technique, a circuit is mapped into overlapping pipelines by selectively freezing different sets of registers so that all feedback loops are temporarily cut. An opportunistic algorithm takes advantage of the pipeline structures and detects most faults using combinational techniques. This technique is feasible to circuits with no or only a few self-loops. In the second DFT technique, they use selective clock freezing to temporarily cut only the global feedback loops. These DFT techniques do not introduce any delay penalty into the data path, have small area overhead, allow for at-speed application of tests, and have low power consumption. Min-Hao Chiu Li, J.C.-M [33] presents a Jump scan technique (or J-scan) for low power testing. The J-scan shifts two bits of scan data per clock cycle so the scan clock frequency is halved without increasing the test time. The experimental data show that the proposed technique effectively reduces the test power by two thirds compared with the traditional MUX scan. The presented technique requires very few changes in the existing MUX-scan design for testability methodology and needs no extra computation. The penalties are area overhead and speed degradation.

V. CONCLUSION

The current methodologies on test power reduction techniques, either it is for external testing, BIST or DFT, are reducing the power consumption by reducing the switching activities during scan-in, scan-out or capture mode. For this purpose, people have used various methods like low power ATPG algorithm, reordering and compression of test vector compression, static compaction, LFSR manipulation, circuit partitioning and so on. Various advance algorithms from another field like Genetic, Artificial intelligence, neural network etc are also explored to reduce the switching activity while constraining various parameters. This survey has prepared a platform to researchers in the area of low power testing. The research can start with any of the method and further explore the possibilities of test power reduction with consideration of other parameters like test time, area overhead and test complexity issues.

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