

VHDL Implementation Of Optimized Cascaded Integrator Comb (CIC) Filters for Ultra High Speed Wideband Rate Conversion

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Abstract— Software defined radio (SDR) is a radio in which the properties of carrier frequency, signal bandwidth, modulation, and several other characteristics are defined by software. Today's SDR is turning the hardware problems into software problems, some or all of the physical layer functions are software defined. Digital down conversion (DDC) and Digital up conversion (DUC) is one of the core technologies in SDR, as well as an important component of digital intermediate frequency (IF) receiver system. Cascade Integrator Comb (CIC) filters are widely used in multirate signal processing as a filter in both decimator (decrease in the sampling rate) and interpolator (increase in the sampling rate). In this paper a CIC filter, an optimized class of linear filters is implemented for digital up conversion (DUC) and digital down conversion (DDC) for efficient transmission and reception in Software Defined Radio (SDR) communication system. In this project a full-fledged digital down conversion and digital up conversion systems are developed in VHDL for FPGA based software defined radio applications. The CIC based architecture is implemented in VHDL and will be tested on Xilinx FPGAs. All the modules functionality is verified with Modelsim simulator. Xilinx ISE tools are used for FPGA synthesis, Place & Route and timing analysis. Spartan 3E development board with Chipscope Pro Analyzer tool is used for on-chip verification.

Key words: CIC filter, Field Programmable Gate Array (FPGA), Decimator, Interpolator, Modelsim and Chipscope.

I. INTRODUCTION

Software defined radio is an emerging technology that is profoundly changing the radio system engineering. To implement software defined radios, the FPGA provides the best reconfigurable solution for high speed signal processing modules that are highly parallel. FPGA provides the best balance between performance, low power consumption, and short design cycle. Beside, the new Xilinx FPGA series provides a dynamic and partial reconfiguration functionality which is the ability to dynamically modify a local region of logic by downloading partial reconfiguration files while the remaining logic continues to operate without interruption.

Software Defined Radio (SDR) platforms make use of Digital Down Converter (DDC) and Digital Up Converter (DUC), while performing baseband processing. Digital up-conversion and down-conversion are well known sample rate conversion processes in Digital Signal Processing. These techniques are widely used for converting a baseband signal to band pass signal and vice versa to enable the transmission and reception. For the baseband signal to be transmitted, it needs to be modulated on to an IF/RF carrier frequency. In simple, down conversion can be defined as removing samples (also called as Decimation) and

generating new samples by virtue of adding zeroes (also called as Interpolation) and interpolate the new samples.

The major blocks in designing DDC and DUC [1] would include Numerical controlled oscillator (NCO), digital mixer, CIC decimation filter and CIC interpolation and compensation FIR filter.

CIC filters are good choice for implementing decimation or interpolation because they don't use multipliers and their frequency response can reduce aliasing and imaging issues resulting due to decimation and interpolation respectively. A CIC filter is typically used in applications where the system sample rate is much larger than the bandwidth occupied by the signal. They are commonly used to build Digital down Converters (DDCs) and Digital up Converters (DUCs) [1]. Some applications that use the CIC filter includes software designed radios, cable modems, satellite receivers, 3G base stations, and radar systems. Direct Digital Synthesizers enable micro-Hertz tuning resolution, extremely fast frequency hopping, digital control interface and elimination of manual tuning to tweak the performance. DDS implementation is very simple; it can be built using a phase accumulation circuitry and a look-up table preserving the signal samples. Having DDS on chip avoids the need of sampling circuits and provides a great flexibility in tuning to the required frequency.

In this project a full fledged digital up conversion and digital down conversion systems will be developed in VHDL for FPGA based software defined radio applications. The CIC [2] based architecture will be implemented in VHDL and will be tested on Xilinx FPGAs. Modelsim (6.2C) Xilinx Edition (MXE) will be used for functional verification of each block in DDC/DUC. Xilinx ISE 9.2i version will be used for synthesis and bit file generation and Xilinx Chip Scope Pro Analyzer tool is used for board level testing. Spartan 3E FPGA board having specification XC3S500E-4FG320 is used for implementing the design.

II. DIGITAL UP AND DOWN CONVERSIONS

Digital up converters (DUCs) and digital down converters (DDCs) [2] are important components of every modern wireless base station design. DUC are typically used in digital transmitters to filter, up sample, and modulate signals from baseband to the carrier frequency. A DDC, on the other hand, resides in the digital receiver to demodulate, filter, and down sample the signal down to baseband so that further processing on the received signal can be done at lower sampling frequencies.

A. Digital Down Conversion:

In digital signal processing, a digital down-converter (DDC) [2] converts a digitized real signal centered at an intermediate frequency (IF) to a base banded complex signal centered at zero frequency. In addition to down conversion, DDCs typically decimate to a lower sampling

rate, allowing follow-on signal processing by lower speed processors.

A DDC consists of three subcomponents: a direct digital synthesizer (DDS), a low-pass filter (LPF), and a down sampler (which may be integrated into the low-pass filter). Digital Down-Converter (DDC) is a key component of digital radios. The DDC performs the frequency translation necessary to convert the high input sample rates found in a digital radio, down to lower sample rates for further and easier processing. The DDC consists of a Numeric Controlled Oscillator (NCO) and a mixer to down convert the input signal to baseband. The baseband signal is then low pass filtered by a Cascaded Integrator-Comb (CIC) filter followed by two FIR decimating filters to achieve a low sample-rate. The DDS generates a complex sinusoidal signal at the intermediate to down converting by creating a difference signal at the IF minus the DDS frequency, they also up convert, generating an unwanted signal at the sum of the two frequencies.

DDCs are most commonly implemented in logic in field-programmable gate arrays or application-specific integrated circuits. While software implementations are also possible, operations in the DDS, multipliers and input stages of the low pass filters all run at the sampling rate of the input data. This data is commonly taken directly from analog to digital converters (ADC's) sampling at tens or hundreds of MHz, which is beyond the real time computational capabilities of software processors.

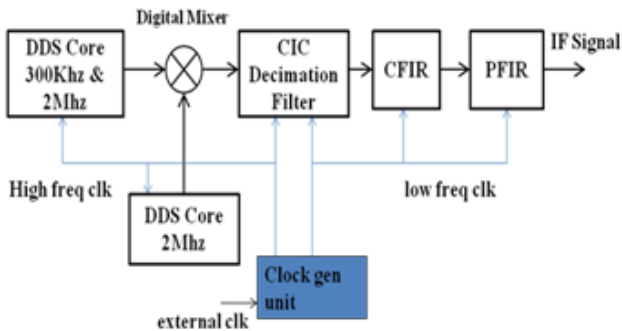


Fig. 1: Block diagram of the Digital down Conversion

A DDC [5] is the main part of digital receiver. The signal that enters the DDC will first be mixed to remove the carrier signal and bring the received signal down to baseband. This is done by multiplying the incoming signal with sine and cosine signal created using a DDS or NCO at the same frequency as the carrier frequency. This new signal, centered on the baseband frequency, is passed through several cascaded decimating CIC filter to shape the signal and reduce the sampling rate [3] of the signal.

Typically, the signal converted by the DDC gets transmitted and received at very high sampling rates. However, the receiver generally does not require such high signal resolution to perform the necessary signal processing. Therefore, it is important to decimate (reduce the number of samples) the incoming signal so that the rest of the signal processing can be done at lower, more reasonable sampling rates.

B. Digital up conversion:

A DUC [6] consists of a series of interpolation cascade integrator comb (CIC) filters, a zero stuffer, and a direct

digital synthesizer (DDS) or numerically controlled oscillator (NCO). Figure 2 shows the block diagram of the DUC and the two clock frequencies given to the various stages in the DUC.

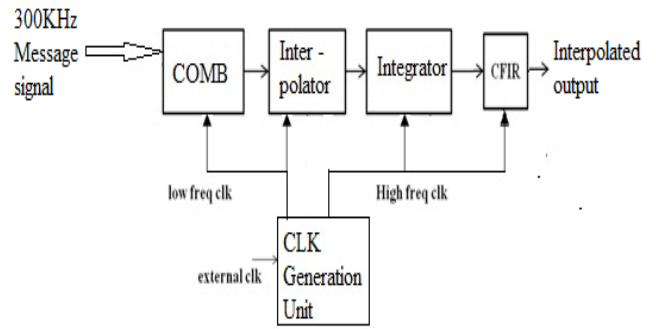


Fig. 2: Block diagram of a Digital up Conversion

In Figure 2, the zero stuffer is used for generating new samples by virtue of adding zeroes (also called as Interpolation) and interpolates the new samples. CIC filter [4] is used to shape and increase the sample rate of the transmit signal. The output signal from these filters is then mixed with the carrier signal prior to transmission. In simple, down conversion can be defined

A number of common building blocks are used to implement narrowband DUC/DDC systems. These include modules to implement functions such as filtering, carrier generation, and complex multiplication. The DUC and DDC consist of the following important blocks:

- [1] Numerically Controlled Oscillator (NCO)
- [2] The Mixer
- [3] Cascaded Integrated Comb (CIC)
- [4] Compensation Finite Impulse Response (CFIR)

1) Numerically Controlled Oscillator:

A numerically controlled oscillator is also called the Direct Digital Synthesizer (DDS). NCO is a digital signal generator creating a synchronous (i.e. clocked) discrete time, discrete valued representation of the sinusoidal waveform. It is an established method of generated periodic sinusoid signals whenever high frequency resolution, fast changes in frequency and phase and high spectrum density of the output signal is required. The major advantage of NCO is extremely fast hopping speed in frequency or phase tuning and easy programmability. The Direct digital synthesizer operates by storing the waveform point which is in digital format and later it recalls generating the waveform. The rate at which the synthesizer completes one waveform then determines the frequency.

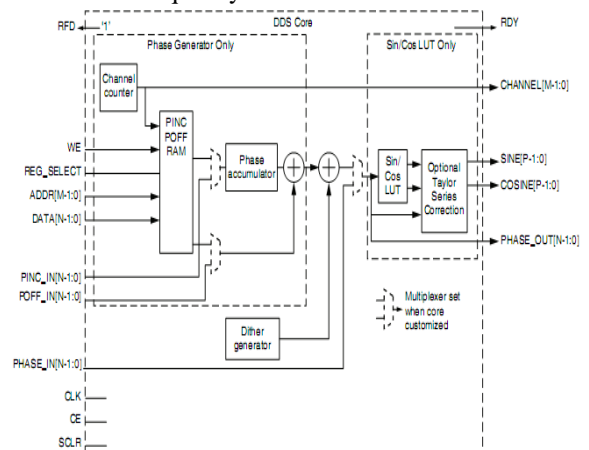


Fig. 3: Operation of Numerically Controlled Oscillator

The implementation of NCO includes the following important blocks:

- [1] Phase accumulator
- [2] Phase to amplitude converter and
- [3] Sin / cos LUT

A DDS produces a sine wave at a given frequency. The frequency depends on two variables, the reference clock frequency and the binary number programmed into the frequency register (tuning word). The binary number in the frequency register provides the main input to the phase accumulator. If a sine look-up table is used, the phase accumulator computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude - corresponding to the sine of that phase angle - to the digital to analog converter. The DAC, in turn, converts that number to a corresponding value of analog voltage or current. To generate a fixed-frequency sine wave, a constant value (the phase increment-which is determined by the binary number) is added to the phase accumulator with each clock cycle. If the phase increment is large, the phase accumulator will step quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, accordingly generating a slower waveform.

A phase to amplitude lookup table is used to convert the phase-accumulator's instantaneous output value with unneeded less significant bits eliminated by truncation into the sine-wave amplitude information that is presented to the D/A converter. The DDS architecture exploits the symmetrical nature of a sine wave and utilizes mapping logic to synthesize a complete sine wave from one quarter-cycle of data from the phase accumulator. The phase to amplitude lookup table generates the remaining data by reading forward then back through the lookup table.

2) *The Mixer:*

A mixer is used to convert the IF signal to baseband signal by multiplying the input signal with complex sinusoidal signal $\cos(wt)-j \sin(wt) = e^{-j\omega t}$ which is generated by NCO thus giving two signals as output i.e.;

- In-Phase signal
- Quadrature-Phase signal

The two signals are 90 degrees out of phase with each other.

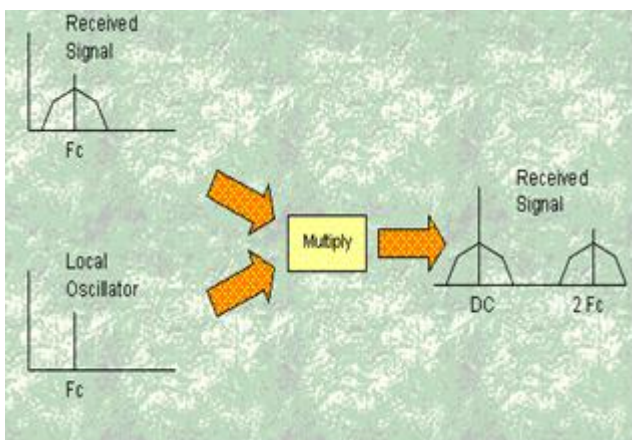


Fig. 4: Mixer

This works on the (simplified) mathematical principle:

Frequency (A) * Frequency (B) = Frequency (A-B) + Frequency (A+B).

3) *Cascade Integrator Comb Filter:*

Cascaded Integrator Comb filter plays a vital role to many high volume wireless communication tasks and components with CIC greatly achieve reliability, performance and reduce cost. The Cascaded Integrator Comb (CIC), first introduced by Hogenauer [6], presents a simple but effective platform for implementation of such decimation and interpolation. CIC filters are well-suited for anti-aliasing filtering prior to decimation (sample-rate reduction), and for anti imaging filtering for interpolated signals (sample-rate increase). This type of filter has extensive applications in low cost Implementation of interpolators and decimators. And major advantage of CIC is the arithmetic computation use adders and subtractors and register they don't require multiplication. However some drawback of CIC filters like pass band droop in this filter but they are eliminated using compensation techniques

The CIC filter consists of N stages of integrator and comb filter. The two basic building blocks of a CIC filter are an integrator and a comb is as shown below.

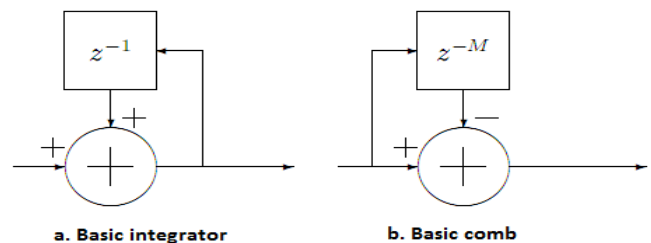


Fig. 5: Basic Building Blocks of CIC Filter

An integrator is simply a single-pole IIR filter with a unity feedback coefficient:

$$y[n]=y[n-1]+x[n]$$

This system is also known as an accumulator. The transfer function for an integrator on the z-plane is

$$H_I(z) = \frac{1}{1 - z^{-1}}$$

A comb filter running at the low sampling rate, f_s / R , for a rate change of R is an odd- symmetric FIR filter.

$$y[n]=x[n]-x[n-RM]$$

In this equation, M is a design parameter and is called the differential delay. M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer at f_s

$$H_C(z) = 1 - z^{-RM}$$

When we build a CIC filter, we cascade, or chain output to input, N integrator sections together with N comb sections. This filter would be fine, but we can simplify it by combining it with the rate changer. The CIC filters operate blocks for interpolator and decimator is as follows:

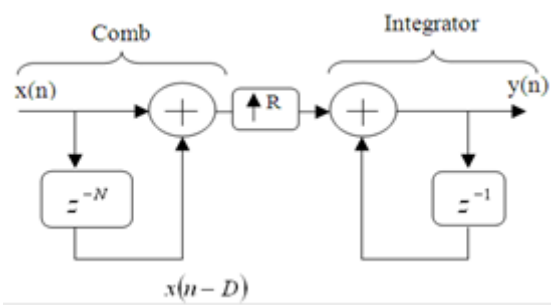


Fig. 6: Cascaded Integrator Comb for Interpolator

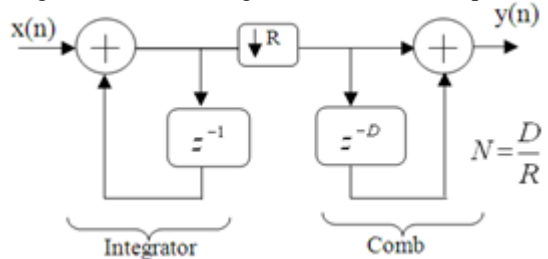


Fig. 7: Cascaded Integrator Comb for Decimator

To summarize, a CIC decimator would have N cascaded integrator stages clocked at fs, followed by a rate change by a factor R, followed by N cascaded comb stages running at fs/R. A CIC interpolator would be N cascaded comb stages running at fs/R, followed by a Zero-stuffer, followed by N cascaded integrator stages running at fs.

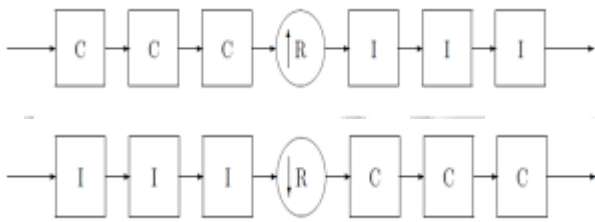


Fig. 8: Three stage decimator and interpolator filters

Frequency Characteristics:

The transfer function for a CIC filter at fs is

$$H(z) = H_I^N(z) H_C^N(z) = \frac{(1 - z^{-D})^N}{(1 - z^{-1})^N} = \left[\sum_{k=0}^{D-1} z^{-k} \right]^N$$

This equation shows that even though a CIC has integrators in it, which by themselves have an infinite impulse response, a CIC filter is equivalent to N FIR filters, each having a rectangular impulse response. Since all of the coefficients of these FIR filters are unity, and therefore symmetric, a CIC filter also has a linear phase response and constant group delay.

4) Compensation FIR Filter:

The compensation filter is a class of FIR filter. In the typical decimation/interpolation filtering applications a reasonably flat pass band and narrow transition region filter performance is required. CIC filter followed by compensating FIR filter are realized to achieve flat magnitude response over pass band. The programmable filter after CFIR is realized to further rejected aliased band due to decimation. FDA tool is used for generating the filter coefficients for various filters. The inverse SINC function is taken for realizing CFIR filter. Filter coefficients are converted to fixed point and used in VHDL coding.

The frequency response can be represented as

$$H(f) = \left| MR \frac{\sin \pi f}{\sin(\pi R M f)} \right|^N \approx \left| \frac{\pi M R f}{\sin(\pi R M f)} \right|^N = |\sin c^{-1}(M R f)|^N$$

III. SOFTWARE & HARDWARE REQUIREMENT

An advantage of using an FPGA for the DDC/DUC is that we can customize the filter chain to exactly meet our requirements. ASSPs don't offer the design flexibility or integration attainable in an FPGA. During the design, a behavioral model of the complete digital down conversion and digital down conversion methods are developed using Xilinx ISE software by writing VHDL code for each individual block and their operation is tested by simulating the design using Modelsim Simulator. Later the design is synthesized and implemented on an FPGA by generating a .bit file of the design and programming, configuring the FPGA with the .bit file. The Xilinx Design flow is shown below.

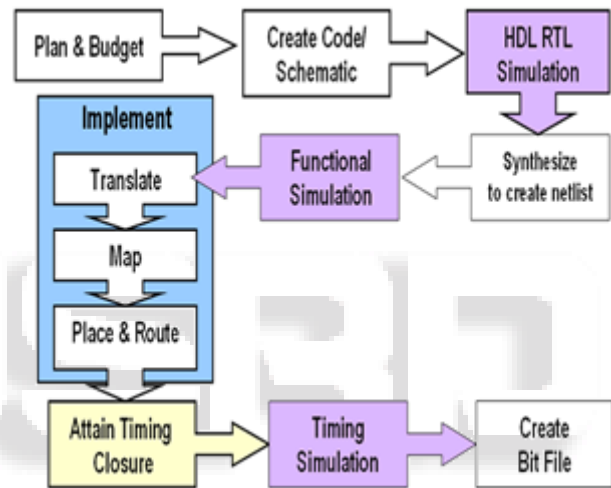


Fig. 9: Xilinx Design Flow

Spartan 3E development board with Chipscope Pro tools is used for on chip analysis and debugging. The correct Operation of the design in the FPGA is tested using Chip Scope Pro Analyzer tool which uses three main blocks to Where M is the differential delay of CIC filter, N is the Stage of the filter.

analyze any part of DDC. These blocks are generated through the IP Core Generator tool in Xilinx ISE.

The blocks are:

- [1] **ICON:** Integrated controller is use as an interface between the other two blocks and PC, JTAG which is connected to FPGA on which the design is programmed.
- [2] **ILA:** Integrated Logic Analyzer is used to control the inputs of any part of DDC thus achieving Controllability of inner circuits.
- [3] **VIO:** Virtual input output is used to observe the outputs of any part of DDC thus achieving observability.

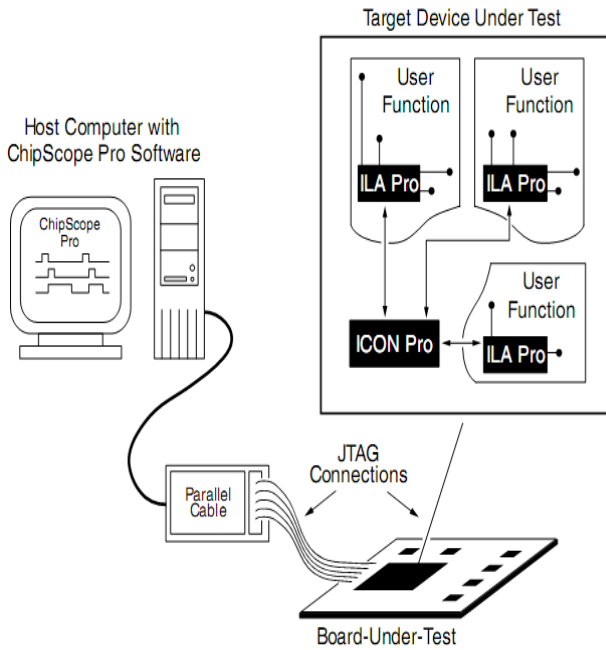


Fig. 10: Chip Scope pro Block Diagram

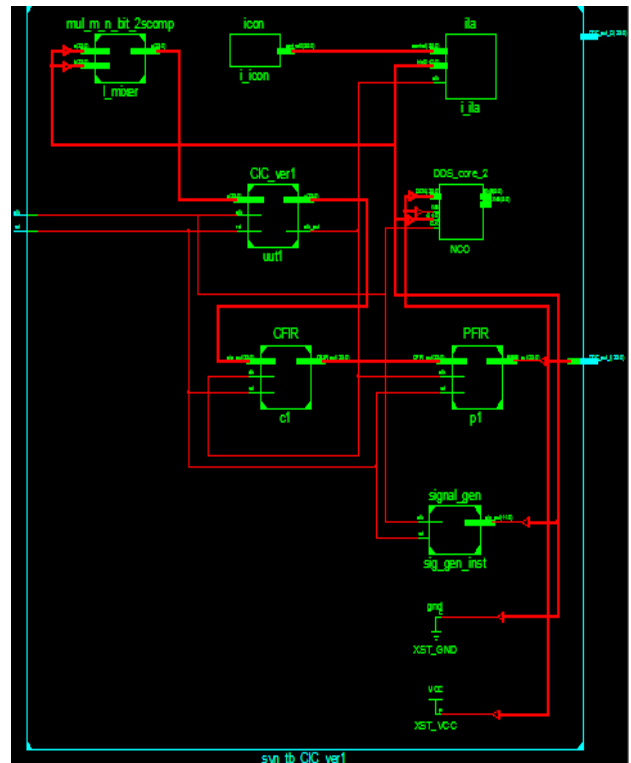


Fig. 12: RTL Schematic of DDC

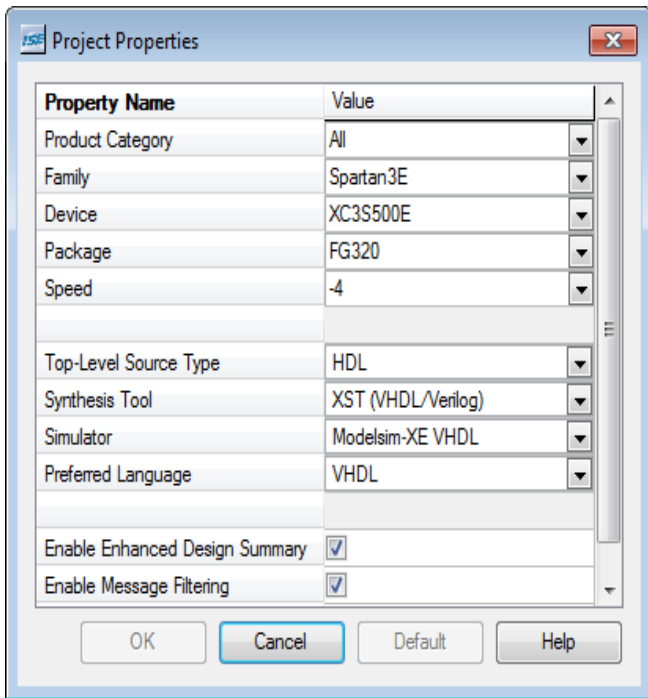


Fig. 11: Device Specifications in Xilinx 9.2 for DDC/DUC

IV. RESULTS

A. RTL Schematics:

The following two figures shows the Register Transfer Level (RTL) Schematics obtained for CIC based DDC and DUC.

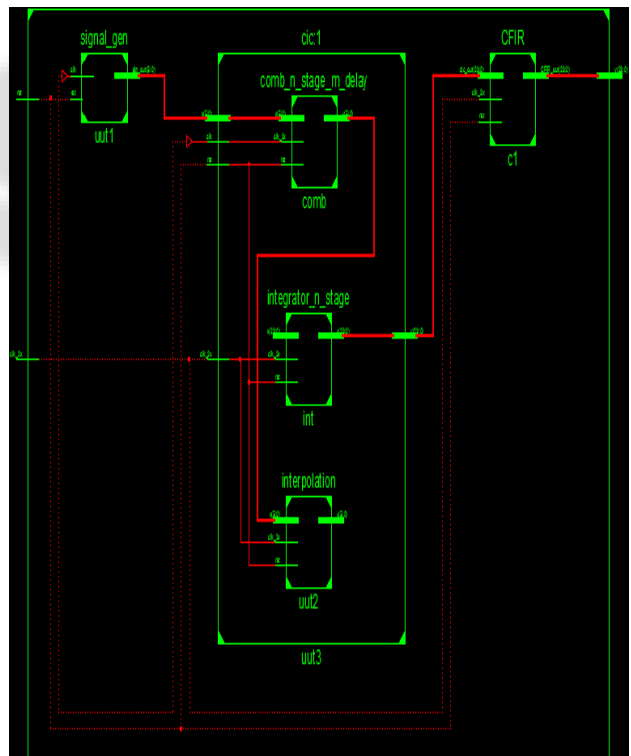


Fig. 13: RTL schematic of DUC

B. Simulation Results:

CIC based DDC Final Output:

The following two figures show the simulation results obtained for CIC based DDC. The test input signal (300KHz) is the first waveform after reset and clock mixed with 2 MHz Carrier signal. This signal is obtained by multiplying two DDS's outputs. This is the third waveform in the below figure. The last waveform is Integrator output having large amount of sampling rate.

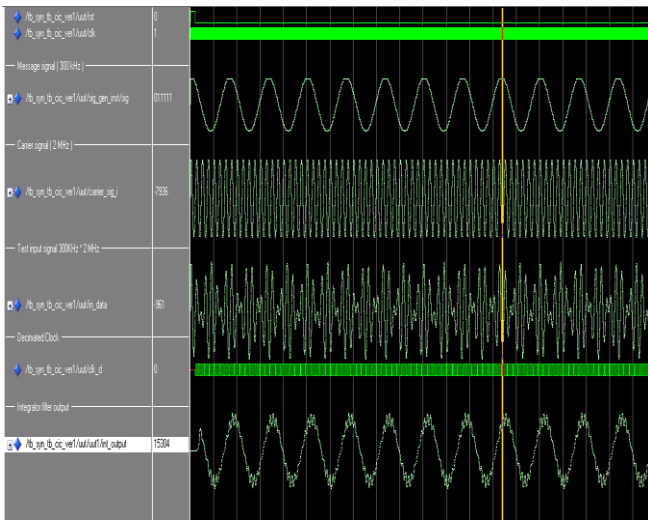


Fig. 14: Simulation of message signal

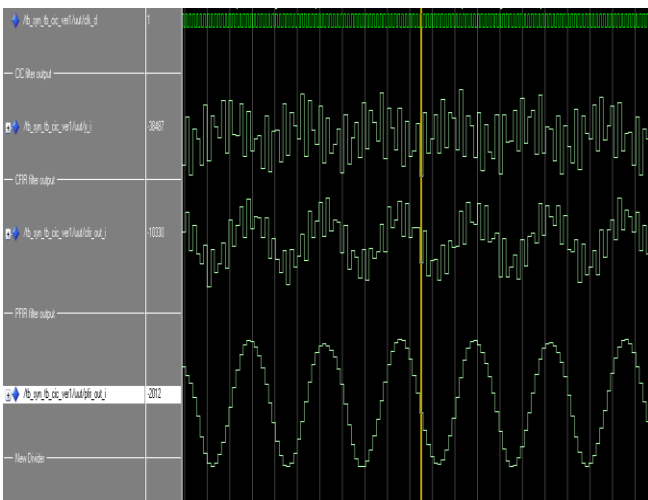


Fig. 15: Simulation of CIC and PFIR outputs

In the above figure first waveform is the decimated clock with a factor of 8. The second waveform is the complete CIC output. We can notice the CIC output is coming with decimated clock. Next in the figure compensating FIR filter (CFIR) output is shown. This becomes input to programmable FIR (PFIR) filter. The last waveform shows the output of PFIR filter. As expected the 300 KHz base band signal with decimated clock is recovered.

CIC based DUC Final Output:

The following figure shows the simulation results obtained for CIC based Digital up conversion (DUC).

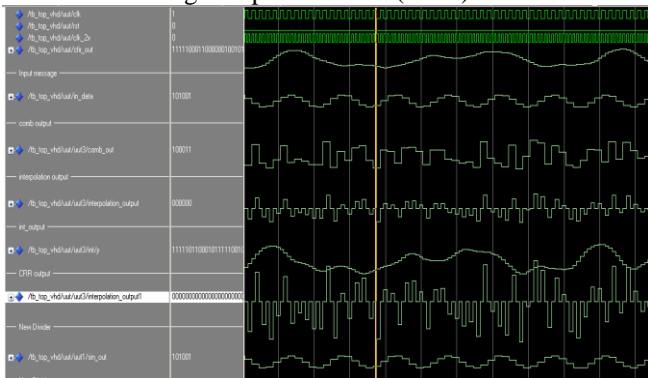


Fig.16:Simulation results of DUC cfir outputs

C. XILINX Synthesys Report:

Device utilization summary:		
Selected Device : XC3S500EFG320-4		
Number of IOs : 50		
1	No. of Slices: 3986 out of 4656	87%
2	No. of Slice Flip Flops : 2635 out of 9312	28%
3	No. of 4 input LUTs : 5322 out of 9312	57%
4	No. of bonded IOBs : 26 out of 232	11%
5	No. of MULT18X18SIOs : 9 out of 20	45%
6	No. of GCLKs : 3 out of 24	12%
7	No. of DCMs : 1 out of 4	25%

Table 1:Synthesis Report of CIC based DDC

Timing summary:	
Speed grade : -4	
1	Min period :16.196ns(Max requency:61.744MHz)
2	Min Input Arrival time before clock: No path found
3	Max output required time after clock:7.245ns
4	Max combinational path delay:4.733ns

Table 2

Device utilization summary:		
Selected Device : XC3S500EFG320-4		
Number of IOs : 26		
1	No. of Slices: 590 out of 4656	12%
2	No. of Slice Flip Flops : 653 out of 9312	07%
3	No. of 4 input LUTs : 1084 out of 9312	11%
4	No. of bonded IOBs : 26 out of 232	11%
5	No. of MULT18X18SIOs : 10 out of 20	50%
6	No. of GCLKs : 2 out of 24	08%
7	No. of DCMs : 1 out of 4	25%

Table 3: Synthesis Report of CIC based DUC

Timing summary:	
Speed grade : -4	
1	Min period:15.395ns (Max Frequency: 64.957MHz)
2	Min Input Arrival time before clock: No path found
3	Max output required time after clock: 4.040ns
4	Max combinational path delay: No path found

Table 4

D. Performance, Area Comparison of Cic and Polyphase Structures:

	CIC Filter	Polyphase Filter
Number of Slices	3320	3966
Number of Slice Flip Flops	2635	2393

Table 5: Area Comparison

	CIC Filter	Polyphase Filter
Minimum period	16.196ns	11.333ns

Table 5: Speed Comparison

E. Hardware Verification Results:

The CIC after porting on FPGA [7] is tested with chipscope. Because of memory limitations on FPGA each stage output is not capture on chipscope. Only the input and output are connected to chipscope data port. The below figure shows the test input signal for DDC which is 300 KHZ mixed with 2 MHz carrier. We can notice that the in data check box is selected in the bus plot.

Chipscope Pro Analyzer results:

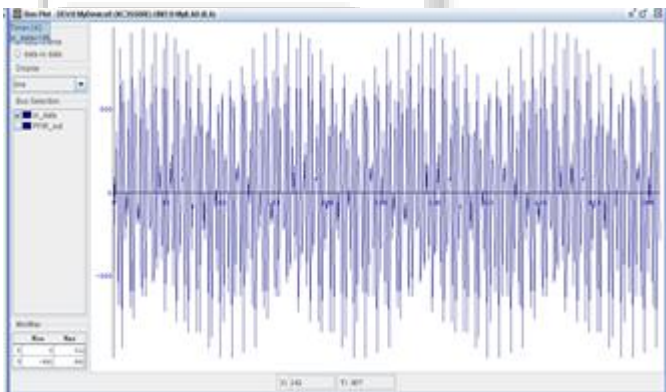


Fig. 17: 300KHZ*2MHZ signal

The below figure shows the output of the DDC. Note that the PFIR out check box is selected in the bus plot. It can be see that the output is only 300 KHz sin wave.

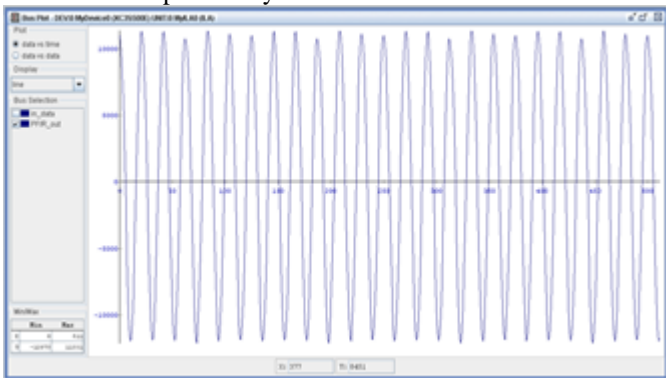


Fig. 18: PFIR output

V. CONCLUSION

The issues in designing digital down converter and up converter are studied. The main applications where DDC becomes the front end of software defined radio are understood. Two architectures; CIC based DDC and DUC are analyzed and implemented for FPGAs. VHDL generic coding style is followed to make the blocks highly configurable so that the same design with generic map can be configured for different decimation rates. Stability issues in realizing CIC filters are studied.

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