Compare "Urdhva Tiryakbhyam Multiplier" and "Hierarchical Array of Array Multiplier"

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Abstract—Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of high speed multiplier is increasing as the need of high speed processors are increasing. In this project, comparative study of different multipliers is done for high speed. The project includes two 4x4 bit Vedic Multiplier (VM) "Urdhva Tiryakbhyam multiplier" and "Hierarchical Array of Array Multiplier" of Ancient Indian Vedic Mathematics which are compared in terms of their speed. Urdhva Tiryakbhyam sutra increases the speed of multiplier by reducing the number of iterations then Hierarchical Array of Array Multiplier.

Keywords: Hierarchical array of array multiplier, Power Delay Product (PDP), Vedic Mathematics, Urdhva Tiryakbhyam.

I. INTRODUCTION

Vedic mathematics was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics and it can be applied to arithmetic, trigonometry, plain and spherical geometry, calculus.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. Digital multipliers are the core components of all the digital signal processors (DSPs) and the speed of the DSP is largely determined by the speed of its multipliers. These are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. Two most common multipliers followed in the digital hardware are array of array multipliers and Urdhva Tiryakbhyam multipliers. Hybrid architectures called „array of array" multipliers have intermediate performance. These multipliers have a time complexity better than array multipliers, and therefore becomes an obvious choice for higher performance multiplier

Urdhva Tiryakbhyam Sutra from Vedic mathematics is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products

In this paper, comparative study of different multipliers is done for low power requirement and high speed. The paper gives information of "Hierarchical" algorithm of Ancient Indian Vedic Mathematics which is utilized for multiplication to improve the speed, area parameters of multipliers. Vedic Mathematics also suggests more formulae for multiplication i.e. "Urdhva Tiryakbhyam" which can increase the speed of multiplier by reducing the number of iterations. Increasingly huge data sets and the need for low power in adders tend to increase. The traditional serial adders are no longer suitable for large adders because of its huge area and high power. All systems tends to trade off between speed and power. The computation time taken by the array multiplier is comparatively less.

II. DESIGN OF A 4X4 HIERARCHICAL MULTIPLIER

For design the 4 bit multiplier firstly we will find the different combinations of input bit pairs that are derived in terms of 2X2 multiplier. In 2 X 2 multiplier, which is the basic building block of hierarchical design for larger bit size multiplier?

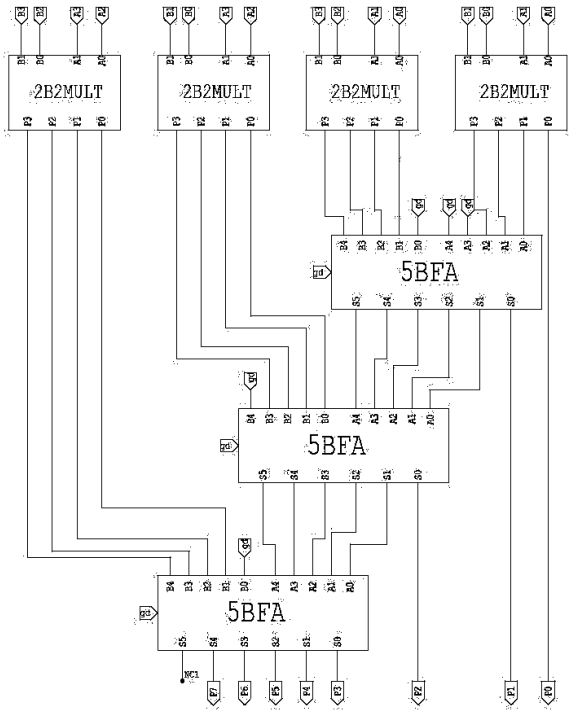

Fig. 1: Hierarchical 4X4 multiplier

A 2 X 2, combinational circuit can be realized using these equations.

P0 = A0.B0

P1=A0B1 (B0 + A1) + A1B0 (B1BAR + A1BAR) + A1B0 (B1BAR + A0BAR)

P2=A1B1 (A0BAR+B0BAR)

P3=A1B0B1B0

Each input bit-pair is handled by a separate 2X2 combinational multiplier to produce 4 partial product rows. These partial products rows are then added optimally to generate final product bits. Fig. 1 shows the schematic of a 4X4 combinational multiplier designed using 2X2 combinational multiplier. These partial products rows are then added optimally using 5-bit full adder cells.

III. DESIGN OF A 4X4 URDHVA TIRYAKBHYAM MULTIPLIER

Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. The Sanskrit term means "Vertically and crosswise". The idea here is based on a concept which results in the generation of all partial products along with the concurrent addition of these partial products in parallel [5]. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam explained in Fig. 2. Since there is a parallel generation of the partial products and their sums, the processor becomes independent of the clock frequency. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The advantage here is that parallelism reduces the need of processors to operate at increasingly high clock frequencies.

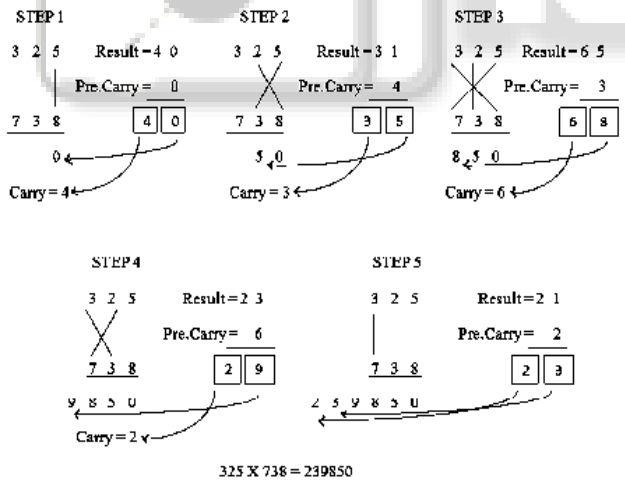

Fig. 2: Multiplication of two numbers using Urdhva Tiryakbhyam Sutra

A higher clock frequency will result in increased processing power, and its demerit is that it will lead to increased power dissipation resulting in higher device operating temperatures. By employing the Vedic multiplier, all the demerits associated with the increase in power dissipation can be negotiated. Since it is quite faster and efficient its layout has a quite regular structure. Owing to its regular structure, its layout can be done easily on a silicon chip. The Vedic multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers, thereby making it time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed.

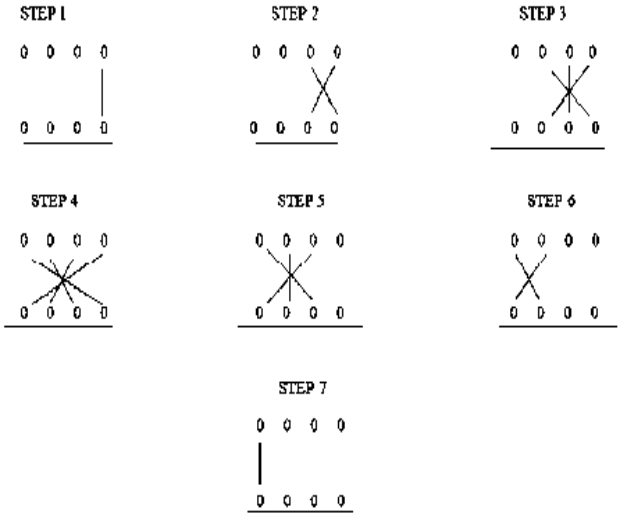

Fig. 3: Line diagram of the multiplication

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Fig.3. Initially the LSB digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and the process goes on likewise. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit act as the result digit and all other digits act as carry for the next step. Initially the carry is taken to be zero.

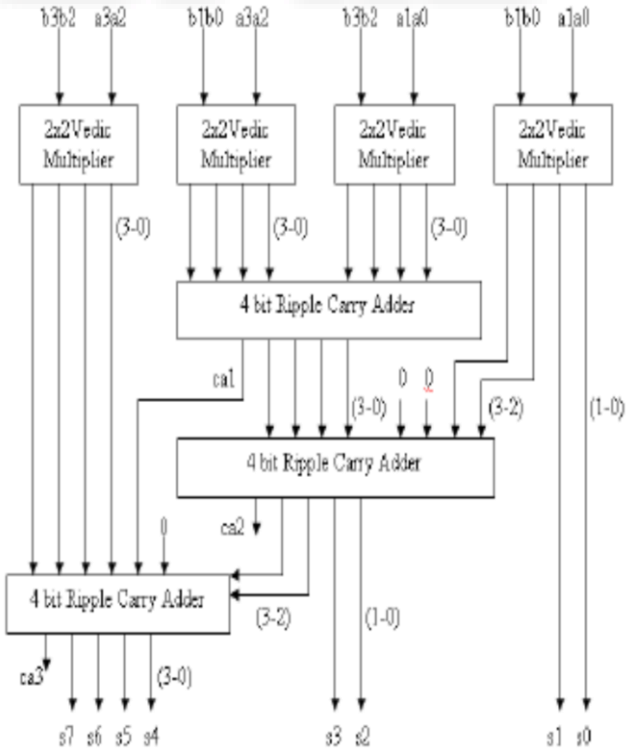

Fig. 4: Urdhva Triyagbhyam 4x4 multiplier

IV. COMPARISON AND SIMULATION RESULTS

A. *Implementation*

In this work two multipliers are compared,

1. A 4x4 bit Hierarchical Array of Array Multiplier is designed in VHDL (Very High Speed Integrated Circuits Hardware Description Language). Logic synthesis and simulation was done XilinxISE12.1i - Project Navigator and Active HDL. The performance of circuit is evaluated on the Xilinx device family Spartan3, package tq144 and speed grade -5. The RTL schematic of 4x4 bit Vedic multiplier comprises of four 2x2 bit Vedic multiplier M_1, M_2, M_3, M_4 and three 5-bit Ripple Carry Adder FA_i_1, FA_i_2, FA_i_3 while the simulation results obtained are shown in Fig. 9 for verification

2. A 4x4 bit Urdhva Triyagbhyam multiplier is designed in VHDL (Very High Speed Integrated Circuits Hardware Description Language). Logic synthesis and simulation was done XilinxISE12.1i - Project Navigator and Active HDL. The performance of circuit is evaluated on the Xilinx device family Spartan3, package tq144 and speed grade -5. The RTL schematic of 4x4 bit Vedic multiplier comprises of four 2x2 bit Vedic multiplier M_1, M_2, M_3, M_4 and three 4-bit Ripple Carry Adder FA_i_1, FA_i_2, FA_i_3,while the simulation results obtained are shown in Fig. 9 for verification.

B. *Comparative Result*

The synthesis result obtained from Urdhva Triyagbhyam is faster than Array of array multiplier. The device utilization summary of 4x4 bit Urdhva Triyagbhyam and Hierarchical Array of Array multiplier for Xilinx, Spartan family with device selected 3s50pq208-4 is shown below:

Sr. No		Total	Urdhva Triyagbhyam Multiplier		Hierarchical Array of Array Multiplier	
			Used	Percent Used	Used	Percent Used
1.	Number of Slices:	768	10	1%	13	1%
2.	Number of 4 input LUTs:	1536	17	1%	22	1%
3.	Number of bonded IOBs	124	16	12%	18	14%

Table 1: Device Utilization Summary

Comparison	Urdhva Triyagbhyam Multiplier	Hierarchical 4-4 Array of Array Multiplier
Path Delay(ns)	9.571	11.175

Table 2: Comparison of Hierarchical Multiplier and Urdhva Tiryakbhyam Multiplier

Table 1 shows the comparison of 4x4 bit Hierarchical Array of Array multipliers with Urdhva Triyagbhyam multiplier in terms of computational path delay in nanoseconds (ns). The timing result shows that Urdhva Triyagbhyam multiplier has the greatest advantage as compared to Hierarchical Array of Array multiplier in terms of execution time.

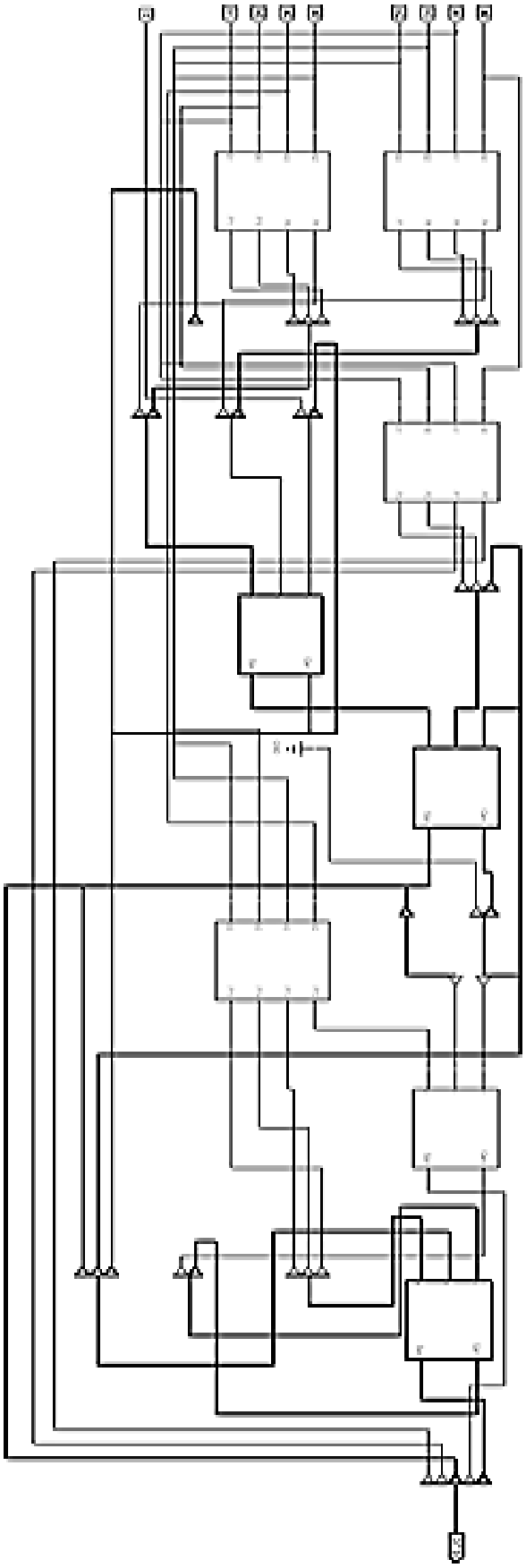

Fig. 7: RTL schematic for Hierarchical Multiplier

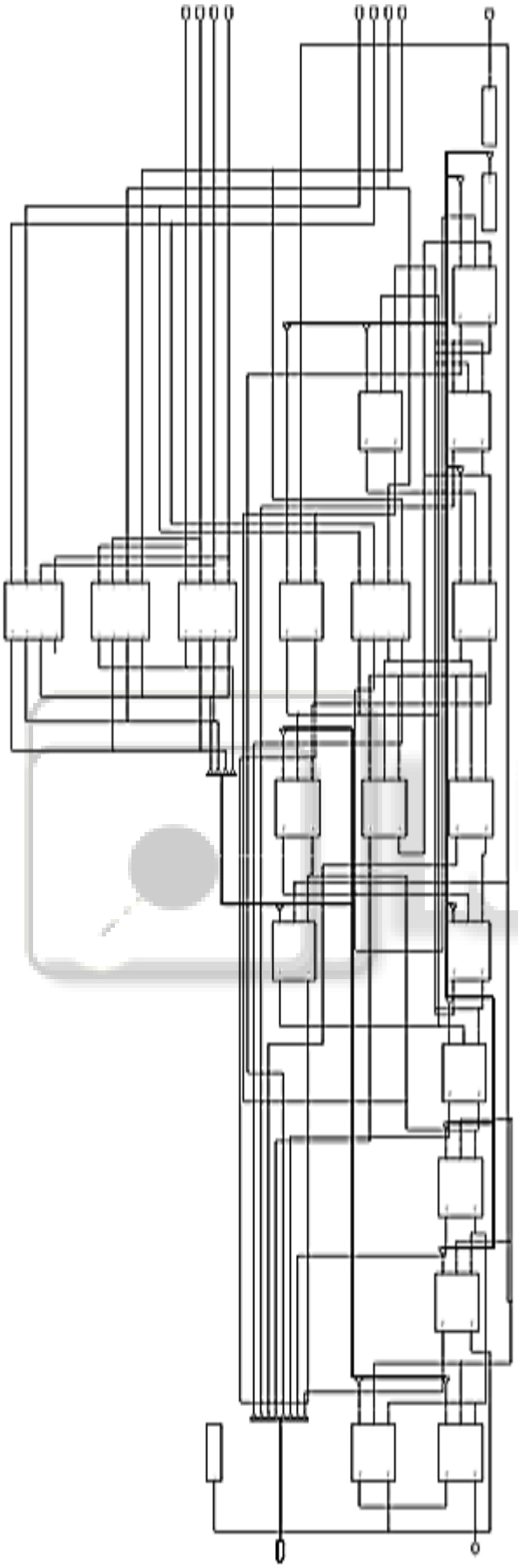

Fig 8: RTL schematic for Urdhva Triyagbhyam 4x4 Multiplier

V. SIMULATION

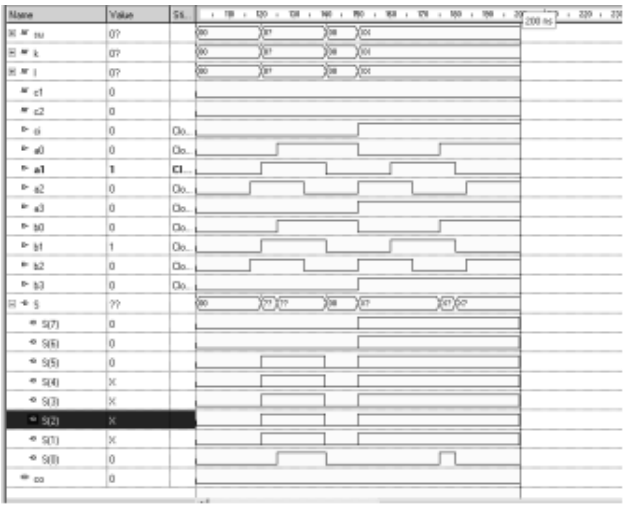

Fig. 9: Output for Hierarchical Multiplier

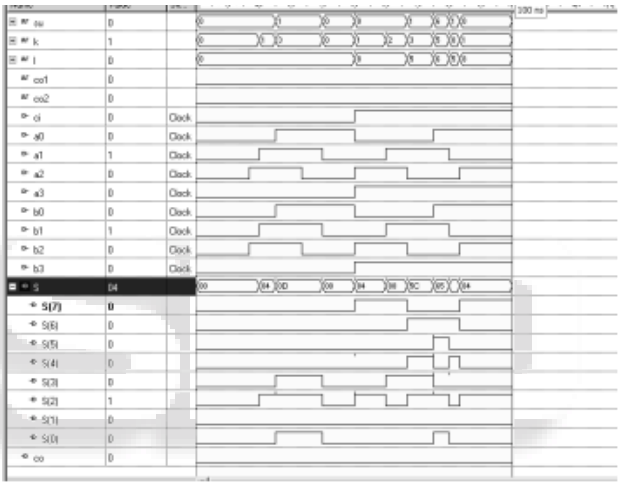

Fig. 10: Output for Urdhva Triyagbhyam 4x4 Multiplier

CONCLUSION

It can be concluded that Vedic Multiplier i.e. U.T smallest, fastest multiplier using low power. The U.T multiplier dominates other multipliers as number of bits increases in multiplication. In summary, the Power Delay in U.T multiplier is reduced by 28.84%, compare to HAM respectively. This is due to the hierarchical structuring & effectual addition of the partial product terms. If the bits in the multipliers are continuously increases to N X N (where N is any number) bits than the U.T multiplier showing better performance in compare to other multiplier on various performance factors

VI. REFERENCES

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