

Design of Efficient High Speed Vedic Multiplier

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ABSTRACT: -- Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. This paper proposed the design of high speed Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. The work has proved the efficiency of Urdhva Tiryagbhyam. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps. Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay for multiplication of all types of numbers, either small or large.

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. In the past, the parameters like high speed, small area and low cost were the major areas of concern, whereas power considerations are now gaining the attention of the scientific community associated with VLSI design [1]. Vedic mathematics was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics and it can be applied to arithmetic, trigonometry, plain and spherical geometry, calculus.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. Digital multipliers are the core components of all the digital signal processors (DSPs) and the speed of the DSP is largely determined by the speed of its multipliers. These are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. Two most common multipliers followed in the digital hardware are array of array multipliers and Urdhva Tiryakbhyam multipliers. Hybrid architectures called „array of array“ multipliers have intermediate performance. These multipliers have a time complexity better than array

multipliers, and therefore becomes an obvious choice for higher performance multiplier

Urdhva Tiryakbhyam Sutra from Vedic mathematics is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products

In this paper, comparative study of different multipliers is done for low power requirement and high speed. The paper gives information of “Hierarchical” algorithm of Ancient Indian Vedic Mathematics which is utilized for multiplication to improve the speed, area parameters of multipliers. Vedic Mathematics also suggests more formulae for multiplication i.e. “Urdhva Tiryakbhyam” which can increase the speed of multiplier by reducing the number of iterations. Increasingly huge data sets and the need for low power in adders tend to increase. The traditional serial adders are no longer suitable for large adders because of its huge area and high power. All systems tend to tradeoff between speed and power. The computation time taken by the array multiplier is comparatively less.

II. DESIGN OF VEDIC MULTIPLIER

Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. The Sanskrit term means “Vertically and crosswise”. The idea here is based on a concept which results in the generation of all partial products along with the concurrent addition of these partial products in parallel [2]. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam explained in Fig. 1. Since there is a parallel generation of the partial products and their sums, the processor becomes independent of the clock frequency. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The advantage here is that parallelism reduces the need of processors to operate at increasingly high clock frequencies. A higher clock frequency will result in increased processing power, and its demerit is that it will lead to increased power dissipation resulting in higher device operating temperatures. By employing the Vedic multiplier, all the demerits associated with the increase in power dissipation can be negotiated. Since it is quite faster and efficient its layout has a quite regular structure. Owing to its regular structure, its layout can be done easily on a silicon chip. The Vedic multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers, thereby making it time, space and power efficient.

It is demonstrated that this architecture is quite efficient in terms of silicon area/speed.

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Fig.2. Initially the LSB digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and the process goes on likewise. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit act as the result digit and all other digits act as carry for the next step. Initially the carry is taken to be zero.

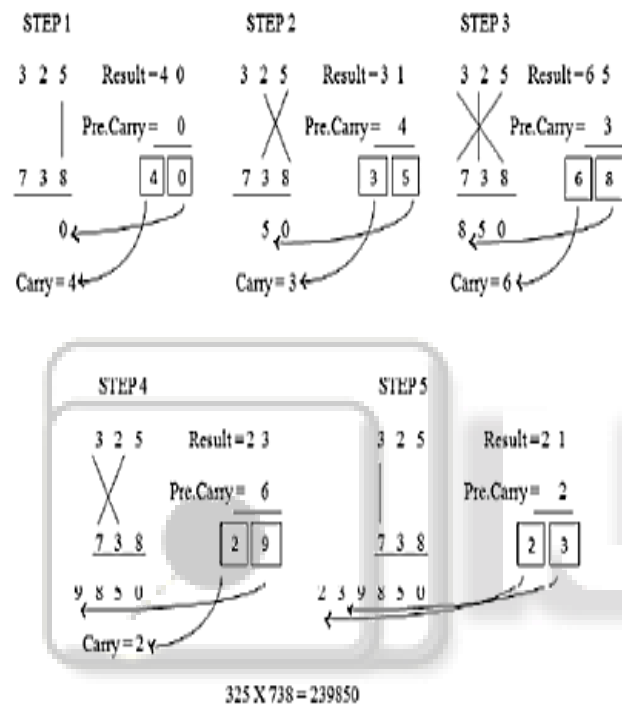


Fig. 1: Multiplication of two numbers using Urdhva Tiryakbhyam Sutra

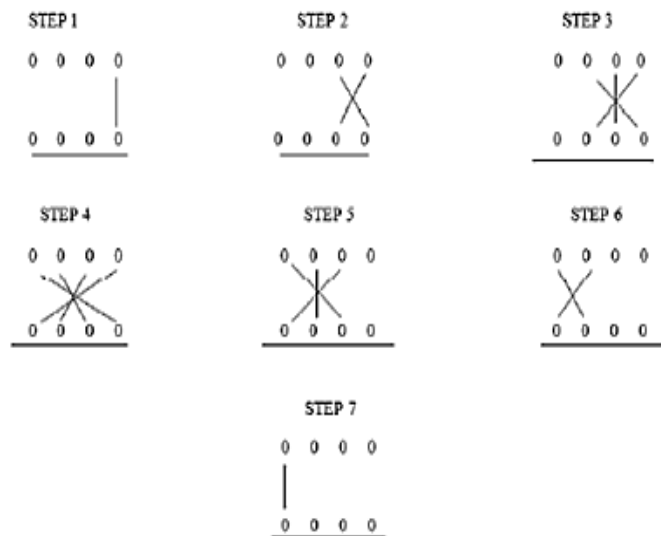


Fig. 2: Line diagram of the multiplication

A. Vedic Multiplier for 4x4 bit Module

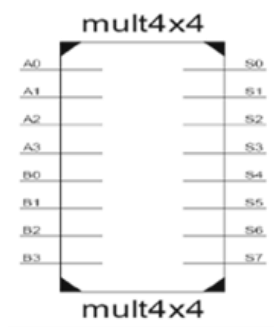


Fig. 3: Block Diagram of 4x4 bit Vedic Multiplier

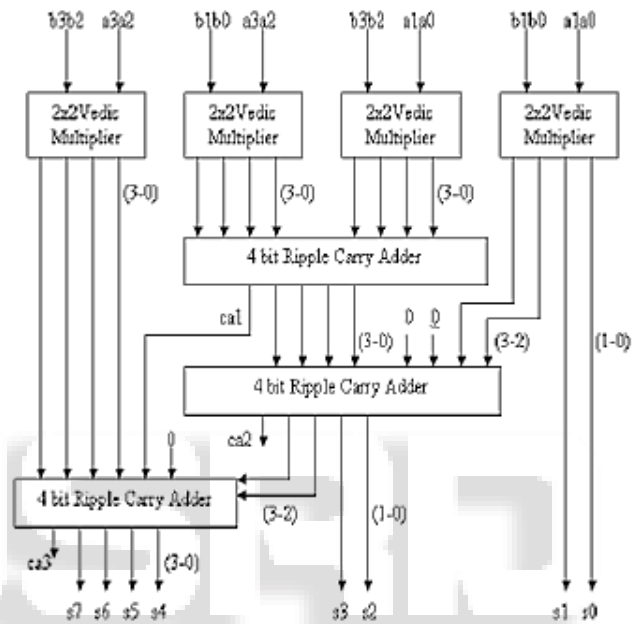


Fig. 4: Diagram of 4x4 bit Vedic Multiplier

Logic Utilization	Used	Available	Utilization
Number of Slices:	18	5888	0%
Number of 4 input LUTs:	32	11776	0%
Number of bonded IOBs	16	372	4%

Table 1: Device Utilization Summary of 4x4 bit

B. Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 4 can be easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section.

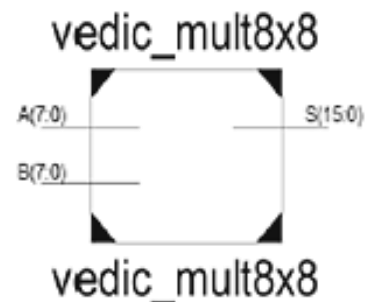


Fig. 5: Block Diagram of 8x8 bit Vedic Multiplier

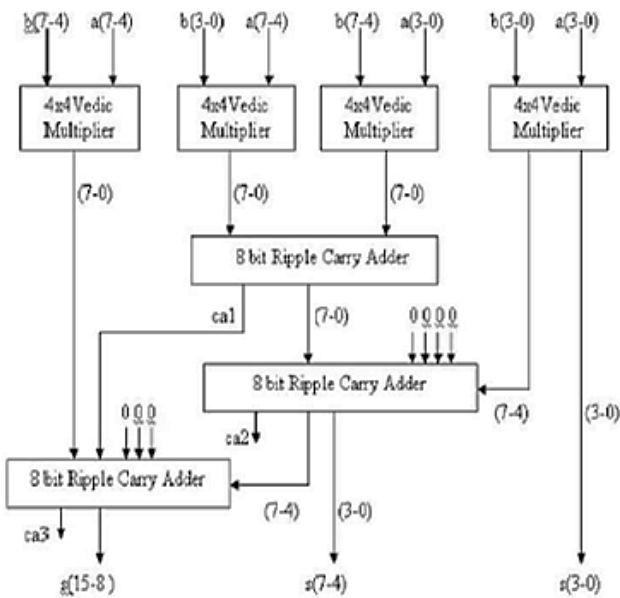


Fig. 6 Diagram of 8x8 bit Vedic Multiplier

C. Implementation Design for 8x8

Logic Utilization	Used	Available	Utilization
Number of Slices:	105	5888	1%
Number of 4 input LUTs:	180	11776	1%
Number of bonded IOBs	35	372	8%

Table 2: Device Utilization Summary of 8x8 bit

Simulation output of the 8x8 Multiplier For the value 8h and 7h gives a result in hexadecimal 38

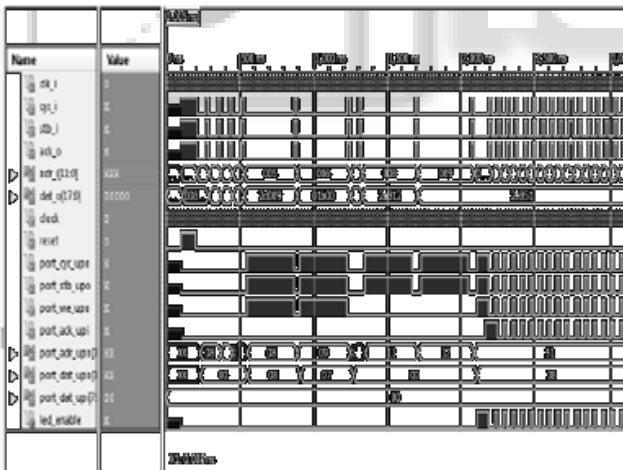


Fig. 7

III. CONCLUSION AND FUTURE WORK

This paper presents a highly efficient method of multiplication – “Urdhva Tiryakbhyam Sutra” based on Vedic mathematics. It is a method for hierarchical multiplier design which clearly indicates the computational advantages offered by Vedic methods. Authors implemented the code on Xilinx FPGA Spartan 3 board . The computational path delay for proposed 8x8 bit Vedic multiplier is found to be 30.27 ns. It is observed that the Vedic multiplier is much more efficient than Array and Booth multiplier in terms of

execution time (speed). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education.

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