VHDL Implementation of Flexible Multiband Divider

Arathy G. [1]
[1]M.Tech Student
[1]Mangalam College of Engg. , Ettumanoor, Kottayam

Abstract--In this paper an efficient multiband flexible divider for Bluetooth, Zigbee and other wireless standards is proposed based on pulse swallow topology and is implemented using Xilinx ISE 13.2 and modalism 6.4c.It consist of a propose wideband multimodulus 32/33/47/48 prescaler, swallow s-counter ,p-counter. As a modification I have implemented a modified multiband flexible divider by combining p and s counters together and by using a modified 2/3 prescaler. Compared to the proposed system modified one will reduce the circuit complexity, power consumption, gate counts etc.

I. INTRODUCTION

The demand for low cost, low power, and multiband RF circuits increased .Bluetooth is known as a short-range RF circuit. Compared to the conventional method the advantage of using multiband RF circuit is we can use a single RF circuit to support a variety of frequency bands which will help to reduce size and cost. In this paper a dynamic logic multiband flexible divider is proposed which uses a low power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler as shown in fig(1).The divider also uses an improved low power loadable bit cell for the swallow s-counter.

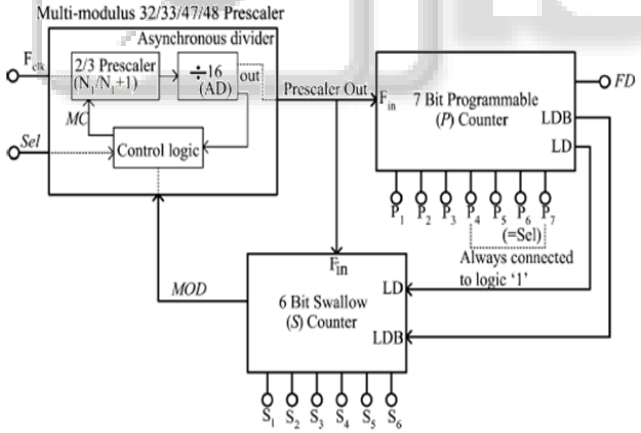


Fig. 1: Dynamic logic multiband flexible divider

II. EXISTING METHOD

In the proposed method I have implemented a dynamic logic multiband flexible divider. Frequency division is applicable for common wireless standards.

A. WIDEBAND E-TSPC 2/3 PRESCALER

The wideband single phase clock 2/3 prescaler used in this design consist of two D flip flops and two NOR gates as shown in fig(2).The first NOR gate is embedded in the last stage of DFF1 and the second NOR gate is embedded in the first stage of DFF2.

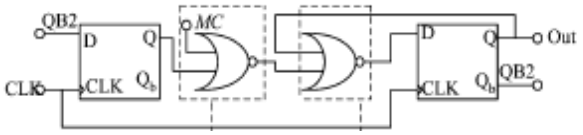


Fig. 2: Wideband single phase clock 2/3 prescaler

The switching of division ratios between 2 and 3 is controlled by logic signal MC. When MC switches from '0' to '1' the wideband 2/3 prescaler operates at the divide by 2 modes. This will remove the switching power contribution of DFF1.When logic signal MC switches from '1' to '0' ,the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of NOR gate embedded in DFF1 is '0' and the wideband prescaler operates at the divide by 3 mode.

B. MULTIMODULUS 32/33/47/48 PRESCALER

The wideband multimodulus prescaler can divide the input frequency by 32,33,47,48 is shown in fig(4).The proposed prescaler performs additional divisions(divide by 47 and divide by 48)without any extra flip-flop, thus saving a considerable amount of power and also it will reduce circuit complexity. The multimodulus prescaler consist of a wideband 2/3(N1/N1+1) prescaler ,four asynchronous TSPC divide by 2 circuits(AD=16) and combinational logic circuits to achieve multiple division ratios.

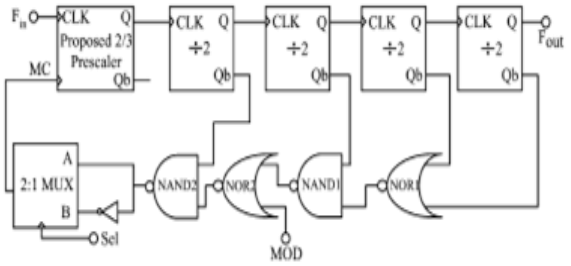


Fig. 4: Proposed multimodulus 32/33/47/48 prescaler

In addition to the MOD signal for controlling N1/(N1+1) divisions, additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.

1) Case 1: Sel='0'

When Sel='0', the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler and the division ratio is controlled by MOD signal. If MOD='1',the NAND2 gate output switches to logic '1'(MC=1)and the wideband prescaler operates in the divide by 2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

$$N = (AD * N1) + (0 * (N1 + 1)) = 32$$

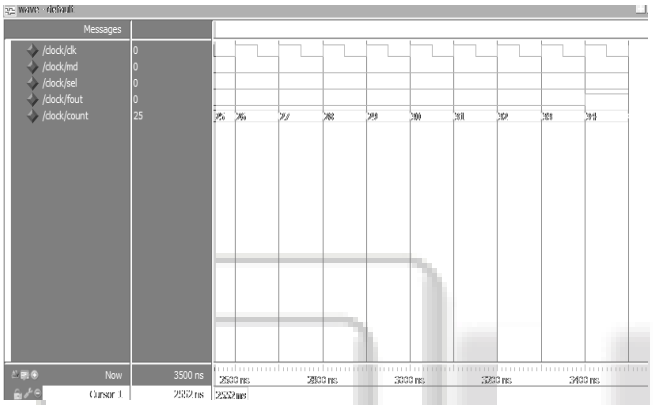
Where N1=2 and AD=16 is fixed for the entire design. If MOD=0, wideband prescaler operates in the divide by 3

mode for three input clock cycles. The division ratio N+1 performed by the multimodulus prescaler is
N+1=((AD-1)*N1)+(1*(N1+1))=33

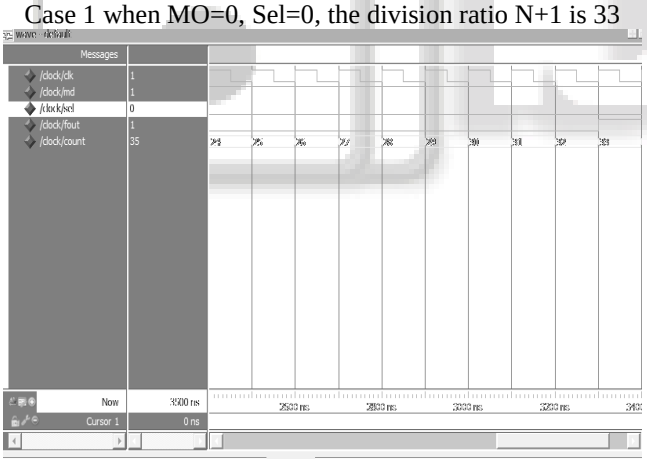
2) Case 2: Sel='1'

When Sel=1,the inverted output of NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. In this case the operation is quite opposite to the previous case. When MOD=1, and Sel=1, the division ratio is
N+1=(AD*(N1+1))+(0*N1)=48
If MOD=1, the division ratio N performed by the multimodulus prescaler is
N= ((AD-1)*(N1+1))+(1*N1)=47

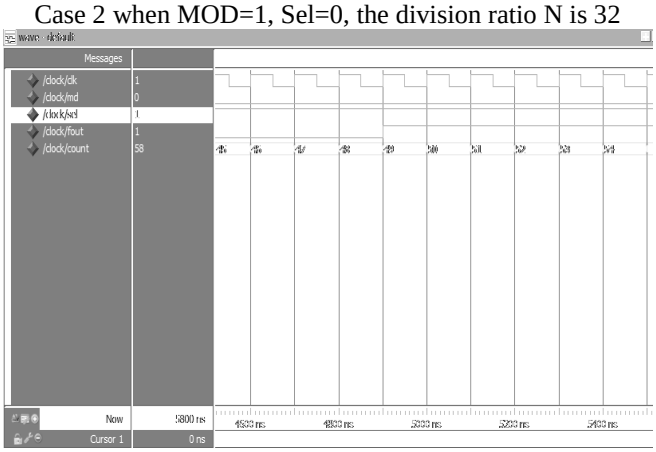
C. SIMULATIONS OF MULTIMODULUS PRESCALER



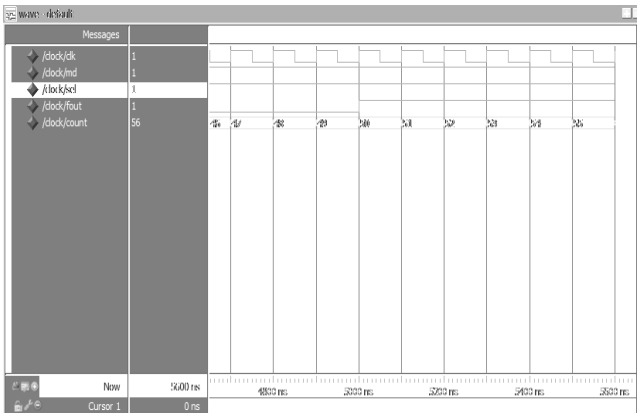
Case 1 when MO=0, Sel=0, the division ratio N+1 is 33



Case 2 when MOD=1, Sel=0, the division ratio N is 32



Case 3 when MOD=0, Sel=1,the division ratio N is 47



Case 4 when MOD=1,Sel=1,then division ratio N+1 is 48

D. MULTIBAND FLEXIBLE DIVIDER

Dynamic logic multiband flexible divider shown in fig(1) consist of the multimodulus 32/33/47/48 prescaler, a 7-bit programmable p-counter and a 6 bit swallow s-counter

E. SWALLOW S COUNTER

The 6 bit s counter shown in fig(5) consist of six asynchronous loadable bit cells, a NOR embedded DFF and additional logic gates. If MOD is logically high nodes s1 and s2 switches to logic 0 and the bit cell does not perform any function. The MOD signal goes logically high only when the s-counter finishes counting down to zero.

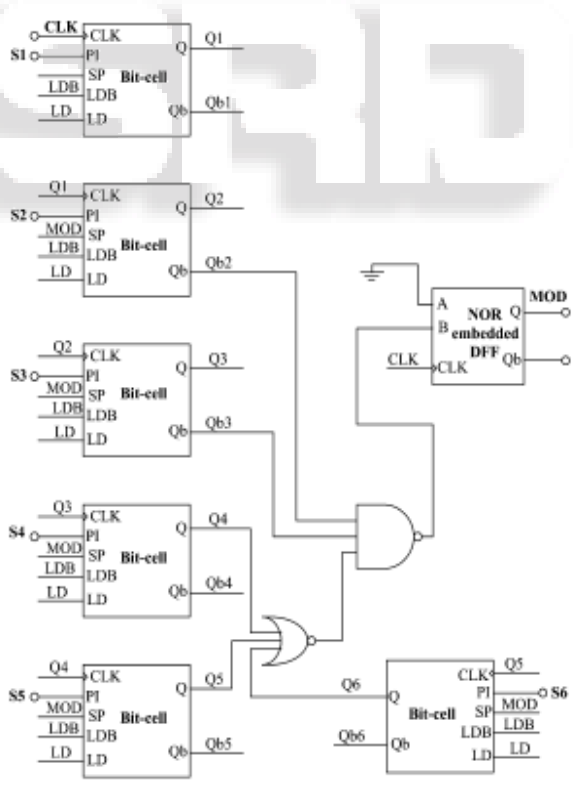


Fig. 5. Asynchronous 6-bit S-counter.

Fig. 5: Asynchronous S counter

In the initial state, MOD=0, multimodulus prescaler selects the divide by (N+1) mode and p, S counter start down counting the input clock cycles. When the s counter finishes counting, MOD switches to logic 1 and the prescaler changes to divide by N mode for the remaining clock cycles

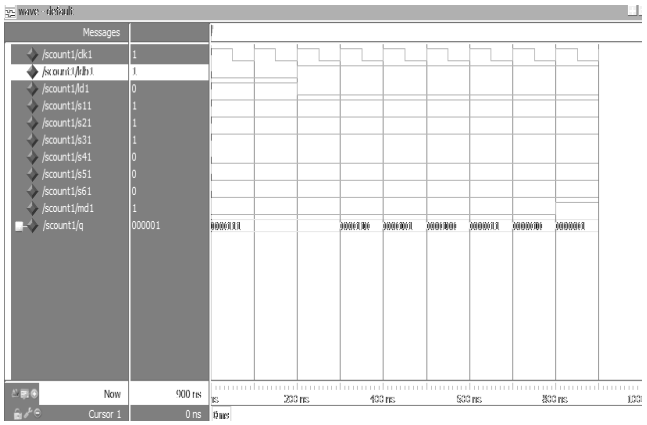


Fig. 6: Swallow S Counter

F. PROGRAMMABLE P COUNTER

It is a 7 bit down counter consists of 7 loadable bit cells and additional logic gates. When the p counter finishes counting down to neither zero, LD switches to logic 1 at which output of all bit cells in s counter switches to logic 1 and the output of NOR embedded DFF switches to logic zero where the divider reset to its initial state and so a fixed division ratio is achieved.

When Sel=0,the multimodulus prescaler act as 32/33 prescaler, the p counter is programmable from 64 to 127 and the s counter is programmable from 0 to 31 to accommodate division ratios from 2048 to 4095.The frequency division ratio of the multiband divider in this mode is given by

FD=(N+1)*S+N*(P-S)=NP+S2)

When logic signal Sel=1,the multimodulus prescaler act as 47/48 prescaler, the p counter is programmable from 64 to 127,and the s counter is programmable from 0 to 48 to accommodate division ratios from 3024 to 6096.The frequency division ratio is

FD=(N*S)+(N+1)*(P-S)=(N+1)P-S

G. SIMULATION OF P COUNTER

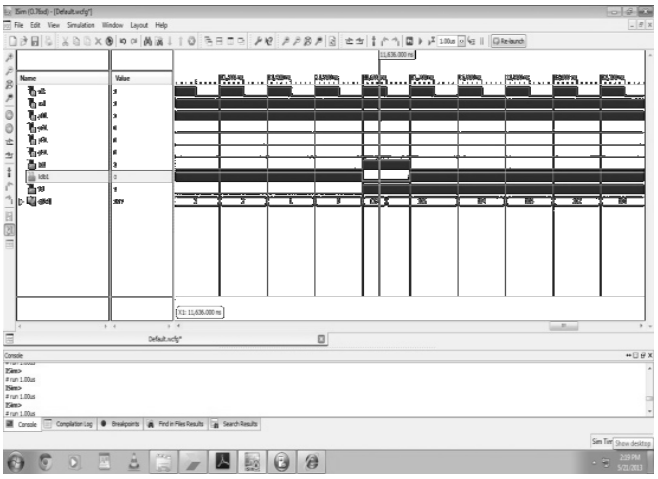


Fig. 7: Simulation of P Counter

H. SIMULATION OF PROPOSED DYNAMIC LOGIC MULTIBAND FLEXIBLE DIVIDER

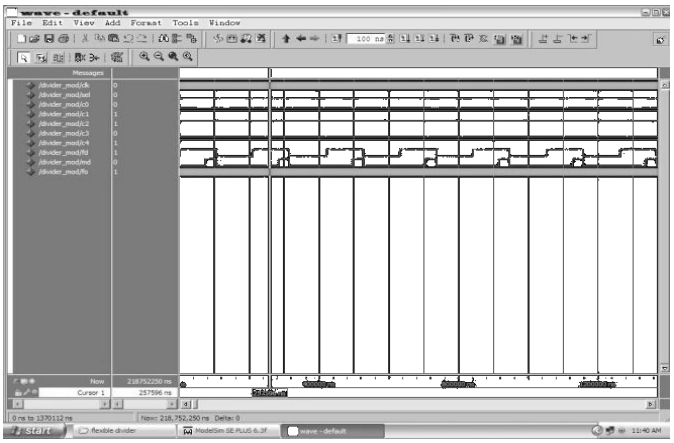


Fig. 8: Simulation of Proposed Dynamic Logic Multiband Flexible Divider

I. MODIFIED MULTIBAND FLEXIBLE DIVIDER

1) Integrated P&S Counter

We have replaced P counter and S counter with an integrated P&S counter. This counter consists of a divide-by-64 (P counter) that is made up of 6 divide-by-2. Digital circuit consists of XNOR gates (X 0 - X4), AND gates (A 0, A 1) and a RESET- SET Flip Flop (RSFF). This digital section has replaced S counter in conventional ones and has the duty to control modulus bit of dual modulus prescaler. When we integrate p and s counters performance of the divider can be improved.

2) Proposed Divide-By-2/3 Counter Design

Neither in the proposed counter design NOR gate is replaced with AND gate and PMOS which Is actually a switch. When the switch is open, input from FF1 is disconnected and FF2 alone divide the clock frequency by 2.

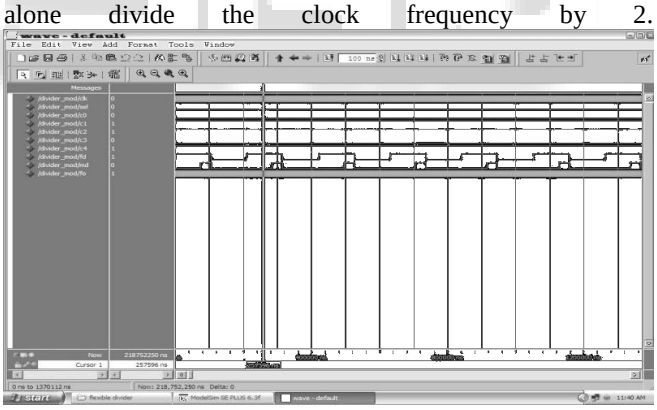


Fig. 9: Proposed Divide-By-2/3 Counter Design

CONCLUSION

In this paper, a multiband flexible divider is implemented which consist of a consist of program counter; swallow s counter and multimodulus prescaler. It is simulated by using modalism 6.4c.This type of divider is widely used in Bluetooth, Zigbee technologies which are the common wireless standards .A modified divider is also implemented in this paper by integrating p and s counters in the existing system to achieve high performance, to simplify the circuit etc. Also in the modified flexible divider existing 2/3 prescaler is replaced with modified 2/3prescaler which consist of an AND gate and PMOS. By the implementation of modified divider we can achieve reduced power consumption,

REFERENCES

[1]P. Y. Deng et al., "A 5 GHz frequency synthesizer with an injection locked frequency divider and differential switched capacitors," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 2, pp. 320–326, Feb 2009.
[2]L. Lai Kan Leung et al., "A 1-V 9.7-mW CMOS frequency synthesizer for IEEE 802.11a transceivers," IEEE Trans. Microw. Theory Tech., vol. 56, no. 1, pp. 39–48, Jan. 2008

