Designing PCI/AHB Bridge

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Abstract— The PCI Local Bus is a bus having features like high performance, 32-bit or 64- bit bus with multiplexed address and data lines. The AHB of AMBA (Advanced Microcontroller Bus Architecture) is also for high-performance, high clock frequency system modules. In SoC design the AMBA AHB acts like the high-performance system backbone bus. The function of AHB-PCI Bridge is to map various control signals and address spaces from one bus into those of another bus. This paper presented the AHBPCI bridge designing.

Keywords: PCI, AHB, PCI-AHB BRIDGE, BRIDGE

I. INTRODUCTION

Before PCI old buses like VLbus were used to connect peripheral components but, during 90's there were huge development in Graphical user interface (GUI) and multimedia so old bus architecture became the bottleneck. The computer's developing high-performance needed the relevant rapid bus to complete the transaction. PCI local bus met the need.

The AMBA AHB is a new generation bus, which was released by ARM Ltd. It is for high-performance, high clock frequency system modules. The AMBA AHB acts like the high-performance system backbone bus. AHB supports the efficiently in connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral microcells functions. AHB is also specified to ensure ease of use in an efficient design flow using synthesis and automated test techniques.

This paper is to design PCI/AHB Bridge which connects the SoC platform with peripheral components based on PCI Bus.

II. PCI/AHB BRIDGE ARCHITECTURE

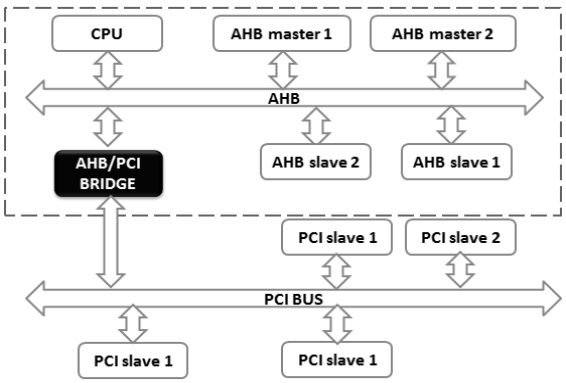

Fig. 1: PCI/AHB Bridge

The AHB/PCI Bridge allows transaction between a master on PCI (AHB) and a target on AHB (PCI). The role of PCI/AHB Bridge is to transfer address, data and commands between the devices. According to the function of AHBPCI bridge, it should be AHB master as well as AHB slave, furthermore it also should be PCI master and PCI slave.

Figure 1 illustrates a simple PCI/AHB bridge topology, here components in the dotted line in Figure 1 compose the SoC platform.

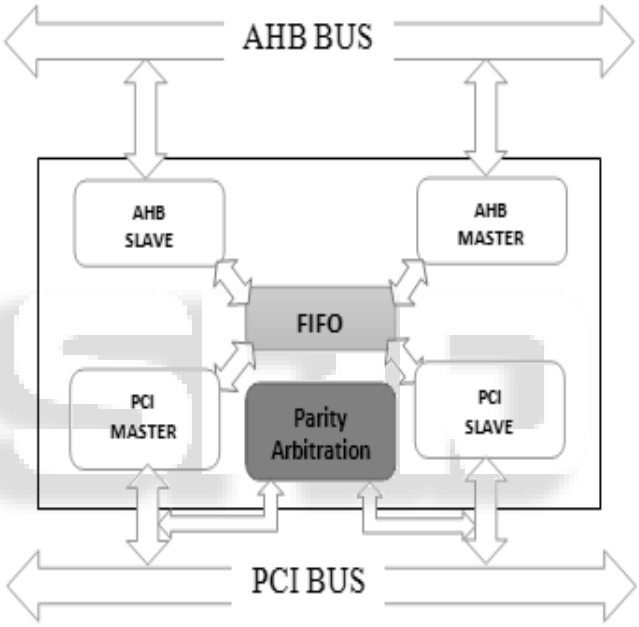

Fig. 2: PCI/AHB Bridge Component Architecture

To make the transaction possible between PCI and AHB interface, PCI/AHB Bridge must at least have the components which are shown in the high level architecture drawing in Figure 2.

III. PCI/AHB BRIDGE FEATURES

PCI/AHB Bridge can perform four basic transactions

1) PCI master read from AHB slave
2) AHB master read from PCI slave
3) PCI master write to PCI slave
4) PCI master write to AHB slave

In order to meet the system performance, Asynchronous FIFOs should be implemented in the Bridge. The key of PCI/AHB Bridge is the FIFO Design.

The case of PCI master on PCI bus reading (writing) from (to) AHB slave on AHB bus is similar to AHB master on AHB bus reading (writing) from (to) PCI slave on PCI bus.

IV. PROCESS OF READ AND WRITE TRANSACTION

A. Read Transaction Process

1) The process of PCI master on PCI bus reads from AHB slave that is on AHB bus is:

2) The PCI master on PCI bus initiates the read transaction and the PCI slave of the bridge encodes PCI command to AHB command.

3) The PCI slave of the bridge samples the beginning address of the read transaction and put it on AHB through the AHB master of the bridge.

4) The AHB master of the bridge requires the AHB ownership and prepares to begin the read transaction.

5) When AHBPCI Bridge gets the ownership, the read pre-fetch buffers begins to store the data from the AHB slave on AHB bus. There're two sets of read pre-fetch buffers in this design. The first one(Bl) and the second one (B2), Bl stores the data first. When B1 is full, the B2 begin storing data.

6) B1 transfers the data stored in it to the PCI master on PCI bus. Before B1 is empty, B1 can't restore other data. When B1 is empty, it should assert it is empty and prepare to store the next data group, at the same time, B2 begin to transfer the data stored in it to the PCI master, just like B1.

7) If one of B1 and B2 is empty, the one will store the data from AHB. If both B1 and B2 are full, or one is full and the other is transferring the data in it to the PCI master, AHBPCI should stop storing and enter the wait state until the transferring one's data is empty and begin the next storage.

It is similar that the process of AHB master on AHB bus read from PCI slave on PCI bus.

B. Write Transaction Process

The process of PCI master on PCI bus writes to AHB slave that is on AHB bus is:

1) The PCI master on PCI bus initiates the write transaction and the PCI slave of the bridge encodes the command.

2) There're two sets of write posting buffers, the first one (WB1) and the second one (WB2). If the PCI slave of the bridge can response the PCI master,WB1 stores the data first, when WB1 is full, theWB2 begin storing data.

3) When WB1 is full, the AHB master of the bridge requires the AHB ownership and prepares to begin the write transaction.

4) When AHBPCI Bridge gets the ownership, WB1 transfers the data stored in it to AHB slave according to the address. Before WB1 is empty, it can't restore other data. When WB1 is empty, it should assert it is empty and prepare to store the next data group. At the time of WBl is empty, ifWB2 is full, WB2 begin to transfer data, if not, and AHBPCI Bridge will enter wait state until WB2 is full.

5) If one of WBl and WB2 is empty, the one will begin to store the data from PCI. If both of WB1and WB2 are full, or one is full and the other is transferring the data in it to AHB slave, AHB PCI-Bridge should wait until there's an empty one, then the bridge will begin the next storage.

The process of AHB master on AHB bus writes to PCI slave that is on PCI bus is similar.

V. COMPARISON

A. Read Transaction

Though PCI master on PCI bus reads AHB slave that is on AHB bus is similar to AHB master on AHB bus reads PCI slave that is on PCI bus, there're some differences between them yet.

The "burst transfer" concept in PCI protocol is different from that of AHB protocol. In PCI protocol, a "burst transfer" is one consisting of a single address phase followed by two or more data phases. In AHB protocol, there're two different forms of burst transfers, one is incrementing bursts, the other is wrapping burst. Figure3 Illustrates PCI burst transfer. Figure4 illustrates AHB burst transfer.

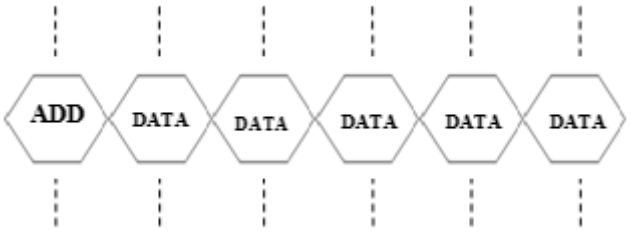

Fig. 3: PCI Burst Transfer

Fig. 4: AHB Burst transfer

Refer to Figure 3 and Figure 4, in PCI protocol only the first address is needed for the whole transaction, but in AHB protocol every address for the data phases is needed. Especially, in AHB protocol, the addresses in wrapping burst are wholly different from that of PCI.

Briefly, when PCI master on PCI bus reads AHB slave that is on *AHB* bus, the AHB master of the bridge only needs to transfer the first address which is from the PCI master and the data phases, and the burst type is incrementing burst of AHB protocol. When AHB master on AHB bus reads PCI slave that is on PCI bus, the PCI master of the bridge needs to calculate the first address of the data phases, then begins the transaction on PCI bus.

When PCI master reads, the pre-fetch buffers store the data from the AHB slave in turns according to the first address and the incrementing of the address. But when AHB master reads, the pre-fetch buffers will store data from the PCI slave according to the AHB master's control signals, address and the size of the data. It's obvious that the transform of the AHB master reads is more complex.

B. Write Transaction

During write process, the data storing is easier than that of read process. This is because read transaction need to deal with the control signals first, then the data will be read into the buffers. When the master device on the bus (PCI master

or AHB master) writes to slave device that is on another bus (Am slave or PCI slave), the data first to be written into the write posting buffers, then the buffers transfer the data to the slave device.

When PCI master on PCI bus writes to AHB slave that is on AHB bus, the write posting buffers store the data from the first one of the buffers in succession. But when AHB master does write transaction, the first data will be stored in one buffer according to the control signals of the AHB master, and the storing sequence will change with the AHB control signals.

VI. CONCLUSION

This paper finishes the model of PCI/AHB Bridge at RTL level, and the presented model is synthesized by Synopsys software using 0.90nm CMOS library. The AHB system clock (HCLK) is 100MHz; the PCI system clock (CLK) is 33MHz.

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