Design and Simulation Low power SRAM Circuits

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Abstract—(SRAMs), focusing on optimizing delay and power. As the scaling trends in the speed and power of SRAMs with size and technology and find that the SRAM delay scales as the logarithm of its size as long as the interconnect delay is negligible. Non-scaling of threshold mismatches with process scaling, causes the signal swings in the bitlines and data lines also not to scale, leading to an increase in the relative delay of an SRAM, across technology generations. Appropriate methods for reduction of power consumption were studied such as capacitance reduction, very low operating voltages, DC and AC current reduction and suppression of leakage currents to name a few.. Many of reviewed techniques are applicable to other applications such as ASICs, DSPs, etc. Battery and solar-cell operation requires an operating voltage environment in low voltage area. These conditions demand new design approaches and more sophisticated concepts to retain high device reliability. The proposed techniques (USRS and LPRS) are topology based and hence easier to implement.

Keywords: LPRS, SRAM, SNM, Sense amplifiers (SA), UPRS

I. INTRODUCTION

The stability of embedded Static Random Access Memories (SRAMs) is a growing concern in the design and test community [1, 2, 3]. Maintaining an acceptable Static Noise Margin (SNM) in embedded SRAMs while scaling the minimal feature sizes and supply voltages of the Systems-on-a-Chip (SoC) becomes increasingly challenging. The increased process spreads of modern scaled-down technologies and non-catastrophic defect-related sensitivity to environmental parameters can cause stability degradation in SRAMs [4]. Moreover, the minimal feature sizes of SRAM cell transistors combined with the high packing density of SRAM arrays, often involving relaxed design rules, aggravate this problem. The static noise margin (SNM) can serve as a figure of merit in evaluation of the stability of SRAM cells. Due to various factors the SNM of even defect free cells is declining with scaling. In the presence of non-catastrophic defects such as poor vias and contacts, cell stability is degraded even further. However, such defective cells can still escape the standard functional tests (e.g., march tests).

International Technology Roadmap for Semiconductors (ITRS)-2003 [5, 6] predicts "greater parametric yield loss with respect to noise margins" for high density circuits.

The growing gap between the Micro Processor Unit (MPU) cycle time and DRAM access time necessitated the introduction of several levels of caching in modern data processors. In personal computer MPUs such levels are often represented by Ll and L2 on-chip embedded SRAM cache memories. As the speed gap between MPU, memory and mass storage continues to widen, deeper memory hierarchies have been introduced in high-end server microprocessors [7].

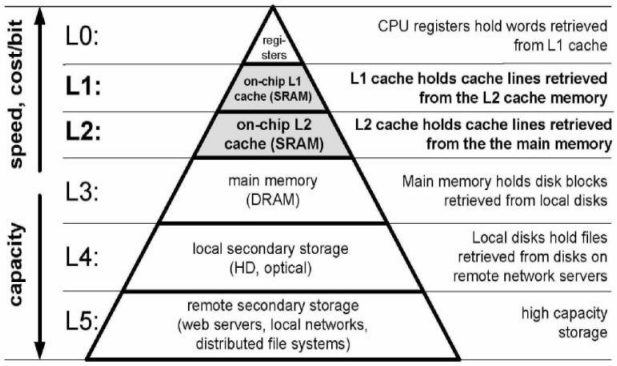

Fig 1: Computer memory hierarchy.

II. SRAM DESIGN AND OPERATION

A. *SRAM Block Structure*

Figure 2 shows an example of the basic SRAM block structure. A row decoder gated by the timing block decodes X row address bits and selects one of the word lines WL_O-WL_N- 1. If an SRAM array of N rows and M bits is arranged in a page manner, an additional Z-decoder activates the accessed page. Figure 2 shows an example with four pages of NxM arrays with the corresponding I/O circuitry.

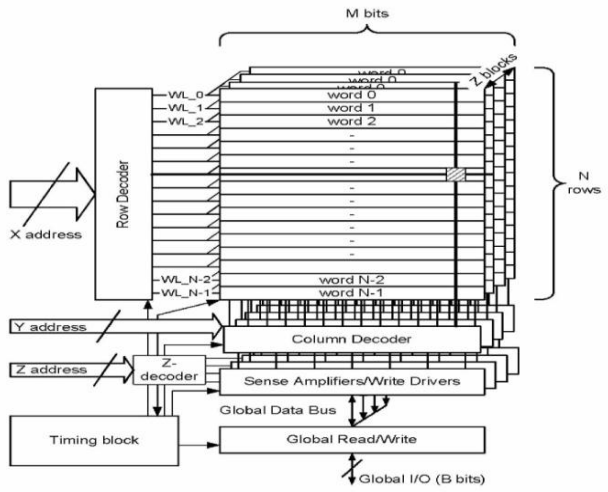

Fig 2: SRAM block diagram

Memories can be bit-oriented or word-oriented. In a bit-oriented memory, each address accesses a single bit. Whereas in a word-oriented memory, a word consisting of ti (where the popular values of ti include 8, 16, 32 or 64) bits is accessed with each address. Column decoders or column

MUXs (YMUX) addressed by Y address bits are often used to allow sharing of a single sense amplifier among 2, 4 or more columns. Most of modern SRAMs are self-timed, i.e. all the internal timing is generated by the timing block within an SRAM instance. An additional Chip Select (CS) signal, introducing an extra decoding hierarchy level, is often provided in multi-chip architectures.

B. *The SRAM CELL*

Memory cells are the key components of any SRAM serving for storage of binary information. A typical SRAM cell is comprised two cross-coupled inverters forming a latch and access transistors. Access transistors enable read and write access to the cell and cell isolation for the not-accessed state. An SRAM cell has to provide non-destructive read access, write capability and infinite storage (or data retention) time provided the power is supplied to the cell. Hierarchically, memory cells are arranged in cores, which can be further divided into blocks and arrays depending on the system speed and power requirements.

There are three more recent SRAM cells: a resistive load four-transistor (4T) SRAM cell, a six-transistor (6T) CMOS SRAM cell and a loadless 4T SRAM cell. We will consider a six-transistor (6T) CMOS SRAM cell and will then discuss its advantages and disadvantages. The cell design considerations represent a tradeoff between cell area, robustness, speed and power. Cell size minimization is one of the most important design objectives.

C. *6T CMOS SRAM Cell*

The mainstream six-transistor (6T) CMOS SRAM cell is shown in Figure 3. Similarly to one of the implementations of an SR latch, it consists of six transistors. Four transistors *(Ql - Q4)* comprise cross-coupled CMOS inverters and two NMOS transistors Q5 and Q6 provide read and write access to the cell. Upon the activation of the word line, the access transistors connect the two internal nodes of the cell to the true (BL) and the complementary (BLB) bit lines.

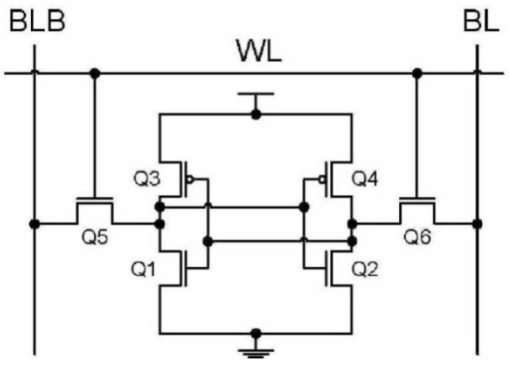

Fig 3: Six-transistor (6T) CMOS SRAM cell.

An SRAM cell has to provide a non-destructive read and a quick write - the two opposing requirements, which impose constraints on the cell transistor currents governed by their transistor sizing.

1) *Read Operation*

The read operation is stared by enabling the word line (WL) and connecting the precharged bit lines, BL and BLB, to the internal nodes of the cell. Upon read access, the bit line voltage V_{BL} remains at the precharged level equal V_{DD}. The complementary bit line voltage V_{BLB} is discharged through transistors Ql and Q5 connected in series (Figure 4). Effectively, transistors Ql and Q5 form a voltage divider whose output is connected to the input of inverter Q2 - Q4 in Figure 3. Sizing of Ql and Q5 should ensure that inverter Q2 - Q4 does not switch causing a read upset. In other words, 0 +, 6. *V* should be less than the switching threshold of inverter Q2 - Q4 plus some *safety margin* or *Noise Margin*

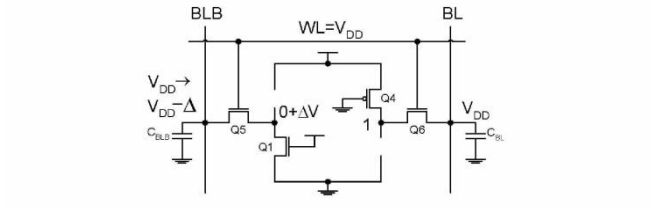

Fig 4: Simplified model of a 6T CMOS SRAM cell during a read operation.

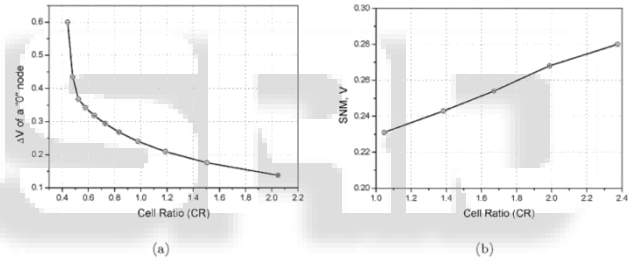

Fig 5: **The rise ΔV of the "0" node (a) and the SNM (b) as a function of the Cell Ratio (CR) $\left(CR = \frac{W_1}{L_1}/\frac{W_5}{L_5} = \frac{W_2}{L_2}/\frac{W_6}{L_6}\right.$ in Figure 2.3$\left.\right)$ in a 6T CMOS SRAM cell (simulated in CMOS 0.13μm technology, V_{DD}=1.2V).**

Ignoring the short-channel and body effects, the maximum allowed value $0+\Delta V$ of the "0" node during read access can be expressed as [3]:

$$\Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{THn}) - \sqrt{V_{DSATn}^2(1+CR) + CR^2(V_{DD} - V_{THn})^2}}{CR} \quad (2.1)$$

where CR (a.k.a. β) is the cell ratio defined as

$$CR = \frac{W_1/L_1}{W_5/L_5} \quad (2.2)$$

One and can be varied depending on the target application of the cell from approximately 1 to 2.5. Larger *CRs* provide higher read current $\mathbf{I_{read}}$ (and hence - the speed) and SNM (see Figure 5(b)) at the expense of larger area taken by the driver transistors Q1 and *Q2.* Whereas smaller *CRs* make for a more compact cell with moderate speed and noise margins. Both for ensuring cell stability and reducing the leakage current of the access transistors, a preferred sizing solution is to use a minimum width with a slightly larger than minimal length access transistors and a larger than minimal width with a minimal length driver transistors.

Once the complementary bit line voltage V_{BLB} has been discharged to a certain V_{DD} -, 6. sufficient for reliable sensing by the sense amplifier, the sense amplifier is enabled and amplifies the small differential voltage between the bit lines to the full-swing CMOS level.

2) *Write Operation*

The write operation is similar to resetting an SR latch. One of the bit lines, e.g., BL in Figure 6, is driven from precharged value *(V_{DD})* to the ground potential by a write driver through transistor *Q6.* If transistors Q4 and Q6 are properly sized, then the cell is flipped and its data is effectively overwritten. Note that the write operation is applied to the node storing a "1". This is necessitated by the non-destructive read constraint that ensures that a "0" node does not exceed the switching threshold of inverter Q2 - *Q4.* The function of the pull-up transistors is only to maintain the high level on the "I" storage node and prevent its discharge by the off-state leakage current of the driver transistor during data retention and to provide the low-to-high transition during overwriting.

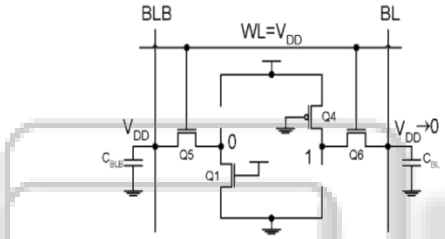

Figure 6 Simplified model of a 6T CMOS SRAM cell during a write operation

Assuming that the switching will not start before "1" node is below V_{TH-Q1} a simplified overwrite condition can be expressed as [3]

$$V_{"1"} = V_{DD} - V_{THn} - \sqrt{(V_{DD} - V_{THn})^2 - 2\frac{\mu_p}{\mu_n} PR\left((V_{DD} - |V_{THp}|)V_{DSATp} - \frac{V_{DSATp}^2}{2}\right)}$$

where the pull-up ratio of the cell, PR, is defined as:

$$PR = \frac{W_4/L_4}{W_6/L_6} \quad (2.4)$$

The $V_{"1"}$ requirement is easily met using minimal-sized access and pull-up transistors only due to μ_n/μ_p ratio. Simulation results shown in Figure 2.7 demonstrate that for a normal

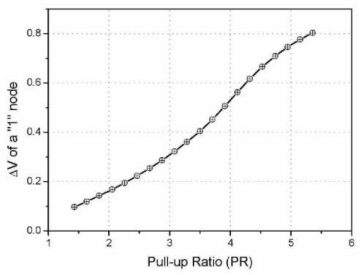

Fig 7: **The voltage drop at node $V_{"1"}$ during write access as a function of the Pull-Up ratio (PR) $\left(CR = \frac{W_4}{L_4}/\frac{W_6}{L_6} = \frac{W_5}{L_5}/\frac{W_3}{L_3}\right.$ in Figure 2.3$\left.\right)$ of a 6T CMOS SRAM cell (simulated in CMOS 0.13μm technology, V_{DD}=1.2V).**

3) *Sense Amplifier and Precharge-Equalization*

Sense amplifiers (SA) represent an important component in memory design. The choice and design of an SA defines the robustness of bit line sensing, impacts the read speed and power. Due to the variety of SAs in semiconductor memories and the impact they have on the final specs of the memory, the sense amplifiers have become a separate class of circuits.

The primary function of an SA in SRAM is to amplify a small analog differential voltage developed on the bit lines by a read-accessed cell to the full swing digital output signal thus greatly reducing the time required for a read operation. Since SRAM do not feature data refresh after sensing, the sensing operation has to be nondestructive, as opposed to a destructive sensing of a DRAM cell. Having an SA allows the storage cells to be small, since each individual cell need not fully discharge the bit line.

III. LOWER POTENTIAL RAISING SCHEME (LPRS) FOR REDUCTION OF LEAKAGE

A. *Topology and current reduction mechanism:*

There are three methods that have been used in the present work to reduce leakage current in standby mode. Out of the three techniques one has been discussed in the previous chapter. Here we discuss the second techniques called LPRS scheme. In this technique we raise the ground potential to a some an extent in standby mode. Due to rise in ground potential overall swing will be reduced so leakage current reduced. As we also know that leakage current also depends upon the value stored in cell. As we know that we are using 6-T SRAM cell. Every transistor has different leakage current in standby mode. Some transistor dissipates so much leakage power that will affect the circuit performance. So our aim to minimize that leakage power. In extra topology we add three transistors.

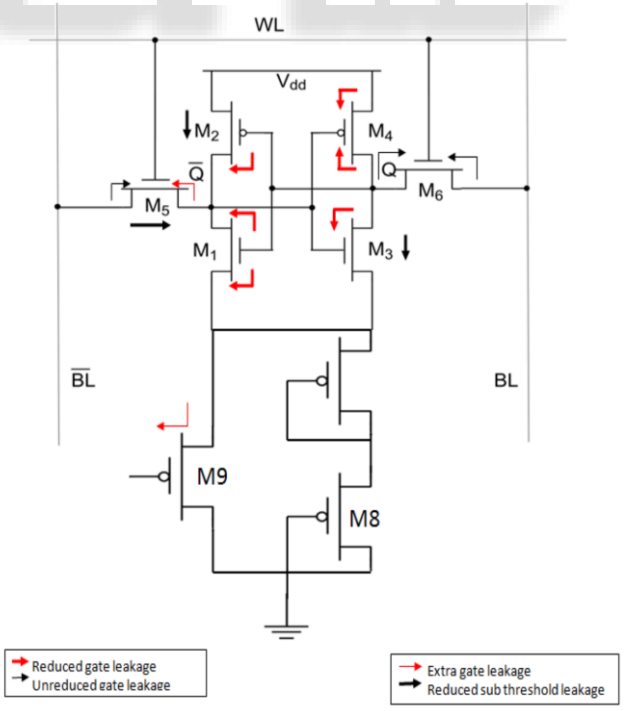

Fig. 8: LPR scheme

Out of three transistors one transistor is driven by clock, which is used as a control switch. In read or write mode we will enable the clock so that there is a direct connection

between ground supply and SRAM bit cell. However, if we disable the clock when SRAM is in active mode then there will be reduction in power supply due to which our stored value will be affected and we will not get the proper output. In standby mode we disable the clock so that there is an alternate path and all the current flows through that path. Due to this there is a reduction in input voltage swing and due to this alternate path there is a reduction in leakage current.

Figure 8 shows a schematic of an SRAM cell in which LPRS is applied. The switch provides 0 volt at ground node during the active mode and raises ground level (virtual ground) during the inactive mode. This scheme is similar to the diode footed cache design scheme proposed to control gate and sub-threshold leakage in SRAM cell, in which a diode designed with high Vt MOS transistor was used to raise the ground level in inactive mode.

B. *Effect on gate leakage*

Let us consider the impact of this approach on gate leakage first. As we know that in this approach we increase the ground potential to increase to reduce the leakage current. An increase in the virtual ground voltage (VS in fig.8), result in decrease of gate-source voltage and gate-drain voltage of transistor M1 and gate-drain voltage of transistor M2 and result in sharp reduction in gate leakage currents of two transistors. However there is no improvement in gate leakage currents for transistors M5 and M6. We know that M5 and M6 are the access transistor. In fact as a result of increase in drain voltage of M1, a new gate leakage current appear in transistor M5 as indicated in Figure 8.In corporation of LPRS results in another new gate leakage current through NMOS transistor in MOS switch.
Although only one transistor is normally used for one bank of SRAM cells, leakage current through it is not necessarily negligible because its size has to be much larger than NMOS transistors within the SRAM cell to avoid performance degradation in the active state.

C. *Effect on subthreshold leakage*

Sub threshold leakage is also an important component in leakage current. This leakage comes in picture when transistor is in off state and operated in sub threshold mode. If this leakage increases from its maximum value then it will affect the whole circuit performance and we will not be able to get a proper output. As we also know that this leakage current is also depend on the value stored in the SRAM bit cell. As for as sub-threshold leakage current are concerned, LPRS approach is successful in reducing currents through M3, M2 and M5 as well. To summarize it should be added that while all sub-threshold currents are reduced using LPRS approach, it is the only partially successful in reducing gate leakage current.

IV. SIMULATION RESULTS & PERFORMANCE COMPARISON OF PROPOSED TOPOLOGIES

A. *Performance comparison*

The simulation results verified for 10 cycles of ‘Read’ and ‘Write’ operations with the conventional 6 transistor SRAM cell and SRAM cells incorporating the proposed leakage reduction schemes. The simulations have been carried out on Cadence Design environment platform. Figs. 9, 15, 17 are the optimized schematics for conventional 6 T SRAM cell, and cells incorporating USRS and LPRS respectively. Furthermore, the rest of the figures are tool generated waveforms for currents in the individual transistors and bit line and word line signals.

The leakage currents in the conventional and the schemes suggested in previous chapters are shown in Table 1. Although from the waveforms it is evident that current in an individual transistor fluctuate during a ‘Read’ ‘Write’ cycle, in this case, only average value of current in standby mode has been measured and reported. Compared to the conventional 6 T SRAM cell, LPRS suppresses the total leakage by 59.8%. While USR scheme without changing the bit line voltages provides a leakage reduction of 69.7%. However, USR-A scheme does not give any significant advantage over the conventional SRAM cell. One of the possible reasons for this is the large current swing obtained when the pre-charge transistors are cut off from the supply. The efforts to minimize this large current swing would comprise the task for the future workers in the field. However, it can be safely presumed that both USRS and LPRS have served to reduce both gate and sub threshold leakages substantially.

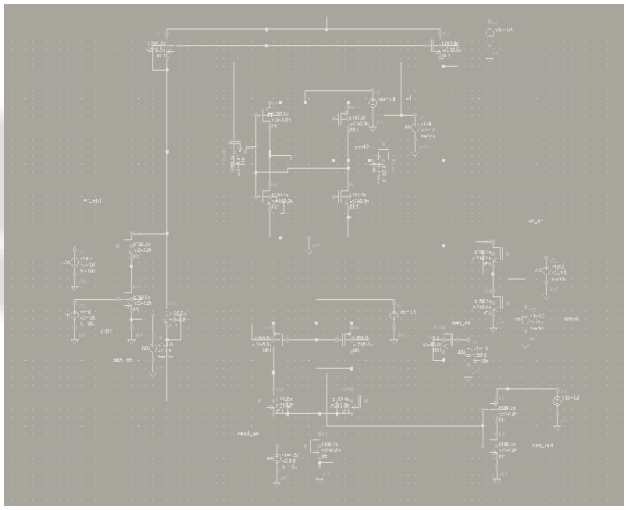

Fig. 9: 6-T Static RAM cell schematic

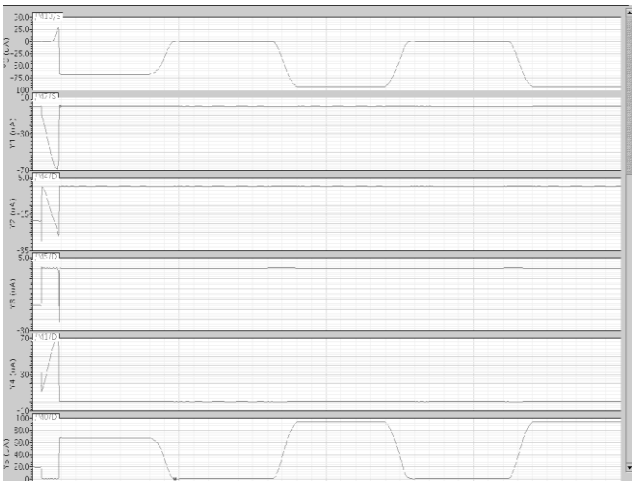

Fig. 10. Current waveforms of Read ‘0’ operation (for conventional 6-T cell)

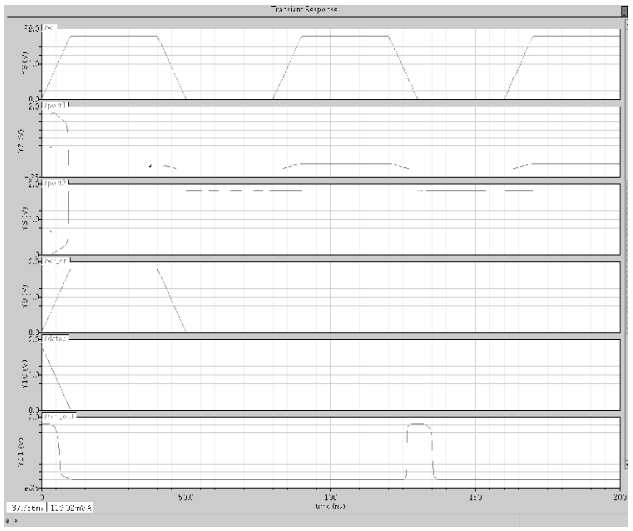

Fig. 11. Word line and bit line waveform for data read "0" operation

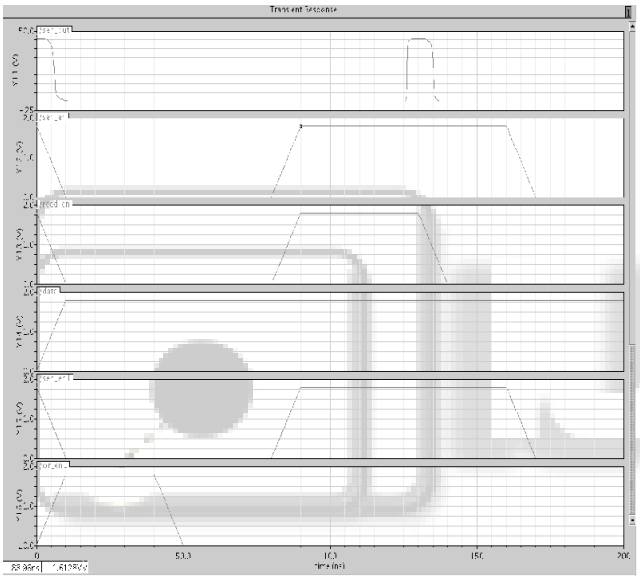

Fig. 12. Control signal and data Read '0' operation waveforms Read '0' operation

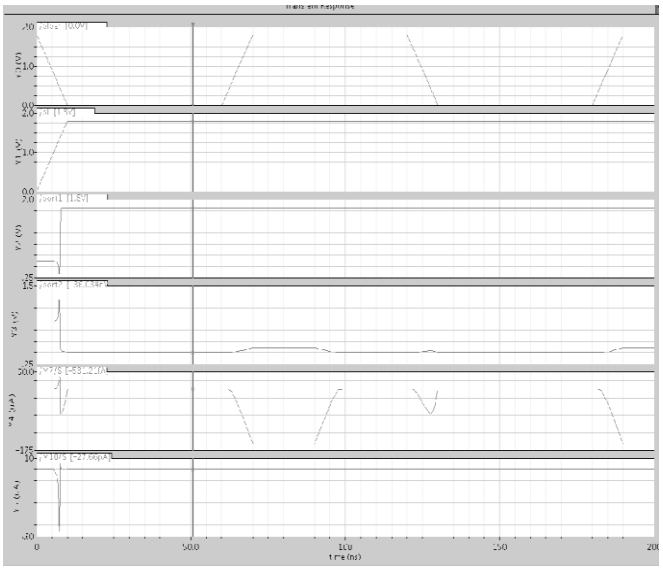

Fig. 13. Bit line and current waveforms

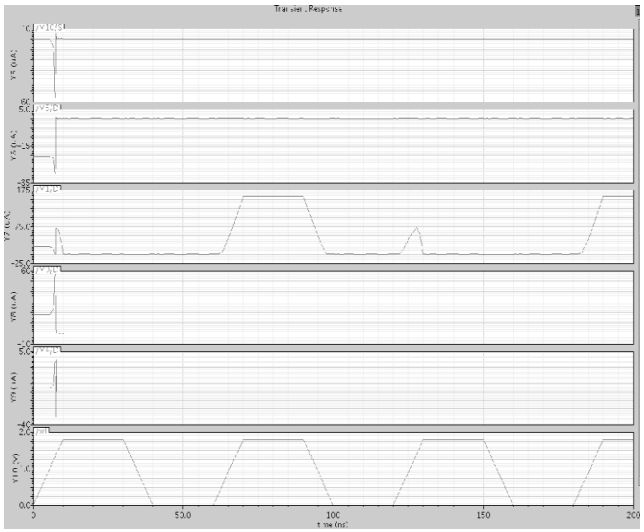

Fig. 14. Current waveforms for for Read '1' for Read '1' operation

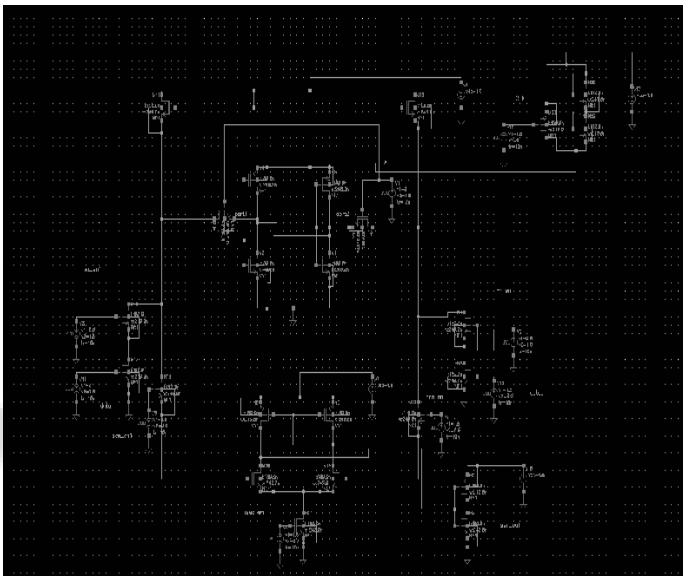

Fig. 15: Schematic for USR scheme

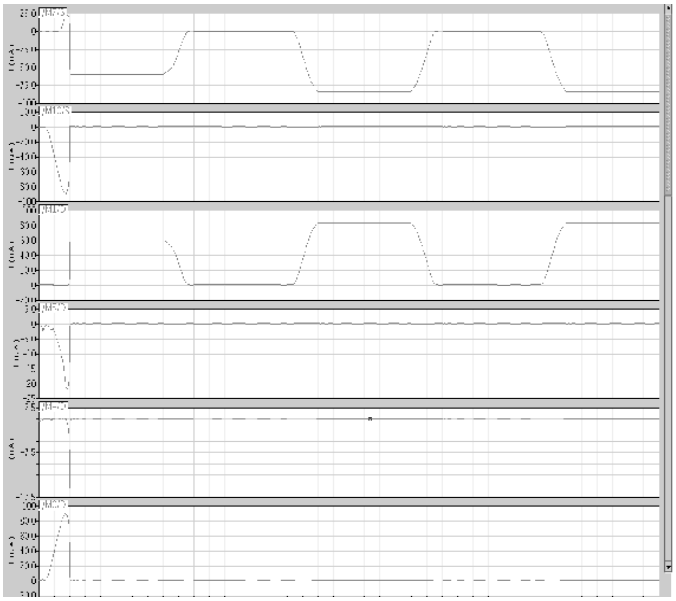

Fig. 16: Current waveforms for Read '1' operation

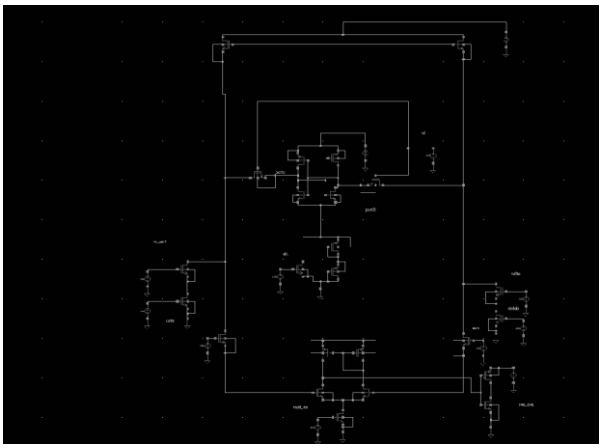

Fig. 17: Schematic for LPR scheme

	M1	M2	M3	M4	M5		M6	I cell	% REDUCTION		
	I_{gate} (pA)	I_{gate} (pA)	I_{sub} (pA)	I_{sub} (pA)	I_{gate} (pA)	I_{sub} (pA)	I_{gate} (pA)		Ig	Is	Io
Conventional cell	37.1	13.9	0.86	0.56	9.84	0.6	19.5	83.6	--	--	--
USRS	2.38	1.14	0.58	--	9.84	0.6	10.6	25.3	70.2	41.6	69.7
LPRS	2.35	1.08	0.17	0.29	10.7	--	19.4	33.6	58.3	77.2	59.8
USRS-A	40.6	1.23	0.4	0.56	11.6	0.7	5.4	64.7	30.7	20.5	23.7

Table 1: For SRAM cell Reduction

V. CONCLUSION

The present work analyzes the latest developments in low-power circuit techniques and methods with an emphasis on SRAMs. Appropriate methods for reduction of power consumption were studied such as capacitance reduction, very low operating voltages, DC and AC current reduction and suppression of leakage currents to name a few.. Many of reviewed techniques are applicable to other applications such as ASICs, DSPs, etc. Battery and solar-cell operation requires an operating voltage environment in low voltage area. These conditions demand new design approaches and more sophisticated concepts to retain high device reliability. The proposed techniques (USRS and LPRS) are topology based and hence easier to implement. The substantial reduction in leakage currents obtained proves them to be as effective as any fabrication level technique would be.

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