Implementation and design Low power VCO

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Abstract— The paper introduces a multi-pass loop voltage controlled ring oscillator. The proposed structure uses cross-coupled PMOS transistors and replica bias with coarse/fine control signal. The design implemented in TSMC 90 nm CMOS technology, 0.9V power supply with frequency tuning range 481MHz to 4.08GHz and -94.17dBc/Hz at 1MHz offset from 4.08GHz with 26.15mW power consumption.

Keywords: IC, PMOS, TSMC, VCO

I. INTRODUCTION

With the development of Integrated Circuit (IC) technologies, communication systems and microprocessors are usually working at several gigahertz frequencies with low power consumption, small chip area and an acceptable cost. For some applications, the systems also have to meet various working frequencies to save power or meet different communication standards working together, such as wi-fi and Bluetooth on the same chip system. In the chip, a Voltage Controlled Oscillator (VCO) is implemented to provide the higher frequency periodic signal for the systems. The design of the VCO has to face many challenges. Firstly, it is hard to design a low noise VCO with a wide frequency tuning band, especially with the shrinking size of technological features, which induces the lower power supply voltage [6]**.** Secondly, for a wide tuning band VCO, the voltage to frequency gain would be very large causing an increase in noise sensitivity. Thirdly, the VCO should maintain acceptable power dissipation, since it is very crucial to some applications. Therefore, the VCO is a bottleneck in the integrated circuits especially for the communication systems. The Complementary-Metal-Oxide-Semiconductor (CMOS) is the most popular technology for the modern integrated circuit design and fabrication. Based on this technology, a VCO can be implemented by the LC resonant or ring structure. Due to higher quality factor, the LC VCO design has a better phase-noise compared to the ring structure and it can also reach a very high frequency. However, because the inductor and/or varactor have to be included in the design, the cost of chip area and the complexity of the fabrication process are increased. The priority to design a ring VCO is to improve the phase noise.

In this paper, how to improve the phase noise is discussed and a ring VCO is designed with cross-coupled PMOS transistors to improve phase noise characteristics and the multi-pass loop to get a wide frequency tuning range. The following goals are aimed at being achieved is Low cost, Wide frequency tuning band, Good phase noise, Low frequency tuning noise sensitivity, Small chip size, Small power consumption.

Based on the considerations of cost and robustness, the 90nm TSMC process has been selected as the target technology for the design. Utilizing cross-coupled PMOS transistors to improve the phase noise and replica bias with coarse/fine control signal to lower frequency tuning noise sensitivity, a multi-pass ring VCO is built with a low power supply (0.9V) and a very wide frequency tuning range (481MHz to 4.08GHz). Good phase noise (-94.17dBc/Hz at 1MHz offset from 4.08GHz) and small power consumption (26.15mW) are achieved here. The core of the VCO area is also small.

II. VOLTAGE-CONTROLLED OSCILLATOR (VCO)

A voltage-controlled oscillator or VCO is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency. Conventionally, the VCO can be thought of as a box with a stable input signal V_{TUNE} and a periodic signal output V_{OUT}, shown as Fig.1.

Fig.1 Concept of VCO

For the ideal VCO, the output frequency is a linear function of the in time domain, described as:

$$V_{out} = V_p \cdot \cos(2\pi f t + \varphi) \quad (1)$$

The V_p is the amplitude of the VCO, f and φare phase parameters, and f can be tuned based on the V_{TUNE} Although equation (1) is easy to understand, it is not suitable for further analysis. In the frequency domain or S-domain, the VCO can be presented as [7]**:**

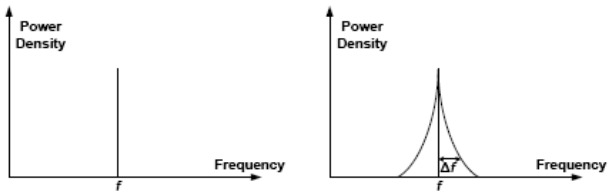
$$\omega_{out} = \omega_0 + K_{VCO} \cdot V_{tune} \quad (2)$$

The ω_{out} is the output frequency, the ω_0 is the fundamental frequency without any gain and the K_{vco} is the frequency tuning gain. The frequency tuning band means the range from the maximal frequency of the VCO to the minimal frequency the system can reach. So, the output frequency of the VCO can continually change in the frequency tuning band based on the change of the tuning signal. Usually, for certain applications, the VCO has to fix the frequency of the output.

In reality, the VCO frequency output is not a simple linear function of the tuning signal. So the VCO frequency gain can be defined as:

$$K_{vco} = \frac{d\omega_{out}}{dV_{tune}} \quad (3)$$

In the frequency domain, the non-ideal frequency fluctuations would give the symmetrical distributions sidebands close to the *f* shown as Fig.2.



(a) ideal (b) non-ideal

Fig.2 The power density of VCO: (a) ideal and (b) non-ideal

A. *LC Resonant VCO*

In LC Resonant VCO, the negative resistors are needed to compensate the parasitic resistive. It is hard to design a negative resistor only by the passive components, such as the resistor, capacitor or inductor. However, based on CMOS technology, it is possible to build it with standard transistors.

For the resistor, the voltage across it is proportional to the current based on Ohm's law. On the other hand, the voltage produced by the negative resistor is inverse proportional to the current. So it has to involve some active component to provide the extra power dissipation.

One of the popular negative resistors widely employed in the LC VCO is illustrated as Fig.3.

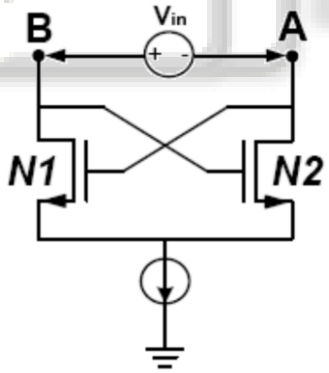


Fig.3 Negative resistor

Based on Fig.3, if the voltage of V_{BA} increases, assuming the V_A is constant compared to the ground, which means the V_{gs} of N2 is increased, that would drive the N2 to the triode region, so the current would be decreased. Although the V_{ds} of N1 is increased, the current will not increase much. Now, let's do the quantitative analysis. The following equations can be got as:

$$V_{BA} = V_{gs2} - V_{gs1} \quad (4)$$

$$I_{ds2} = I_{ds1} - I_{AB} \quad (5)$$

$$I_{ds1} = -\frac{g_m}{2} \cdot (V_{gs2} - V_{gs1}) \quad (6)$$

$$I_{AB} = -\frac{g_m}{2} \cdot V_{AB} \quad (7)$$

From the equation (7), the voltage across A and B is inverse proportional to the current and the slope is $-\frac{gm}{2}$.

Based on the negative resistor, the LC Resonant VCO can be simply built by just adding the LC tank on it, shown as Fig.4

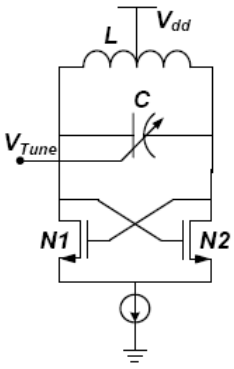


Fig.4 Simple LC resonant VCO

The LC VCO employs the varactor to tune the LC tank resonant frequency.

B. *Ring Structure VCO*

The simplest ring VCO is the single-end signal structure, which is shown as Fig.8. D1 to Dn represents the delay cells, which provide the gain and phase shift. They construct a closed loop by cascading all stages.

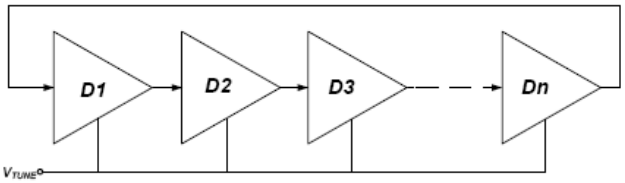


Fig.5 Single-end signal ring VCO

Assuming $D_1(s)$, $D_2(s)$, $D_2(s)$, $D_3(s)$….. $D_n(s)$ represent the transfer function of each stage delay cell, the open loop transfer function H(s) is illustrated as:

$$H(s) = D_1(s) \cdot D_2(s) \cdot D_3(s) \cdot D_4(s) \ldots D_n(s) \quad (8)$$

Supposing the all delay stages are identical and their transfer function is D(s), the open loop transfer function H(s) will be as:

$$H(s) = D^n(s) \quad (9)$$

Based on the Barkhausen Criteria, the following relationships can be got as:

$$|D(s)|^n \geq 1 \quad (10)$$

$$\angle D(s) = \frac{360^\circ}{n} \quad (11)$$

From the equation (11), each stage delay cell has to provide $360^o/n$ phase shift for the ring VCO, which means if the single pole structure is being used, the n has to equal or be more than 3 since the single pole delay cell can only provide 180^o phase shift at the infinite frequency.

The delay cell of the Single-End Signal Ring VCO can be various structures, such as single-stage amplifiers or inverters; however, the tuning signals have to be added on the VCO. There are many ways to tune the frequency; for example, changing the load which can be the resistor or capacitor shown as Fig.9 or changing the tail current for the inverters shown as Fig.10.

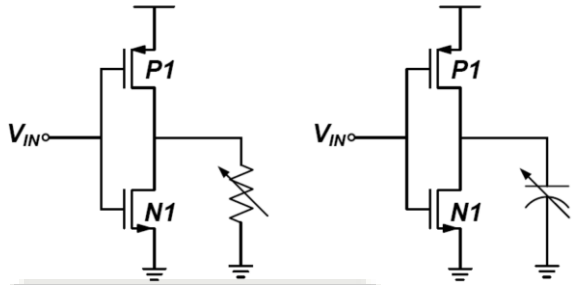


Fig.6 Resistor and capacitor load controlled delay cell

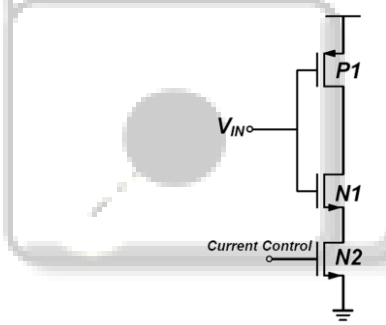


Fig.7 Current controlled delay cell

The Single-end signal ring VCO is simple and easy to design, but when it is integrated with other applications, the VCO output is affected by the other circuits, so most systems use a differential loop VCO for the applications.

III. CIRCUIT DESIGN AND ANALYSIS

A. *Cross-Couple PMOS Delay Stage*

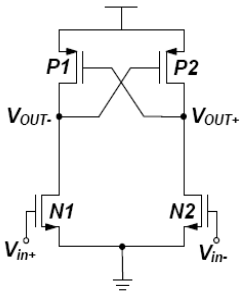


Fig.8 Cross-couple PMOS Delay Stage

The delay stage has to be carefully selected for the ring structure VCO to meet the design requirements. Also, the differential pair should be applied to avoid to be affected by other applications existed on the same system. There are many candidates that can be employed for ring VCO. One of the best is the cross-couple PMOS differential delay stage that is shown in Fig.8[8].

As can be seen in Fig.8, this structure is simple, and it has some obvious advantages. The cross-couple PMOS transistors P1 and P2 can accelerate the transition time of the oscillated signal. For example, when the signal V_{in+} is going from to high; correspondingly, the V_{OUT-} will change from high to low, which would make the V_{SG} of P2 to increase. Consequently that speeds up the changing from low to high of V_{OUT+}. So, the load transistor P1 and P2 in the delay stage would help the differential pair to transfer the signal. Because of the cross-couple transistors, this structure is very suitable for the ring VCO design. The phase noise level base on this ring VCO can be compared with its LC counterparts.

On the other hand, this structure has an undeniable drawback, as there is no frequency tuning signal in the circuit. Therefore, several studies on how to add the tuning signals are applied; for example the circuit in Fig.9 is one of them.

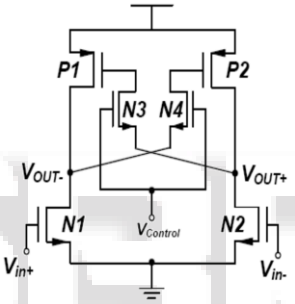


Fig.9 Cross-couple PMOS delay stage with 2 transistors control

The transistor N3 and N4 are connected to the gate of cross-coupled PMOS transistors to tune the slew time of the load P1 and P2 and to tune the oscillating frequency. The drawback of this structure is that the frequency tuning band cannot be wide since the control signal cannot greatly vary the gain or resistance of the delay stage.

A different technique to apply a tuning signal is by adding a tail current as shown in Fig.10. By doing so, the frequency tuning band will be improved; however the flicker noise of the tail current will experience up-conversion, so this has to be addressed. Also, although the frequency tuning band is wide, the linearity of the frequency to voltage of the tuning signal is not good.

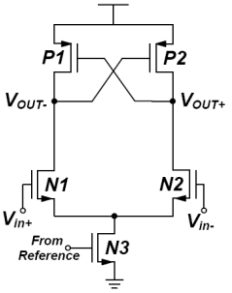


Fig.10 Cross-couple PMOS delay stage with tail current control

B. *Replica Bias Design*

The cross-couple PMOS transistor differential pair is selected for the delay stage and the tail current will be added to be the tuning signal. Now the linearity of the frequency to voltage of tuning signal problem has to be fixed while the up-conversion flicker noise will be discussed in the next chapter.

To address the linearity problem, the 2 PMOS transistors are paralleled with cross-couple PMOS and the replica bias is designed to tune the load of each stage, as shown as Fig.11.

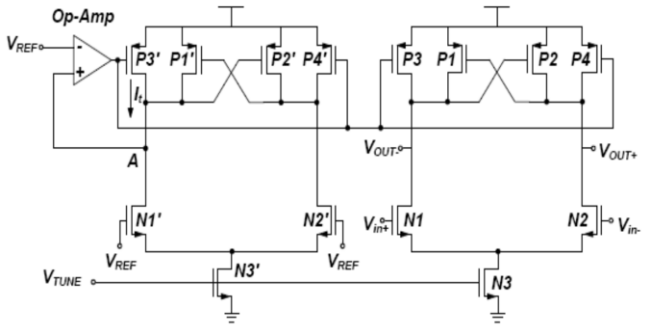


Fig.11 Delay stage with replica bias

The replica bias part has exactly same structure of a delay stage with the addition of an op-amp to construct a negative feedback system.

If I_t is increased, which means V_A is decreased and V_{DS} of transistor P3' is increased. At same time, because of the decrease of V_A, the output of the op-amp will be increased, and the voltage V_{SG} of P3' is decreased. Finally, R_{DS} the resistance between the source and drain of P3' is decreased, so the V_A gets compensated and is almost kept constant. Similarly V_A is maintained constant and the current I_t is decreased.

Based on the above discussion, R_{DS} of P3' can be automatically changed to keep V_A constant, so it makes the VCO have the better linearity for the frequency to the voltage tuning. In addition, because of the almost constant V_A, the common mode signal of the periodic signal from the VCO will not much vary. This is also very important to VCOs, especially for the one with a wide frequency tuning range. Since these periodic signals from VCOs cannot drive the other applications or circuits, the buffer has to be applied to regulate these signals. If there is too much variation on the common mode signal, the design of a buffer would be complicated. So the reference signal for the N1', N2' and Op-Amp are same, which is the common mode signal of the VCO.

Therefore, with the replica bias stage, the VCO can offer good voltage to frequency linearity and make the buffer design easier.

C. *Multi-Pass Loop Design*

Usually, the ring VCO only has a loop to provide the feedback, but in some cases, the frequency tuning requirement cannot meet based on this structure. Researchers have tried to use other technologies to improve the ring VCO, and multi-pass loop is one of them, shown as Fig.12.

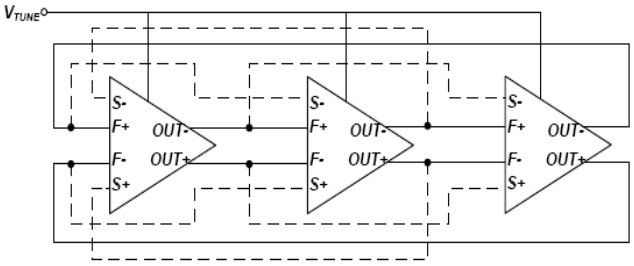


Fig.12 Multi-pass loop ring VCO

This structure employs two operating loops, the first loop (solid line), which works as a normal differential input pair, and the second loop (dash line), which provides an additional feed forward loop to reduce the slew time of the output nodes when switching.

The reason why the multi-pass can improve the frequency tuning characteristic is because the slew time of the first differential loop is enhanced. For the ring VCO, the total phase shift of the 3 stages is 360^o based on the Barkhausen Criteria, so each stage should have a 120^o phase shift. From Fig. 24, the second loop is feedback from the next stage; therefore, the phase shift of each stage for the second loop is 240^o as shown in Fig.13.

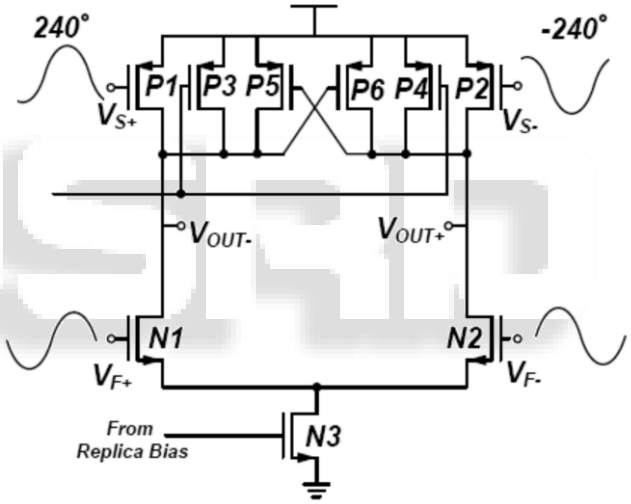


Fig.13 Phase shift for the second loop

When the gate of the first loop transistor N1 is changing from low to high, the secondary input transistor P5 has already left the highest point, which would decrease the rising time, because the second loop signal will contribute to charge the parasitic capacitors of the output node. Also, the second loop differential pair will provide some gain for the oscillation, but it cannot be very large, otherwise the oscillation would not be started since the system would violate the Barkhausen Criteria.

D. *Small Signal Analysis*

The ring oscillator is a non-linear large signal feedback system. Analyzing this system is very difficult, but there are still some methods can be used, such as small signal analysis. Although it cannot give the exact frequency tuning range and amplitude level, the small signal analysis can offer insight into the frequency and oscillation characteristics. It is impossible to directly employ small signal analysis on the ring oscillator; therefore, the following 2 assumptions are made:

1) The periodic oscillation waveform is exactly a sinusoidal shape.

2) The amplitude of the periodic oscillation is small.

In practice, the oscillation signal is composed of many harmonics attached together, but it is impossible to analyze the higher order functions. If the first assumption is met, the order of the model is one, which simplifies the analysis. In the same way, the amplitude from the ring oscillator is a large signal, which means the transistors of delay stages will go through from triode region to the saturation region and to the triode region again. And for the phase noise, the amplitude of the oscillator should be as large as possible, which will be discussed in the next chapter. Therefore, because of the second assumption, the transconductance g_m of the small signal model can be considered as a constant amount.

The proposed 3 stages multi-pass ring VCO is shown as Fig.14.

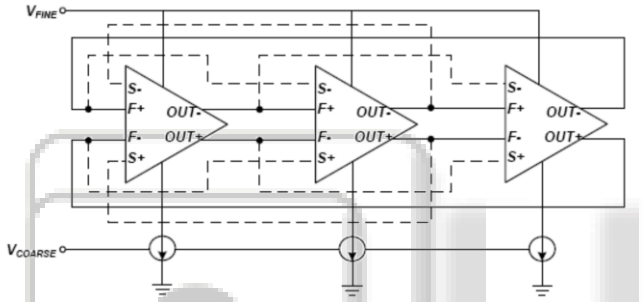


Fig.14 stage multi-loop VCO with first loop (solid line) and second loop (dash line)

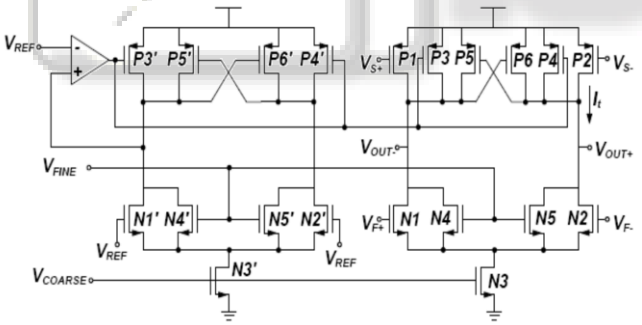


Fig.15 Proposed multi-pass loop delay stage with fine/coarse control

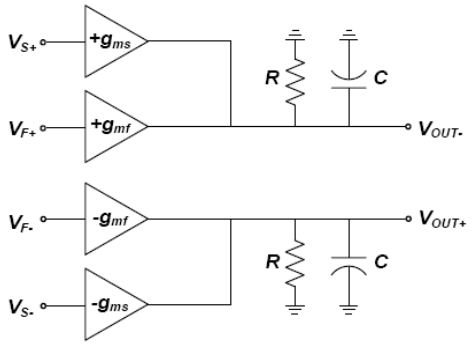


Fig.16 First order model of the delay cell

The VCO employs two operating loops, the first loop (solid line) and the secondary loop (dash line); also, it has dual signals for the frequency tuning. Based on the architecture from Fig.14, repeated as follows in Fig.15, the first order small signal model of the proposed delay cell can be drawn as shown in Fig.16.

IV. SIMULATION RESULTS

Based on the previous analysis, the transistor size of the proposed multi-pass ring VCO is summarized in Table 1. The replica bias circuit is the same as the delay cell, but without the secondary loop input pair. The length of the current mirror transistors is enlarged to 1 μm.

Transistor	W/L
N1/N1'/N2/N2'	96/0.1
N4/N4'/N5/N5'	48/0.1
N3/N3'	90/1
P1/P2	55/0.1
P3/P3'/P4/P4'	5/0.1
P5/P5'/P6/P6'	80/0.1

Table. 1: Transistor sizes of proposed delay cell and replica bias (μm)

SpectreRF is employed to do the simulation with TSMC 90nm technology. The coarse frequency tuning range is shown as Fig.32.

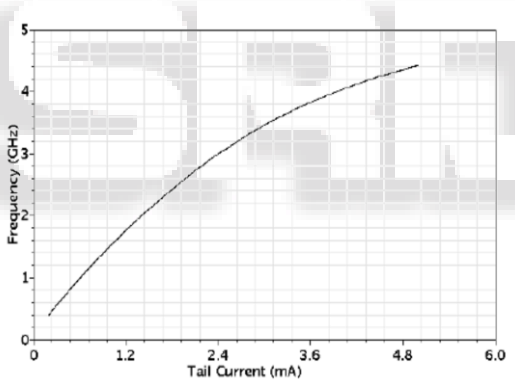
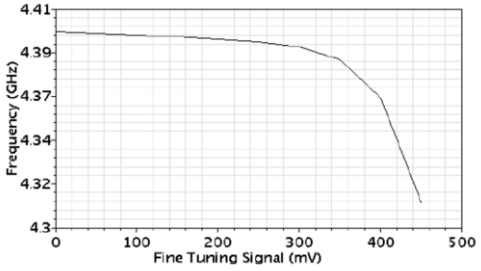


Fig.17 Coarse frequency tuning range

From Fig.17, the coarse tuning range of the proposed oscillator is from 394MHz to 4.4GHz when V_{FINE} is equal to 200mV and while the coarse tuning gain is 834.5MHz/mA. The fine frequency tuning characteristic is simulated and illustrated in Fig.33 with a tail current of 5mA, 4mA, 3mA, 2mA, 1mA and 200 A, respectively.



(a)

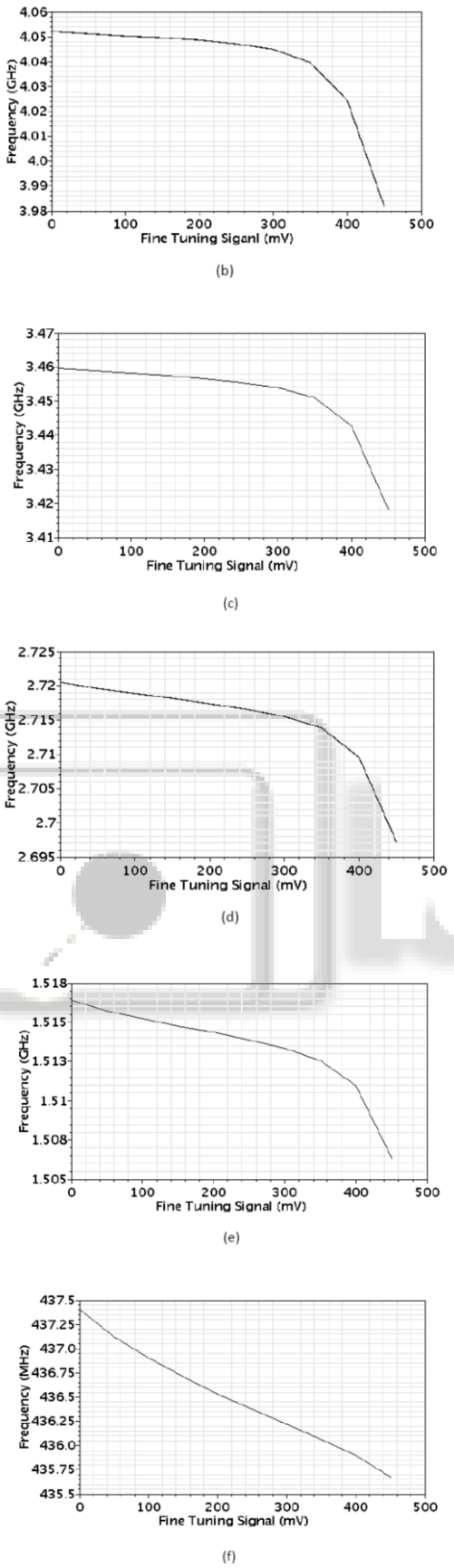


Fig.18 Simulation results of fine tuning signal with tail current (a) 5mA, (b) 4mA, (c) 3mA, (d) 2mA, (e) 1mA and (f) 200 A

From Fig.18 the higher frequency tuning gain is 200MHz/V, and the lower one is 3.8MHz/V and the average is 90MHz/V. Because N2/N3 has to work in the triode region, the fine tuning signal can be varied from 0V to 450mV.

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