A comprehensive study on Implementing of 10bit Two step Flash ADC

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Abstract— This paper proposes a 10bit two step flash ADC.As the CMOS technology continues to scale down, signal processing is favourably done in digital domain, which requires Analog to digital converters (ADCs) to be integrated on-chip. Among various ADC architectures, the two step flash ADC architecture is the best suited for low power and 10 bit resolution. To decrease the area, power consumption, and cost while maintaining 10bit accuracy, the architecture is divided into coarse flash ADC and fine flash ADC connected through current steering Digital to analog converter (DAC) and residue amplifier. To get the best performance the coarse convertor of 5bit and the fine convertor of 5bit are chosen. The comparator design is done with optimum power and area. Intermediate state accuracy increased by thermometer coded current steering DAC.

I. INTRODUCTION

Analog-to-digital converters (ADCs) are useful building blocks in many applications such as a data storage read channel and an optical receiver because they represent the interface between the real world analog signal and the digital processors.

The digital circuits which are designed at the higher level of abstraction are highly beneficial from the advanced technologies which lead to the processing of signals in digital domain. In many application, it is quite often that signals is processed in analog and then digital and vice-versa in some other application. All processing is done within system on chip. Data convertors are important blocks in application specification integrated circuits (ASIC). Digital to analog (DAC) and analog to digital convertors (ADC) are used for entire communication transmitter and receiver, computer, cellular phones and many electronics gadgets.

The specification of data conversion system in these applications depends on the static and dynamic parameter such as power supply, power dissipation, integral and differential non linearity, signal to noise ratio, spurious free dynamic range and the most important the number of bits. The choice of the data conversion architecture falls within following architectures: Nyquist rate, over sampled or low speed, high resolution (sigma delta, dual ramp),medium speed (successive approximation) and high speed low resolution(full flash, two-step flash) The comparison between different types of analog to digital convertors is shown in figure 1.the comparison shows that the resolution of analog to digital convertor is decreased as the speed of signal processing is increased from several kilohertz to some gigahertz. Apart from speed-resolution metric, another performance metric is time to reading (the number of clock cycle required to perform the conversion).the flash convertors are very high speed devices which requires only one cycle for reading of data hence there is not an issue of synchronization as compare to others like successive approximation type ADC, In which output data comes after the several clock cycles after the convert command. The application like high definition multimedia transmission wide band radio and system like communication receiver require high data rate and large data storage.

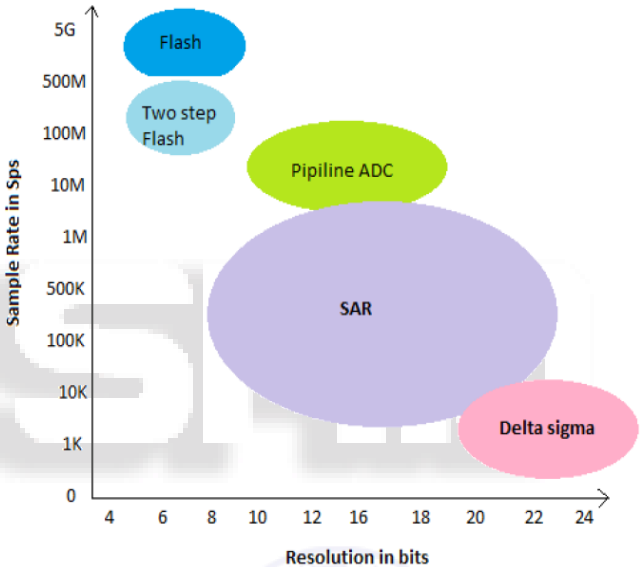

Figure 1: ADC type comparison

The number of comparator in flash ADC ($2^n - 1$) increases exponentially with the increase in number of bits (n). This results in overall increase in chip area and power consumption.

In order to reduce the power and total area, we can proceed towards an alternative of fully Flash ADC. Fully flash ADC is used as an intermediate state in the multistage architectures such as pipe line ADC, two step flash ADC.

II. PREVIOUS HIGH SPEED ARCHITECTURES:

A. *Flash ADC Architecture*

Flash converter use $2^n - 1$ comparator and 2^n matched resistors for n bit resolution. While 8 bit flash ADC requires 256 comparator s,10bit requires 1024.In addition the comparator Offset requirement becomes exponentially more stringent with resolution; the offset of 10 bit comparator must be less than ¼ the offset of an 8 bit comparator. Thus when the resolution increased by 2bits from the currently available 8bits, to 10bits flash converter' area and power increase by a factor of 4. The time requirements are also four times more severe. It shows as figure 2[1].

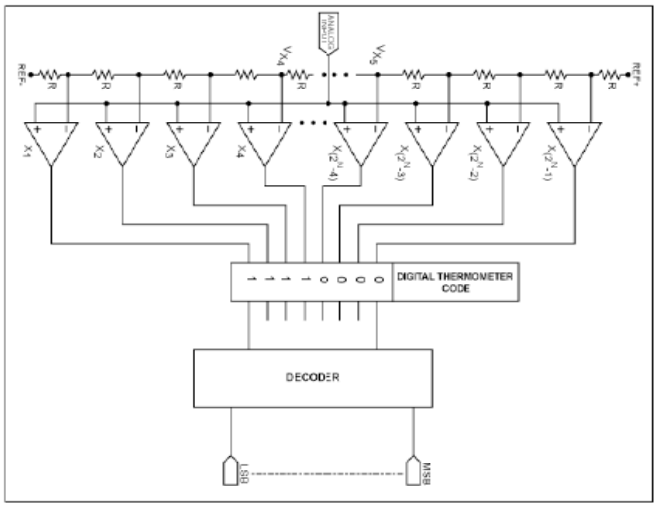

Figure 2: Flash ADC architecture

B. *Pipelined Architecture*

The pipelined architecture uses two or more stages that each does an analog to digital conversion (A/D) and passes residual voltage on to the next stage to do another conversion. Each stage consists of an S/H, ADC, DAC, subtractor and again block. The S/H holds the input during each conversion cycle. The ADC does a conversion. Then the DAC creates a quantized version of input that is subtracted from the held input. The result of subtraction is a small residual voltage that is amplified and passed on to the next stage for the conversion in next clock cycle. While the next stage operates on this input, the previous stage takes new sample and converts it, thus the increasing throughput via concurrent operation. One conversion is done each clock period. This however is not as fast as CMOS flash converter. The advantage is the potentially fast operation gained by stages operating concurrently while the increased resolution is attained by adding additional stages. Thus the area and power consumptions grow linearly with precision. We can see the pipeline architecture in figure 3[2].

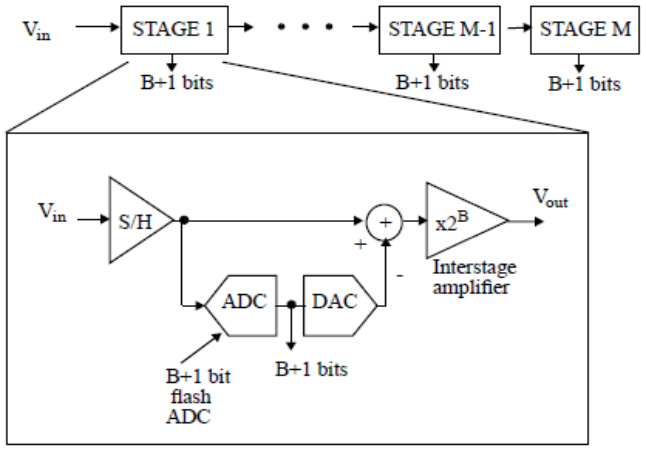

Figure 3: Pipelined Architecture

III. TWO STEP FLASH ARCHITECTURE

Unlike the Flash ADC, two steps Flash ADC do not require more comparator. It requires only (2N/2-1) comparators means if we are use 10 bit it require only 62 comparators. The exponential growth of power, area and input capacitance of flash converters as a function of resolution makes them impractical for resolution above 8 bits, calling for other topologies that provide a more relaxed trade off among these parameters. Two step architecture trade speed for power, area and input capacitance.

In a two step ADC, first a coarse analog estimate of the input is obtained to yield a small voltage range around the input level. Subsequently input is determined with higher precision with this range. Figure 4 is two step architecture consisting of an S/H, a coarse flash ADC stage, a DAC, a subtractor and fine flash ADC stage. We describe its operation with timing diagram in the same figure 4[1].

For t < t1, the SHA tracks the analog input. At t = t1the SHA Enters the hold mode and the first flash stage is strobe to perform the coarse conversion. The first stage digital estimate of the signal held by the SHA (VA), and the DAC converts. This estimate to analog signal (VB) which is a coarse approximation of the SHA output. Next the subtractor generates an output equal to the difference between VA and VB (VC called the "residue") which is subsequently digitized by the fine ADC.

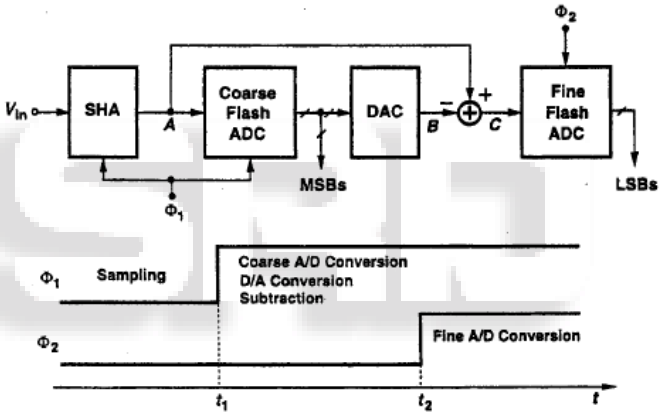

Figure 4: Two step flash Architecture

The front end SHA plays crucial role in the performance of two step ADCs. Without the SHA. The maximum permissible slew rate of the input signal is harshly limited. This is occurs because if the analog input varies rapidly in the conversion mode, then the signal is digitized by the first stage is not equal to that sensed subtractor immediately before fine conversion .figure 5 illustrate this timing issue, which fundamentally arise from the delay of the first stage and the DAC[1].

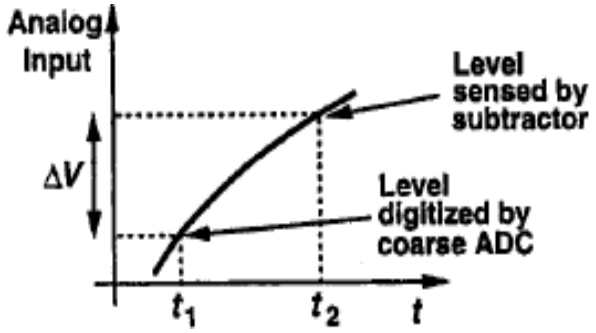

Figure 5: Timing issue of two steps ADC

This discussion also reveals another timing issue in the presence of SHAs. Since the output of typical SHA takes a finite time to settle after the transition from the sampling to the hold mode, the coarse conversion cannot begin immediately after that transition if the subtractor is to sense the same level. As shown in figure 6.We note that coarse conversion occurs at t = t1, then the level digitized by the coarse stage substantially deviates from that sensed by subtractor before the fine conversion. A simple way of avoiding this error is to begin the coarse conversion only after the SHA output has settled to within 0.5 LSB of its final value, of course this time ADC is idle.

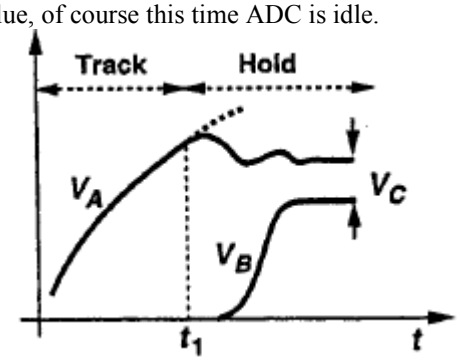

Figure 6: Timing issue with SHA

A. *Design of Sample and Hold Circuit*

It is first most important block of 10 bit two step ADC design. A sample and hold circuit sample an analog input in first half of clock period and hold the sample value for the next half of clock. It is also referred as track and hold circuit. Sample and hold circuit is an important block in the data convertors and it is used to minimize the error due to the signal appearing at the different time in the interval operation of the convertor at different block.

Normally the maximum throughput of the flash ADC is dependent on the accuracy and precision at which the comparison is done but the maximum input bandwidth at which the ADC work depends on the precision and accuracy at which signal is sampled. In order to meet the performance requirement in the monolithic implementation of flash data convertors, new techniques are invented in the open loop sample and hold circuit with lower value of sampling capacitance but this indented technique decrease the sampling rate. In our approach we also deal with the small capacitor during the sampling mode but with an increase in the value by introducing the miller capacitor in hold mode. The sampling and hold circuit shown in figure 7[3].

The circuit is made of high gain operational amplifier and the transmission gate, in order to improve the performance. The sample NMOS in sample mode charges the capacitor to the input value and causes the negative charge injection during the hold mode by turning off the MOS transistor. The charge injected through the transistor change the voltage level at the sampling capacitor in hold mode called as pedestal error and is input dependent. The relation between change in voltage and input Vin given is

$$\Delta V = -\frac{C_{ox}\, W\, L\, (Vdd - Vt - Vin)}{2C_{hld}}$$

Where the ΔV is change in voltage, Cox is oxide capacitance and L is effective width and length and Chld is the capacitance in hold mode.

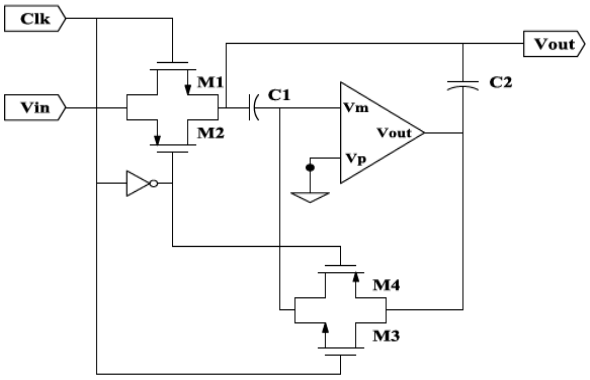

Figure 7: Sample and hold circuit with miller holding capacitor

B. *Design of Comparator*

In this section we discuss issue related to comparator and its internal circuit. The main circuits are:

[1] Pre-amplifier
[2] Decision Circuit or Latch
[3] Output Buffer

1) Pre-amplifier

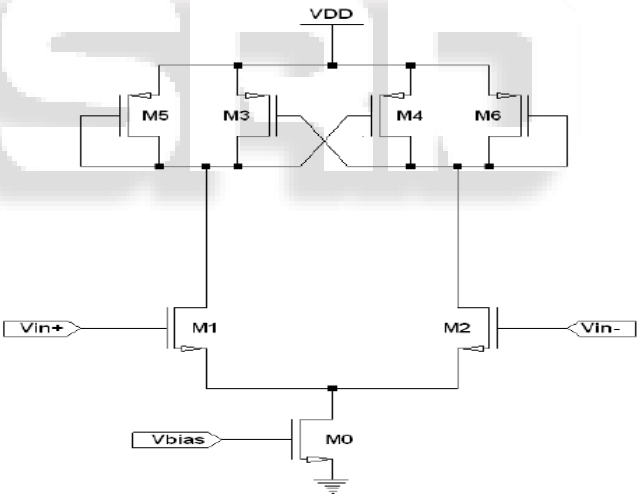

Figure 8: Pre-amplifier

The Pre-amplifier is the most commonly used solution placed in front of the comparator to reduce the kickback effect. The pre-amplifier are mainly used for isolation of the input nodes and reference nodes from the switching nodes while providing small amount of amplification. The load devices are connected such that in differential mode, the outer transistors act as positive resistors, while the cross-coupled devices act as negative resistors.

The negative resistance cancels the positive, thus presenting high differential output impedance. An advantage of cross-coupling is that the PMOS load provides implicit local common-mode feedback with no extra devices. Therefore, the common-mode voltage is stabilized [7]. Pre –amplifier shows in figure 8.

2) Decision Circuit or Latch

The numbers of comparator used in the two step flash ADC are 62, so the design of comparator is critical task because it consumes a large percentage of power and requires large are for ADC. The low gain of pre-amplifier is increased using positive feedback latch in controlled manner. The dynamic latch is used most of the time as it reduces the power consumption of the comparator. The gain and bandwidth of the comparator depends on the resolution and speed of ADC [7]. Regenerative latch is shown in figure 9.

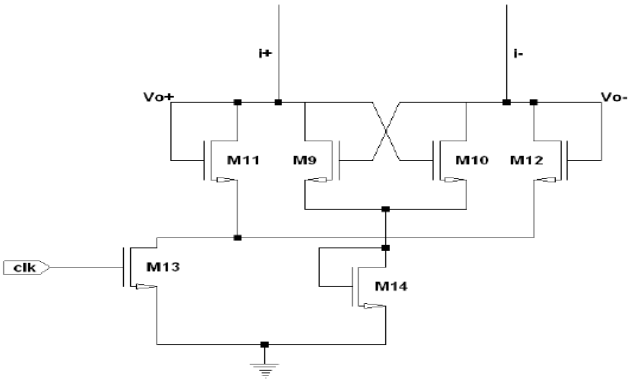

Figure 9: Decision Circuit or Latch

The positive feedback latch stage is used to determine which of the input signals is larger and extremely amplifies their difference. Transistor M13 is controlled by the clock switching; M9, M10, M11 and M12 constitute a positive feedback unit. When the clock signal clk is high, a relatively state of the comparator to compare the result directly from the pre-amplifier output decision. When the clock signal clk is low, M13 transistor cut-off, and can effectively latch output signal, comparing this time to stop comparing, in the latch state. It takes positive feedback from the cross gate connection of M9 and M10. Consider i+ >> i- so that M11 and M10 are ON and M9 and M12 are OFF. Here also β11=β12 and β9=β10=βb for which Vo- is 0v and Vo+ is

$$Vo+= \sqrt{\frac{2i+}{\beta a}} +VTHN$$

Where β = kp w/L

If we start to increase i- and decrease i+ when drain to source voltage of M10 is equal to the threshold voltage, VTHN of M9, switching takes place. At this point M9 takes current away from M11 which decrease drain to source voltage of M11 and M10 turns off. If we assume that maximum value of Vo+ or Vo- is equal to 2VTHN then under these circumstances M9 and M10 operate under cut-off or triode region under steady state condition. Then voltage across M10 becomes VTHN and M10 enters into saturation and current of M10 is

$$i-=\frac{\beta b}{\beta a} i +$$

This is the point at which switching takes place; i.e. M10 shuts off and M9 turn on. If βa=β, then switching takes place when the currents, i+ and i- are equal. A similar analysis of increasing i+ and decreasing i- results in

$$i+=\frac{\beta b}{\beta a} i -$$

3) Output Buffer

The output buffer is used in comparator to convert the output of the decision circuit into a logic signals (i.e., 0 or 1.8v). The output buffer should accept a differential input signal. The result of the gain of the preamplifier and the gain of the latch are makes overall comparator gain. The gain of invertors inserted after the latch does not contribute to the overall gain anymore, as the latch already establishes full logic level at VOH and VOL. Nevertheless, additional inverters (called buffer or drivers) are used to drive the capacitive load [7]. The complete comparator circuit is given in figure 10.

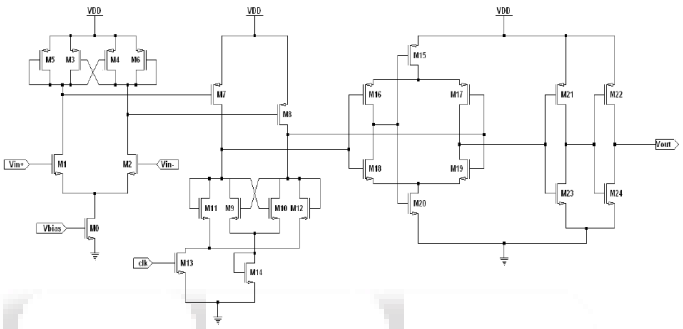

Figure 10: Comparator

C. *Thermometer coded Current Steering DAC*

Most high speed D/A converters are based on current steering architectures. Since these architectures can drive resistive loads directly, they do not require high speed amplifiers at the output and hence are potentially faster than other type of DACs. While the high speed switching of bipolar transistors makes them the natural choice for current steering DACs, Many designs have been recently reported in CMOS technology as well. The main part of Thermometer coded current steering is Unit current cell. The main task of current cell is providing a constant cover over the entire frequency and output voltage range. This means that the output impedance should be as large as possible. In its simplest form a current cell for a differential current steering DAC look like figure 11. In the circuit transistor M3 is the current source and M1 and M2 are the switches. The signals driving the switches are complementary such that only one of the two switches is ON at any time [6].

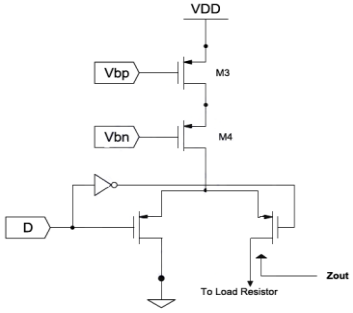

Figure 11: Current steering

The problem with simple current cell is its limited output impedance. The output impedance can be increased by cascading the current source so M4 is used in order to increase the output impedance. The output of current steering DAC must have equal step size so that it does not introduce error such that output amplitude of residue amplifier is equal to the input signal.

IV. IMPLEMENTATION

In this section, we present version 0.9, Service Pack 8 of CadeBord, the culmination ofyears of implementing. On a similar note,it was necessary to cap the bandwidth used by our system to 5122 teraflops. Similarly,the centralized logging facility and the homegrown database must run in the same JVM.our framework requires root access in order tocache the exploration of symmetric encryption. Since our approach runs in $\Omega(n)$ time Implementing the client-side library was relatively straightforward. CadeBord is composed of a centralized logging facility, a serverdaemon, and a collection of shell scripts.

V. CONCLUSION

After detailed analysis about the communication receiver an analog to digital convertor is defined with high speed and low power consumption requirements. Next, a broad literature survey have been made, in order to select a particular ADC architecture among the different architecture present till now. The two step flash ADC architecture is chosen because of high enough resolution, low power consumption, high speed of operation, simple principle of working, and it is very useful in the communication application.

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