# Fault Injection Approach for Network on Chip

**Tapas Patel**[1]
[1]Gujarat Technological University Ahmedabad, Gujarat.

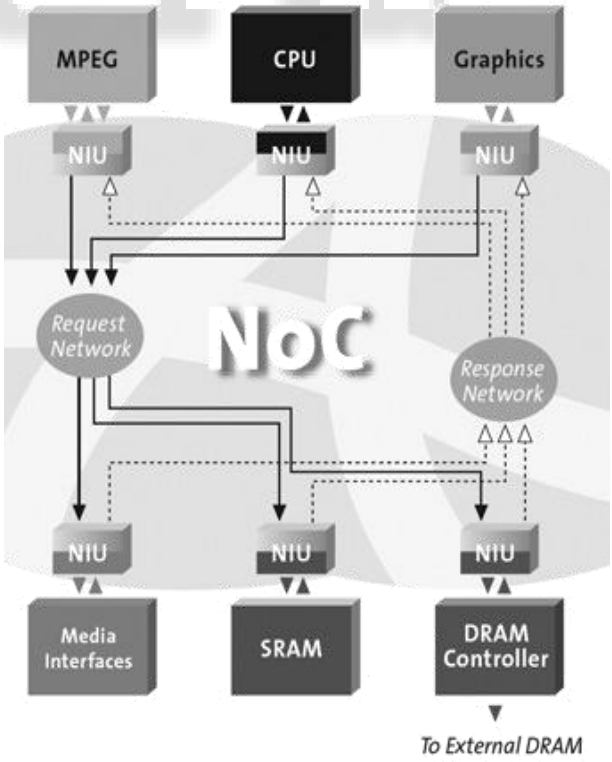
*Abstract*— Packet-based on-chip interconnection networks, or Network-on-Chips (NoCs) are progressively replacing global on-chip interconnections in Multi-processor System-on-Chips (MP-SoCs) thanks to better performances and lower power consumption. However, modern generations of MP-SoCs have an increasing sensitivity to faults due to the progressive shrinking technology. Consequently, in order to evaluate the fault sensitivity in NoC architectures, there is the need of accurate test solution which allows evaluating the fault tolerance capability of NoCs. Presents an innovative test architecture based on a dual-processor system which is able to extensively test mesh based NoCs. The proposed solution improves previously developed methods since it is based on a NoC physical implementation which allows investigating the effects induced by several kind of faults thanks to the execution of on-line fault injection within all the network interface and router resources during NoC run-time operations. The solution has been physically implemented on an FPGA platform using a NoC emulation model adopting standard communication protocols. The obtained results demonstrated the effectiveness of the developed solution in term of testability and diagnostic capabilities and make our solutions suitable for testing large scale.

## I. INTRODUCTION

Nevertheless, NoCs are characterized by high performances and low power consumption; one of the open problems that afflict research activities on NoCs is the evaluation of their fault tolerance capabilities. Indeed, as specified in, faults are increasing happening and a very large set of effects must be considered in new generation of NoCs. The larger occurrence of fault is mostly due to the technology scaling of the new chip generations that result more susceptible to fault appearance induced by different phenomena such as single-event upsets, cross-talk, age-related degradation or process variability. Generally, test method of NoC infrastructures address two issues: testing the switch blocks and testing the interconnection segments layout including the logic routers logic resources. Different testing techniques have been proposed in order to evaluate fault effects on NoC. Several NoC test methods have been focused on testing of the functional IP cores using Test Access Mechanism (TAM). Other authors assumed specific fault model for NoC fabric and subsequently adopting it to test the data transportation and the functional blocks.

Vice versa, dedicated TAM based on specific on-chip network is adopted by functional test solutions on SoCs multi-cores. The solution of our work improves previously proposed method by developing a flexible and accurate fault injection environment, which can be adopted in order to evaluate the fault tolerance capability of different NoC architectures. The main advantage of the proposed solution rely on the possibility to apply different fault models that can emulate the effective faults affecting NoC architectures, besides the proposed solutions has a full controllability an observability of the NoC under test, since interconnections values and routers functional behavior can be directly observed during the test operations, feature which is extremely reduced for test solutions applied directly to the manufactured chip, since NoC interconnections are deeply embedded and spread across the chip, therefore adding of probe interconnections results inapplicable. The implementation of our solution relies on the main idea illustrated in Figure 1.

The fault injection method we developed is innovative since it is based on single reconfigurable chip, such a Static RAM-based Field Programmable Gate Array (SRAM-based FPGAs) where thanks to a suitable architecture, faults can be injected and evaluated. As illustrated in Figure 1, the architecture consists of two processors: the processor 1 is devoted to the application of the test pattern to the NoC under test while the processor 2 performs the injection of the faults. The execution of the fault injection does not require the insertion of intrusive module into the NoC architecture, since modifying the configuration memory bit of the FPGA device thus physically inserting the desired fault performs the injection. This operation is performed thanks to the availability of the Configuration Access Port which is located internally to the device and can be controlled by a logic core; in our case by the processor 2.




Thanks to our solution the fault injection into the NoC architecture can be performed without intrusive modules affecting the real behavior and with optimal performances,

since the working frequency of the NoC is not drastically degraded by the fault insertion. Figure1. The main architectural scheme of the proposed approach. The rest of this paper is organized as follows. In Section II we present the main background concepts behind the implementation and testing of NoC. The description of the fault injection method, the developed architecture and the NoC fault models are presented in Section III. Section IV describes the testing routines developed for testing the router logic blocks and the NoC switches and interconnections. Fault injection results performed on a real NoC case study are presented in Section V. Finally, conclusions and future works are drawn in Section IV.

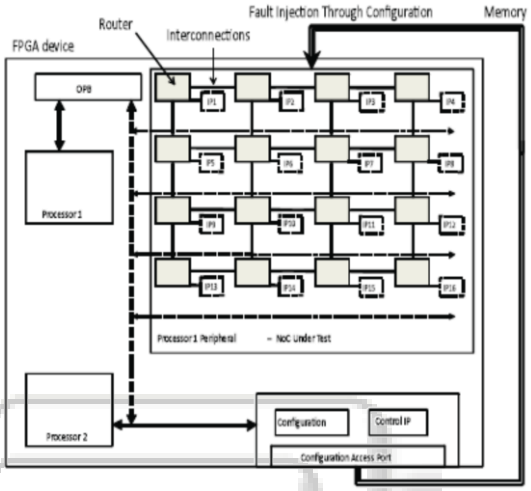



Figure 1. The main architectural scheme of the proposed approach.

## II. BACKGROUND

A Network on Chip is an interconnection architecture consisting of a 2-D mesh of routers each of which connected to a set of interconnection resources. An example of NoC structure is illustrated by the NoC under Test box in Figure 1. Each router may be connected to its four neighboring routers and to a set of other routers not located on its same row and column. Various NoC architectures have been proposed basing on the 2-D matrix of resources. \ll of them are characterized by several aspects including topology, routing algorithms, switching and flow control mechanisms. Several NoC architectures have been proposed in the past. The typical NoC design is based on the data exchange between the functional IP cores in the form of data packets. Depending on the adopted communication scheme, data packets are transmitted through routers and interconnections from the source to the destination IP port.

Different schemes have been proposed for NoC communication such as communication switching, virtual cut-through and wormhole switching. While communication switching is more applicable to small-size networks, virtual cut-through and wormhole switching are appropriate for large MPSoCs since data have to traverse large distances and packets are buffered by halfway routers on the routing path from the source to the destination. NoC architecture embeds two main resources: interconnections and routers. Interconnections are wire segments that link the various routers inside to the NoC array architecture, while routers are the most complex part of the NoC architecture. The details of a generic router are illustrated in the following section.

The architecture of a NoC router, which an example is illustrated in Figure 2, consists of a set of FIFO buffers forming the input and output data ports, a crossbar switch controlled by a logic circuitry that allow to implement the transportation methodology. A router generally consists of multiple buffer stages connected through the input and output ports to the routers placed on the same row (SR), column (SC) or on other locations (OL) of the considered router. Each input/output buffer stage form an input/output queue which is internally connected to a crossbar switch. The crossbar switch is the core of the router since it allows to form the links between the input and output queues in all the possible combinations. The connection between the input and output queues are managed by an arbitration circuitry, which on the basis of the adopted communication protocol routes the data packets.

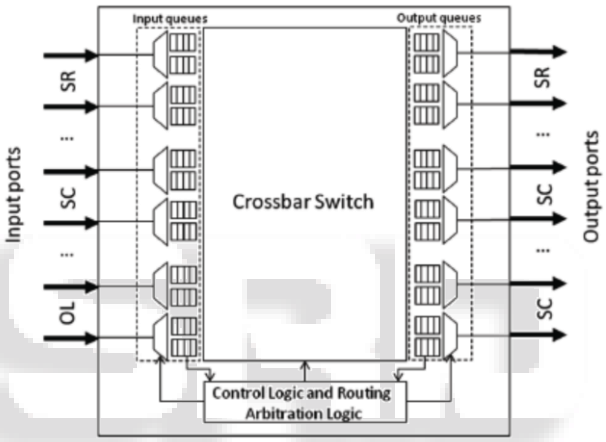



Figure 2. NoC router scheme including input and output registers, crossbar switch and routing and arbitration logic.

## III. THE PRAPOSED FAULT INJECTION METHOD

The environment of the proposed method consists of a host-PC which communicates to the FPGA board through a JTAG connection and a RS-232 serial cable. The method consists of the preliminary generation of the fault list performed on the host-PC by parsing the NoC net list and creating all the possible fault locations according to the used synthesis model. The fault locations are consequently transferred through the JTAG cable to the processor 2 dedicated memories. The fault injection execution flow is illustrated in Figure 3. It consists on the following principal modules:

*A. Fault Application:* the fault application module is executed by the processor 2 and consists on all the operations dedicated to the insertion of a fault into the NoC architecture. At first a fault location is read from the memory module, secondly, the fault location is converted into the correspondent FPGA's configuration memory coordinates that control the selected NoC resource. Finally, the processor 2 accesses to the FPGA's internal configuration access port facility and activate the reconfiguration of the configuration memory bits related to

the selected coordinates. During the modification of the FPGA's configuration memory, the NoC functionality is temporary freeze. This has not any impact on performance degradation of the NoC, since the freezing is synchronized with the microprocessor control clock.

*B. Configuration memory coordinates:* The configuration memory coordinates are the physical identification of the FPGA's configuration memory bits. Each configuration memory coordinate is associated to a correspondent sequence of FPGA's configuration memory bits.

*C. FPGA configuration memory:* The FPGA's configuration memory contains millions of SRAM cells that configure the behavior of the circuit mapped on the FPGA device. The main idea of the present work consists in acting on the configuration memory cells related to the behavior of the NoC architecture in order to insert a fault. Therefore, in order to perform the right fault injection it is necessary to know the exact correspondence between each configuration memory bit and the controlled FPGA's resource. The modification of the configuration memory is performed by the Internal Configuration Access Port (ICAP) controlled by the software running on the Processor 2. Through the ICAP port it is possible to modify selectively a single FPGA configuration frame in a small amount of time (dependent from the kind of FPGA device adopted).

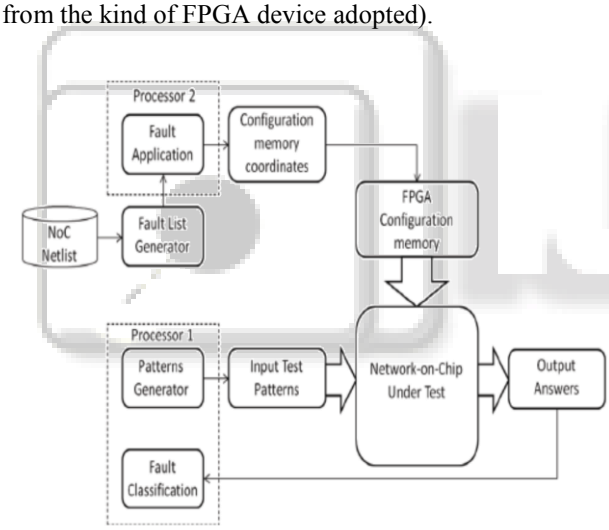



Figure 3. The fault injection execution flow of the proposed method.

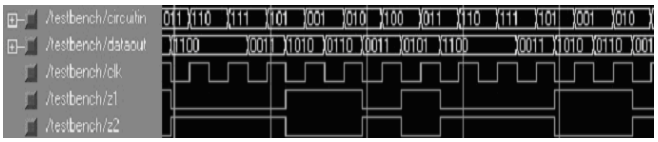
*D. Patterns generator:* The patterns generator aims at generating the test stimuli applied to the NoC. The stimuli are generated in the form of data packets transmitted from a source to a destination IP considering a NoC using a Wormhole transport methodology. The patterns are generated by the software running on the Processor 1. Each pattern consists of a signature composed by the identification of the source and destination IPs and by the complete data packet. The application of the test patterns is executed by the Processor 2 by executing the following steps: at first the signature is decoded individuating the source IP; secondly the Processor 2 access through the On-Chip Peripheral Bus (OPB) to the source IP and send the data packet; third, the signature is decoded individuating the destination IP and finally, the Processor 2 reads through the OPB bus the data packet received by all the IP (except to the source one).

*E. Fault classification:* The fault classification is executed by the Processor 2. The first action consists on capturing all the outputs of the IP destination ports. Secondly, the pattern signature is decoded individuating the destination IP.

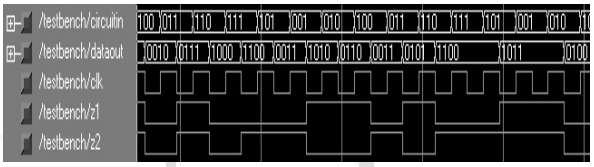
*F. Network-on-Chip under Test:* It consists on the architecture of the NoC under evaluation. The NoC model should be described in HDL language in order to facilitate the integration in our environment. The integration into the testing environment is performed by linking each NoC's port to the platform IP port.

## IV. SIMULATION

### A. Simulation without fault injection




### B. Simulation for testing with fault injection




## V. ADVANTAGE

The approach has several advantages: flexibility, observability and test speed. The approach has been implemented on an FPGA platform and a real NoC architecture using standard communication protocol has been tested. The experimental results demonstrated the effectiveness of the developed approach and make our approach suitable for testing large scale NoC design. ICs have been designed with dedicated point-to-point connections, with one wire dedicated to each signal. For large designs; in particular, this has several limitations from a physical design viewpoint. The wires occupy much of the area of the chip, and in nanometer CMOS technology, interconnects dominate both performance and dynamic power dissipation, as signal propagation in wires across the chip requires multiple clock cycles. NoC links can reduce the complexity of designing wires for predictable speed, power, noise, reliability, etc., Multi-core processor systems; a network is a natural architectural choice. A NoC can provide separation Between computation and communication, support modularity and IP reuse via standard interfaces, handle synchronization issues, serve as a platform for system test, and, hence, increase engineering productivity.

## VI. APPLICATION MULTI-CORE PROCESSOR SYSTEMS: A NETWORK IS A NATURAL ARCHITECTURAL CHOICE

Test approach based on a dual-processor system implemented on SRAM based FPGA which is able to test

mesh-based Network on Chips. Applicable for large scale network on chip.

REFERENCES

[1] S. Borkar, "Designing reliable systems from unreliable components: the challenges of transistor variability and degradation", IEEE Micro, Vol. 25, No. 6, pp. 10-16, November 2005.

[2] L. Chunsheng, V. Iyengar, S. Jiangfan, E. Cota, "Power-Aware Test Scheduling in Network-on-Chip Using Variable-Rate On Chip Clocking", IEEE International Very Large Scale of Integration Test Symposium , 2005, pp. 349 - 354

[3] B. Vermeulen, J. Dielissen, K. Goossens, C. Ciordas, "Bringing communications networks on a chip: test and verification implications", IEEE Communications Magazine, Volume 41, September, 2003, pp. 74 - 81.
[4] A. Kohler, G. Schley, M. Radetzki, "Fault Tolerant Network on Chip Switching With Graceful Performance Degradation", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 29, No. 6, June 2010, pp. 883 - 896.

[5] M. Nahvi, A. Ivanov, "Indirect Test Architecture for SoC Testing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 23, Issue 7,July 2004, pp. 1128 - 1142.

[6] Xilinx Product Specification, "Logic ORE IP XPS HIWCAP", Product Spec., DS586, June 22, 2011.
[7] T. Bjerregaard and S. Mahadevan, "A survey of research and practices of network-on-chip", ACM Computing Surveys, Vol. 38, pp. 1-51, March, 2006.

[8] J. Duato, S. Yalamanchili, L. Ni, "Interconnection Networks - An Engineering Approach", Morgan Kaufmann, 2002.

[9] C. Grecu, P. Pande, A. Ivanov, R. Saleh, "Timing Analysis of Network-on-chip Architectures for MP-SoC

[10] Platforms", Elsevier Microelectronics Journal, XX [10] L. Benini, D. Bertozzi, "Xpipes: Network on-chip architecture for gigascale systems-on-chip", IEEE Circuits and Systems Magazine, Volume 4, Issue 2, 2004, pp. 18-31.

[11] S. Pasricha, Y. Zou, D. Connors, H. J. Siegel, "OE+IOE: A novel turn model based fault tolerant routing scheme for networks-on-chip", IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, 2010, pp. 85 - 93

[12] H .Zimmer, A. Jantsch, "A fault model notation and error-control scheme for switch-to-switch buses in a network-on-chip", IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, 2003, pp. 188 - 193.

[13] E. Cota,"Power aware NoC Reuse on the Testing of Core-Based Systems", proceedings of the IEEE International Test Conference 2003, pp. 612 - 621.

[14] Yung-Chang Chang, Ching-Te Chiu, Shih-Yin Lin, Chung-Kai Liu, "On the Design and Analysis of Fault Tolerant NoC Architecture Using Spare Routers", International DAC Conference, 2011, pp. 431 - 436.

[15] L.Sterpone, M. Violante, "A new analytical approach to estimate the effects of SEUs in TMR architectures implemented through SRAM-based FPGAs", IEEE Transactions on Nuclear Science, Vol. 52, Issue 6, 2005,pp. 2217 - 2223.

[16] A. Perreira, J. P. Teixeir and M. Santos, "A Novel Approach to FPGA-based Hardware Fault Modeling and Simulation", IEEE International Workshop on Design and Diagnostic of Electronic Circuits and Systems, 2003, pp. 17 - 24.

[17] Reference to the Network-on-Chip emulator on www.opencores.org