Unveiling Power Reduction Techniques in VLSI Physical Design: A Comprehensive Review

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Abstract — As semiconductor devices become more complex, power consumption in VLSI physical design is a significant challenge. This paper examines power reduction approaches, focusing on multibit flip flops, gate resizing, multi-threshold voltage design, and clock gating. The goal is to reduce power while maintaining performance in high-performance, energy-efficient integrated circuits. This study aims to assess the effectiveness of power reduction techniques in VLSI architectures. It provides insights into the applicability and impact of multibit flip flops, gate resizing, multi-threshold voltage design, and clock gating. Multibit flip flops combine single-bit flip flops, resulting in area savings, reduced clock tree power, and minimized global congestion. Gate resizing optimizes gate sizes for a balance between power consumption and performance. Multi-threshold voltage design utilizes different voltage levels in different circuit sections to reduce power dissipation. Clock gating involves selectively disabling clock signals to inactive circuit elements, conserving power. By thoroughly examining these power reduction techniques, this research paper aims to contribute to the existing body of knowledge in VLSI physical design and provide valuable insights for designers and researchers in their quest for energy-efficient and high-performance integrated circuits.

Keywords: VLSI Physical Design, Power Reduction, Multibit Flip Flops, Gate Resizing, Multi-Threshold Voltage Design, Clock Gating

I. INTRODUCTION

A. *Types of Power Dissipation –*

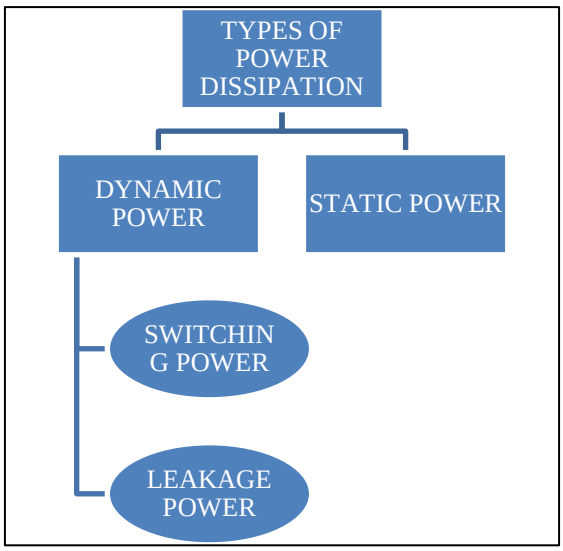

Fig. 1: Types of Power Dissipation

1) Static Power - Static power dissipation, also known as leakage power, occurs through mechanisms such as subthreshold leakage current between the source and drain and leakage between diffusion layers and the substrate.

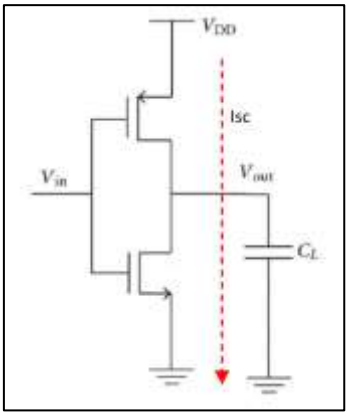

Fig. 2: Short circuit power

2) Dynamic Power - Dynamic power is consumed during circuit operation, depending on frequency, power supply, load capacitance, and includes switching and internal power components.

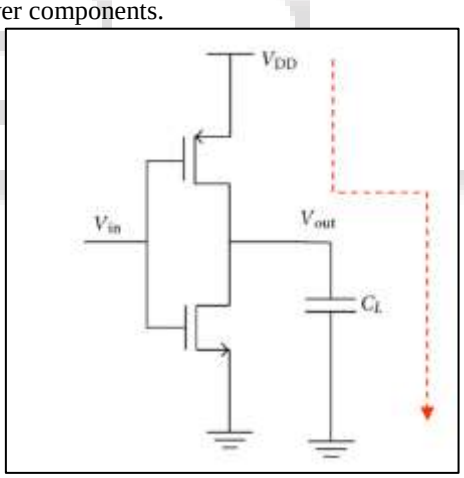

Fig. 3: Charging of Load

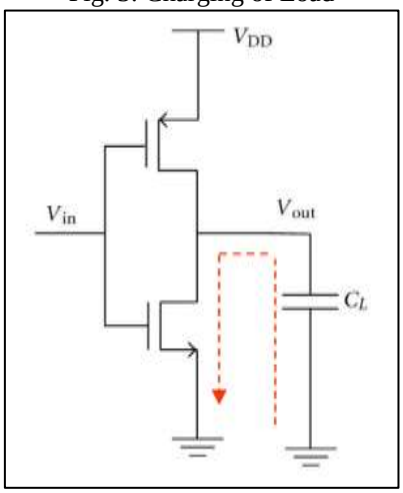

Fig. 4: Discharging of Load

1) Switching Power – (NET)

The switching power is the power dissipated when a circuit becomes active as a result of a stimulus causing a change in voltage on a net.

$$P_{switching} = a.f.C_{eff}.V_{dd}^2$$

In the given equation, "a" represents the switching activity, "Ceff" denotes the effective capacitance, "Vdd" signifies the supply voltage, and "f" represents the switching frequency.

2) Internal Power – (CELL)

The power dissipated during switching in a circuit includes energy consumption for charging and discharging internal capacitances, as well as power dissipation from transient short circuit paths.

$$P_{short\text{-}circuit} = I_{sc}.V_{dd}.f$$

Total power is the sum of the dynamic and leakage power.

$$\textbf{Total Power} = P_{switching} + P_{short\text{-}circuit} + P_{leakage}$$

Some of the techniques for achieving power optimized design are discussed below:

B. Multibit Flip flop

In ultra-deep submicron technology, merging single-bit flip-flops into multibit flip-flops offers several advantages. It provides increased driving strength of clock drivers, reduces duplicate inverters, lowers clock tree power, and enables area savings. Additionally, it helps in reducing global congestion. Multibit flops, featuring multiple D and Q pins, are widely used in ASIC designs to achieve power reduction without compromising performance.

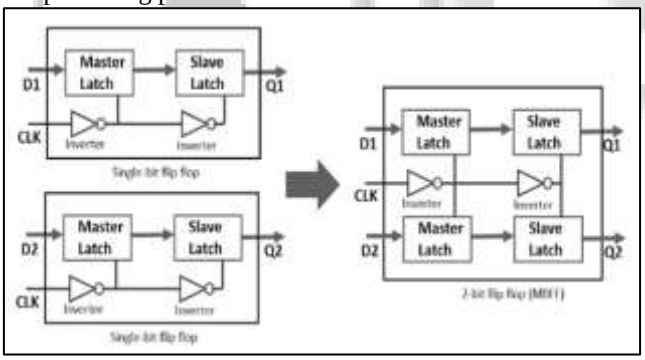

Fig. 1: Conversion of two Single Bit Flip Flops to One Multibit FIip Flop (MBFF)

1) Clock Tree Power Reduction: Merging single-bit flip-flops into multibit flops reduces switching capacitance (Cclk) and helps in lowering power consumption for the clock tree (Pclk) in ASIC designs.
2) Area Reduction: It reduces the overall number of flip-flops in the circuit.. As a result, the overall area of the circuit is reduced.
3) Global Congestion Reduction: Reducing the number of flip-flops decreases clock tree endpoints, reducing congestion in global routing resources. This leads to more efficient distribution of clock signals in the circuit.

Multibit flip flops reduce switching power, particularly in the context of clock tree power, by merging single-bit flip flops and reducing the number of sequentially clocked cells.

C. Gate Resizing

Gate resizing techniques in VLSI physical design not only equalize or minimize delays across all paths, including non-critical ones, but also optimize power consumption. By strategically adjusting gate sizes, timing disparities are reduced, and timing predictability is enhanced. This approach carefully manages the tradeoff between speed and static power dissipation, addressing power optimization concerns and achieving a more balanced distribution of delays throughout the circuit.

It focuses on minimizing the area, subject to delay <=Tspec

Delay of a gate g_i, denoted by d_i, in a standard cell library can be expressed by-

$$d_i = R_{out} * C_{out} + \tau_i = (R_u/w_e) * C_{out} + \tau_i.w_i + \tau_{i2}$$

where R_{out} is equivalent gate resistance , C_{out} is output capacitance and τ_i is intrinsic gate delay

$$Gate\ delay:\ g_i(w,z) = z/w$$

z is proportional to the size of the gate and w is proportional to size of driving gate.

Slack time calculation:

Source delay – maximum delay of a sub-path from primary input to the given lead

Required time – time at which signal on lead j required to be stable

$$Slack(g) = RT(j) - SD(j)$$

The load capacitance of gate G can be expressed as follows:

$$C_{load}(G) = \sum_{j \in fanout(G)} C_{gate}(j) + C_{wire}$$

where $C_{gate}(j)$ is the gate capacitance of j, and C_{wire} is the wiring capacitance of the output net. Since the gate capacitance is proportional to the gate area, the traditional approach for minimizing the power consumption has been to minimize the total gate area.

1) Timing-Driven Placement and Gate Sizing:

In timing-driven placement, gate sizing is determined before placement and remains fixed throughout the process to minimize wire length while satisfying timing constraints. Gate resizing and relocation are iteratively performed, considering area, delay, power consumption, and timing requirements. This approach achieves an optimized placement that meets timing specifications while considering tradeoffs between design metrics.

2) Delay Optimization:

In delay optimization, the delay constraints are imposed on the gates present in a timing path. The objective is to ensure that the total delay of the path meets the desired timing specifications. If the delay constraint is satisfied, the optimization process is completed. However, if the delay constraint is not met, the most critical gate in the timing path is selected for resizing or other optimization techniques to improve the delay and meet the timing requirements.

3) Power Optimization under Delay Constraint:

In power optimization with a constraint on delay, the gates are organized in a list. If the list is empty, indicating that all gates have been optimized, the optimization process is finished. Otherwise, the gate with the minimum criticality is identified, and resizing is applied to reduce power consumption. If the resulting delay violates the constraint, the

gate is removed from the list to ensure the circuit meets the desired timing specifications while optimizing power consumption.

Timing-driven placement and gate sizing optimize wire length and timing constraints through iterative resizing and relocation of gates. Delay optimization ensures timing specifications are met by selectively resizing critical gates. Power optimization under a delay constraint reduces power consumption through gate resizing and removal. These techniques enhance VLSI design efficiency and performance.

D. Multi-threshold (Vth) CMOS MTCMOS circuits

MTCMOS (Multi-Threshold CMOS) is a power reduction technique in CMOS circuits that addresses leakage and standby power. It utilizes different threshold voltage levels for various circuit states. Higher thresholds minimize leakage during idle or standby, while lower thresholds improve performance in active mode.

By utilizing higher threshold voltages during idle states, leakage current is effectively reduced, conserving power during standby periods. In contrast, lower threshold voltages are used during active operation to meet high-performance requirements, enabling faster transistor switching and reducing propagation delays.

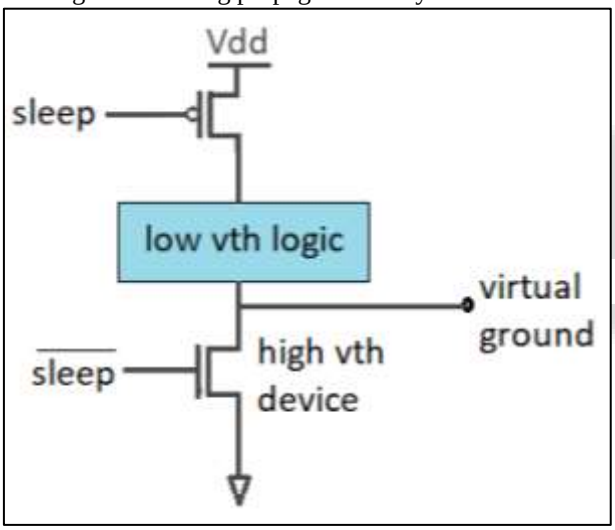

Fig. 2: MTCMOS

Also the different vth cells can be used in different power domains which can reduce Vdd and can effectively decrease power consumption. HV modules, which operate at a higher Vdd, tend to use high-voltage transistors (HVt) that have lower subthreshold leakage currents, leading to lower static power dissipation. On the other hand, LV modules, operating at a lower Vdd, may employ low-voltage transistors (LVt) that have higher subthreshold leakage currents but lower dynamic power dissipation due to the reduced supply voltage.

By leveraging the benefits of HVt and LVt transistors in the respective domains, power consumption can be optimized. The reduction in supply voltage for LV modules results in decreased dynamic power dissipation, while the use of HVt transistors in HV modules helps reduce static power dissipation.

E. Clock gating

The clock distribution network in integrated circuit (IC) design contributes significantly to power consumption, with up to 40% attributed to it. Clock gating is a technique used to reduce power in the clock tree by inserting clock gates. These gates selectively control the clock signal, shutting off parts of the clock tree when not needed. Dynamic gating enables all registers to latch data, while idle gating conserves power during periods of inactivity. By employing clock gating, unnecessary clock transitions and toggling of registers are prevented, reducing dynamic power consumption in the clock distribution network. The decision to use gated or ungated clocks depends on the specific logic in the System-on-Chip (SoC) design, allowing for effective power management and optimization.

There are two primary types of clock gating cells:

1) Clock gating using AND gate: This type of clock gating cell involves the use of an AND gate to control the clock signal. The AND gate acts as a switch, enabling or disabling the clock to specific parts of the circuit based on certain conditions or control signals.

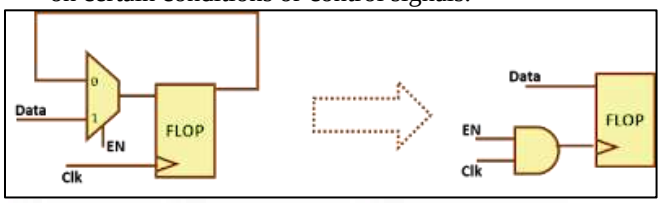

Fig. 3: Usage of AND Gate for Clock Gating

2) Integrated clock gating cell: This type of clock gating cell is a dedicated component designed specifically for clock gating. It typically consists of flip-flops, logic gates, and control signals. Integrated clock gating cells provide more advanced and efficient clock gating capabilities, allowing for finer control and optimized power savings in the circuit.

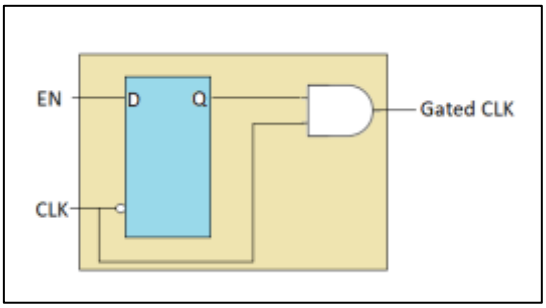

Fig. 4: ICG (Integrated Clock Gating Cell)

These clock gating cells play a crucial role in reducing power consumption by selectively controlling the clock signal and preventing unnecessary clock transitions and toggling of registers. By implementing appropriate clock gating techniques, designers can effectively manage power consumption and optimize power usage in integrated circuits.

II. CONCLUSION:

This review highlights key power reduction techniques in VLSI physical design: multibit flip flops, gate resizing, multi-threshold CMOS (MTCMOS), and clock gating. Multibit flip flops save area and reduce clock tree power. Gate resizing optimizes gate sizes for a balanced power-performance tradeoff. MTCMOS uses multiple threshold voltage levels for

power reduction. Clock gating selectively disables clock signals to save power. This research paper contributes to knowledge in energy-efficient integrated circuits and provides valuable insights for designers and researchers. Further research is needed to meet demand for high-performance, energy-efficient designs. Continuous exploration and advancement of these techniques will lead to greater power optimization and sustainable VLSI physical designs.

REFERENCES

[1] Girard, P. & Landrault, Christian & Pravossoudovitch, S. & Severac, Daniel. (1997). A gate resizing technique for high reduction in power consumption. 281- 286.
[2] Y. -S. Wang and C. -H. Cheng, "A hierarchy multiple-voltage design technique for low-power performance-manageable bio-chips," 2016 IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW), Nantou, Taiwan, 2016, pp. 1-2.
[3] Gautam, Saurabh. (2014). Analysis of multi-bit flip flop low power methodology to reduce area and power in physical synthesis and clock tree synthesis in 90nm CMOS technology. Proceedings of the 2014 International Conference on Advances in Computing, Communications and Informatics, ICACCI 2014. 570-574.
[4] Chuang, Weitong & Hajj, I.N.. (1994). Delay and area optimization for compact placement by gate resizing and relocation. 145-148.
[5] H.F. Jyu, S. Malik, S. Devadas and K. W. Keutzer, "Statisti cal Timing Analysis of Combinational Logic Circuits," IEEE Trans. VLSI Systems, Vol. 1, No. 2, pp.126-137, June 1993.
[6] Girard, P. & Landrault, Christian & Pravossoudovitch, S. & Severac, Daniel. (1997). A gate resizing technique for high reduction in power consumption. 281- 286.
[7] B. Tan, W. Lee, K. Mok and H. Goh, "Clock gating implementation on commercial Field Programmable Gate Array (FPGA)", Proceedings of the 4th International Conference on Electrical, Electronics and System Engineering (ICEESE), Kuala Lumpur, Malaysia, (2018) pp. 102-106.
[8] T. S. Kiong and N. Soin, "Physical aware low power clock gates synthesis algorithm for high speed VLSI design," 2009 International Conference for Technical Postgraduates (TECHPOS), Kuala Lumpur, Malaysia, 2009, pp. 1-5.
[9] Dushyant Kumar Sharma, Effects of Different Clock Gating Techniques on Design, International Journal of Scientific & Engineering Research, Vol. 3, Issue 5, May-2012
[10] Srinivas Devadas and Sharad Malik, "A survey of optimization techniques targeting low power VLSI circuits", Proceedings of the 32nd Design Automation Conference, San Francisco, CA, (1995) pp. 242- 247
[11] V. Chickermane, P. Gallagher, J. Sage, P. Yuan and K. Chakravadhanula, "A Power-Aware Test Methodology for Multi-Supply Multi-Voltage Designs," 2008 IEEE International Test Conference, Santa Clara, CA, USA, 2008, pp. 1-10

