A Nobel Design of An Efficient Decimator using Matlab Simulink

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Abstract— The need to process data at more than one sampling rate is increasing in modern digital systems. Through this paper we are presenting the various techniques of altering the sampling rate in a multi rate system and we have also discussed the filter requirements for efficient output of the decimator for the professional recording production equipment application having a sampling rate of 96 kHz. We have also compared the total storage requirements (TSR) and multiplications per second (MPS) requirements at each stage of decimator using Matlab Simulink.

Key words: Digital Signal Processing, Filters, Multirate, Decimation, Interpolation And Matlab Simulink

I. INTRODUCTION

In many digital Signal Processing applications we need to change the sampling frequency as per the requirement. The frequency of occurrence of a sample i.e. sampling frequency of a signal can be varied, by using Multi Rate System. A multi Rate system may have different sampling rates at different stages of process by allowing the sampling frequency to be decreased or increased without significant undesirable effects of errors such as quantization and aliasing [2]. The existing signal sampled at a different sampling rate can be converted to the desired sample rate signal by one of the following techniques-

- Up Sampling
- Down Sampling
- Resampling

A. Up Sampling-

If the sampling rate of the existing signal is an integer multiple of the sampling rate of desired signal then up sampling is employed. The process of increasing the number of samples in the signal by an up sampling factor L, where L is a positive integer, is called up sampling [5], and the device performing this operation is called an up-sampler or sampling rate expander or simply expander.

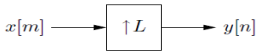

Fig. 1: Block diagram representation of an up-sampler

An up- sampler pads L-1 zeros between every two consecutive input samples as we are increasing the number of bits in the signal it is also known as Bit Stuffing[*], that means an up sampled signal in time domain is equivalent to division of time by the up sampling factor L, as per the relation

$$y[n] = \begin{cases} x[\frac{n}{L}] & \text{when } \frac{n}{L} \in \mathbb{Z} \\ 0 & \text{else.} \end{cases}$$

B. Down Sampling-

If the sampling rate of the existing signal is a factor of the sampling rate of desired signal then down sampling is required. The process of reducing the number of samples in the signal is called down sampling [5], and the device performing this operation is called a down-sampler or sampling rate compressor or simply compressor.

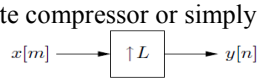

Fig. 2: Block diagram representation of a down-sampler

The down sampling factor (commonly denoted by *M*) is usually an integer or a rational fraction greater than unity. This factor multiplies the sampling time or, equivalently, divides the sampling rate [6]. A down sampler eliminates the M-1 samples in between the input sampled signal and only keeps samples occurring at an integer multiple of M and thus equivalent to multiplication of the time by the down sampling factor M and can be given by the relation

$$y[n] = x[nM]$$

C. Resampling-

Resampling is usually done to interface two systems whose sampling rate ratio is not equal to some integer value. Resampling can be achieved by cascading an up sampler followed by a down sampler.

Up sampling is reversible whereas down sampling is irreversible, because in up-sampling we are adding zero samples in the input sampled signal whereas in down sampling we are eliminating the samples which cannot be retrieved later. Resampling is reversible only when the up sampling factor and down sampling factor are co-prime to each other which means that we can exchange the positon of up sampler and down sampler without affecting the output.
For L factor up sampler the z-transform of up sampled signal can be written as-

$$Y(z) = \sum_n y[n]z^{-n} = \sum_{n:\frac{n}{L}\in\mathbb{Z}} x\left[\frac{n}{L}\right]z^{-n} = \sum_k x[k]z^{-kL} = X(z^L)$$

Substituting $z = e^{jw}$ for the DTFT

$$Y(e^{j\omega}) = X(e^{j\omega L})$$

L factor up sampling leads to L-fold repetition of X (e^{jw}) which means that in our baseband signal we are getting L-1 additional images of the spectrum of the original signal. This phenomenon is known as imaging [1]. Thus the spectrum of the original signal which is band limited to the low frequency region is no more band limited after up-sampling because of the insertion of zero valued samples between the nonzero samples of the original signal. Thus a filter is needed to remove these images or we can say to band limited the signal. This up sampling followed by filtering is called interpolation as shown as figure

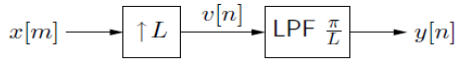

Fig. 3: Filter in Interpolator

While doing the down sampling Nyquist criteria should be kept in mind and the spectrum of baseband should be confined in a limit of π/M, where M is the down sampling factor [1]. If the spectrum exceeds this limit aliasing takes place. To restrict the original signal within the limits a Low Pass filter having its stopband frequency equal to π/M is imposed before down sampling and this technique is known as decimation as depicted in the diagram below.

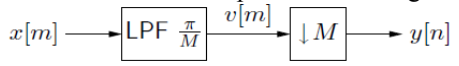

Fig. 4: Filter in decimator

In resampling a Low Pass Filter can be employed in between the up sampler and the down sampler having its transfer function equal to product of the anti-imaging filter of interpolator and antialiasing filter of decimator i.e. $H_{Re}(z)=H_u(z)* H_d(z)$,.having its cut-off frequency equal to $\omega_s= \min(\pi/L, \pi/M)$.

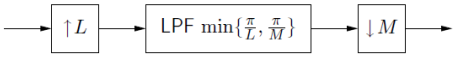

Fig. 5: Filter in resampling

A Multi Rate system comprises a decimator or (and) interpolator. The function of decimator is complimentary to interpolator. By incrementing or decrementing the sample rate we are actually varying the size of data accordingly.

D. Design of Practical Sampling Rate Converters

On the practical ground we may follow the following steps for sampling rate conversion-

- Specifying the overall anti-aliasing or anti-imaging filter requirements.
- Determine the optimum number of stages of decimation or interpolation that will yield the most efficient implementation.
- Determine the decimation or interpolation factor for each stage.
- Design an appropriate filter for each stage.

Our main aim is to prove that for the design of a single stage decimator, the order of Low Pass Filter is very high and practically very hard to achieve, thus a multi stage approach is used in design of a decimator. When large changes in the sampling rate are required it is more efficient to change the rate in two or more stages than in one single stage. If M>>1, the multistage approach leads to much reduced computational and storage requirements with a relaxation in the characteristics of the filters used in decimation and consequently results as the filters which are less sensitive to finite word length effects. However, these advantages are achieved at the expense of increased difficulty in the design and the implementation of the systems. The overall decimation factor M can be expressed as the product of small decimation factors:

$$M = M_1M_2\ldots..M_n$$

For a multistage decimator, the filter requirements for each stage to avoid aliasing after rate reduction are:

passband	$0 \leq f \leq f_p$
stopband	$(F_i - F_s/2M) < f < F_{i-1}/2, \quad i = 1, 2, \ldots, I$
passband ripple	δ_p/I
stopband ripple	δ_s
filter length	$N \approx \frac{D_\infty(\delta_p, \delta_s)}{\Delta f_i} - f(\delta_p, \delta_s)\Delta f_i + 1$

Where F_i is output sampling frequency at i^{th}stage, N is filter length and Δf_i is normalized transition width for the i^{th}stage decimator.

$$D_\infty(\delta_p, \delta_s) = (\log_{10}\delta_s)[a_1(\log_{10}\delta_p)^2 + a_2(\log_{10}\delta_p) + a_3] + a_4(\log_{10}\delta_p)^2 + a_5(\log_{10}\delta_p) + a_6$$

where

$$a_1=5.309 * 10^{-3},\ a_2 = 7.114*10^{-2},\ a_3 = -0.4761,\ a_4 = -2.66*10^{-3},\ a_5 = -0.5941,\ a_6 = -0.4278$$

$$f(\delta_p, \delta_s) = 11.01217 + 0.51244(\log_{10}\delta_p - \log_{10}\delta_s)$$

δ_p is the passband ripple or deviation and δ_s is the stop band ripple or deviation [2].

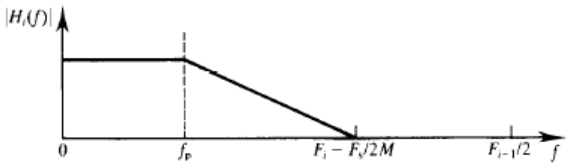

Fig. 6: Filter specification for stage i, i=1, 2, 3…I

Multirate design yields significant reduction in both computation and storage requirements over a single stage design. The efficient saving can be achieved by the choice of no. of stages and the decimation factor for the individual stages. Efficiency of the multirate design may be defined in terms of number of multiplication per second (MPS) or total storage requirement (TSR) for the coefficients.

$$\text{MPS} = \sum_{i=1}^{I} N_i F_i$$

$$\text{TSR} = \sum_{i=1}^{I} N_i$$

Where N_i is the number of filter coefficients for i^{th} stage, F_i is the output sampling frequency for i^{th} stage.

II. Block Modeling of Decimator

A. Single Stage Decimator (I=1):

In this single stage FIR Filter model, the sampling rate of a signal x (n) is to be reduced by decimation from 96 KHz to 1 KHz. The highest frequency of interest after decimation is 450 Hz. The block diagram and filter specification and response are given in figure

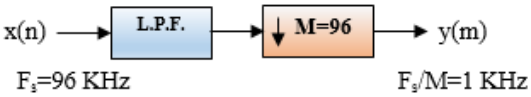

Fig. 7: Block diagram of single stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	96
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	0.50
5.	Passband Attenuation (linear)	0.01
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	4880

Table 1: Filter specification of single stage decimator

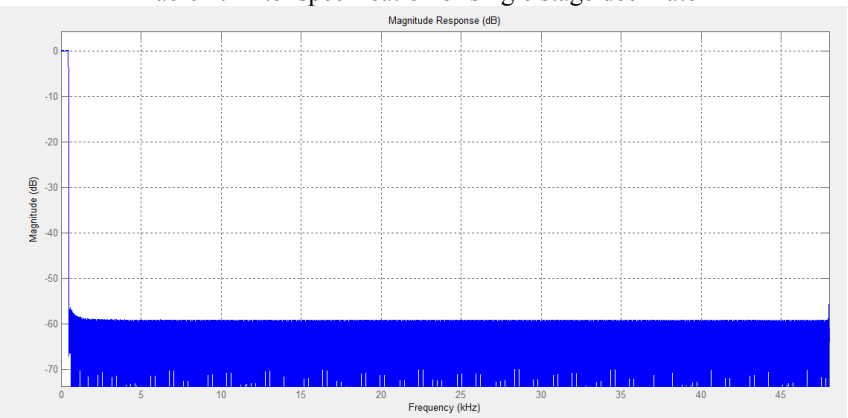

Fig. 8: Frequency Response of single stage FIR Filter

B. Two Stage Decimator (I=2)

In this two stage FIR Filter model, the sampling rate of a signal x (n) is to be reduced by decimation from 96 KHz to 1 KHz in two stages. The optimum integer decimation factor for I=2 are M_1=32 and M_2 =3.At the first stage the sampling rate is reduced by 32 to 3 KHz and second stage is further reduced by 3 to 1 KHz. The block diagram and filter specification and responses are given in figure

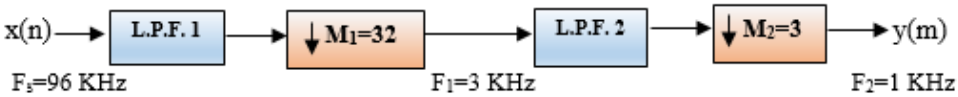

Fig. 9: Block diagram of two stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	32
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	2.50
5.	Passband Attenuation (linear)	0.005
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	130

Table 2: Filter specification of L.P.F. 1 of two stage decimator

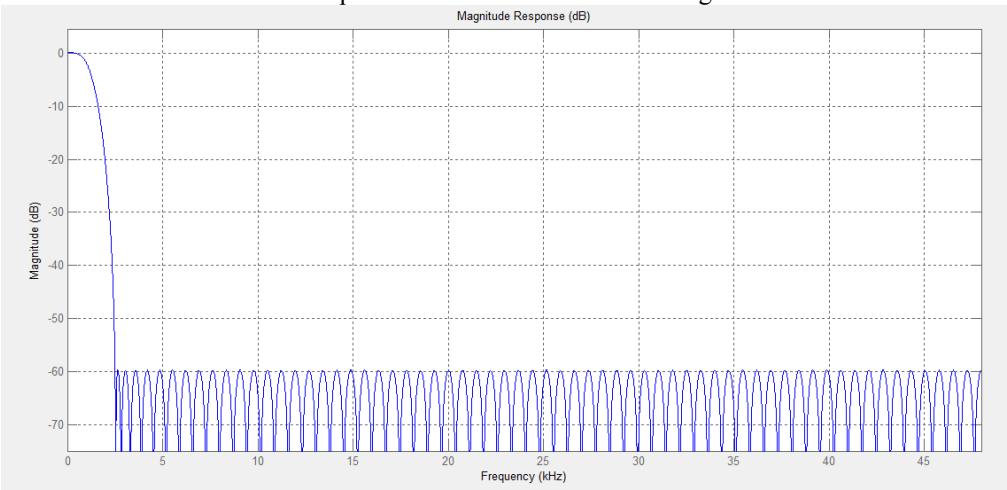

Fig. 10: Frequency Response of L.P.F. 1 of two stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	3
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	0.50
5.	Passband Attenuation (linear)	0.005
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	166

Table 3: Filter specification of L.P.F. 2 of two stage decimator

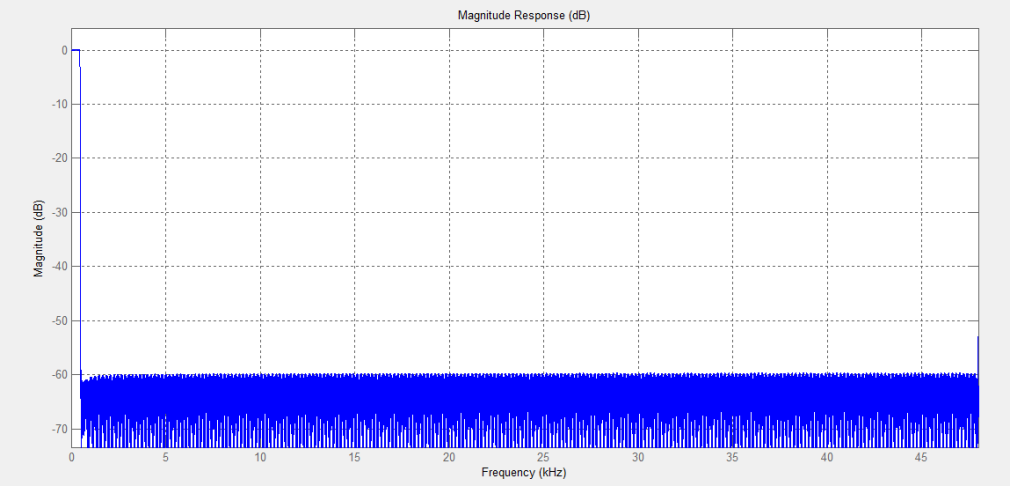

Fig. 11: Frequency Response of L.P.F. 2 of two stage decimator

C. Three Stage Decimator (I=3):

In this three stage FIR Filter model, the sampling rate of a signal x (n) is to be reduced by decimation from 96 KHz to 1 KHz in three stages. The optimum integer decimation factor for I=3 are M_1=8, M_2 =6 and M_3=2. The block diagram and filter specification and responses are given in figure

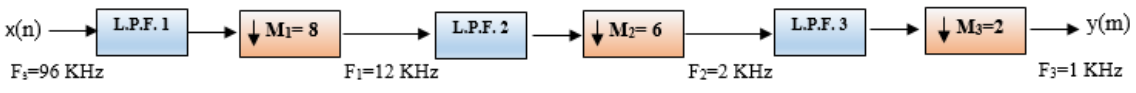

Fig. 12: Block diagram of three stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	8
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	11.500
5.	Passband Attenuation (linear)	0.0033
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	24

Table 4: Filter specification of L.P.F. 1 of three stage decimator

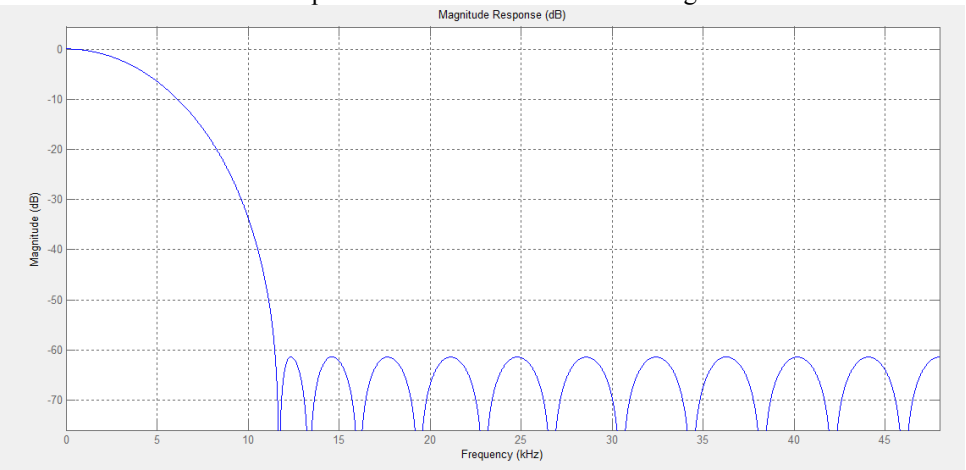

Fig. 13: Frequency Response of L.P.F. 1 of three stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	6
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	1.50
5.	Passband Attenuation (linear)	0.0033
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	33

Table 5: Filter specification of L.P.F. 2 of three stage decimator

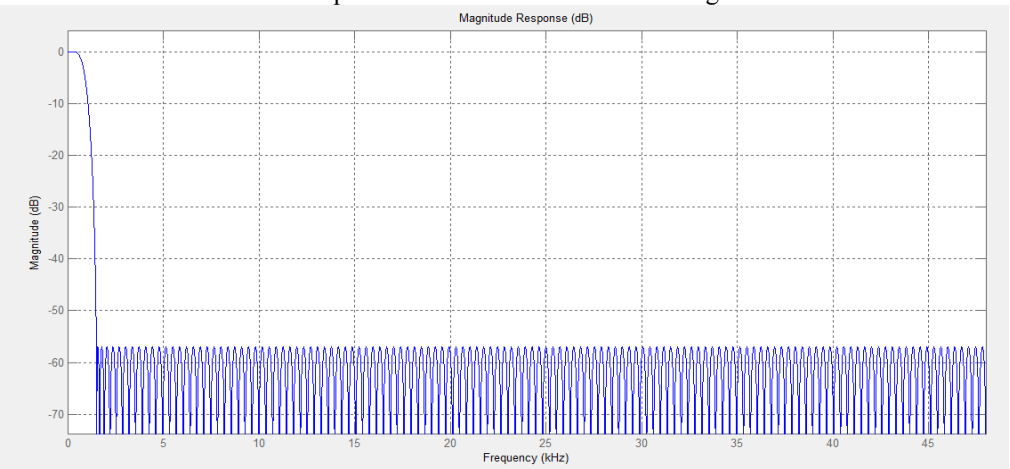

Fig. 14: Frequency Response of L.P.F. 2 of three stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	2
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	0.50
5.	Passband Attenuation (linear)	0.0033
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	116

Table 6: Filter specification of L.P.F. 3 of three stage decimator

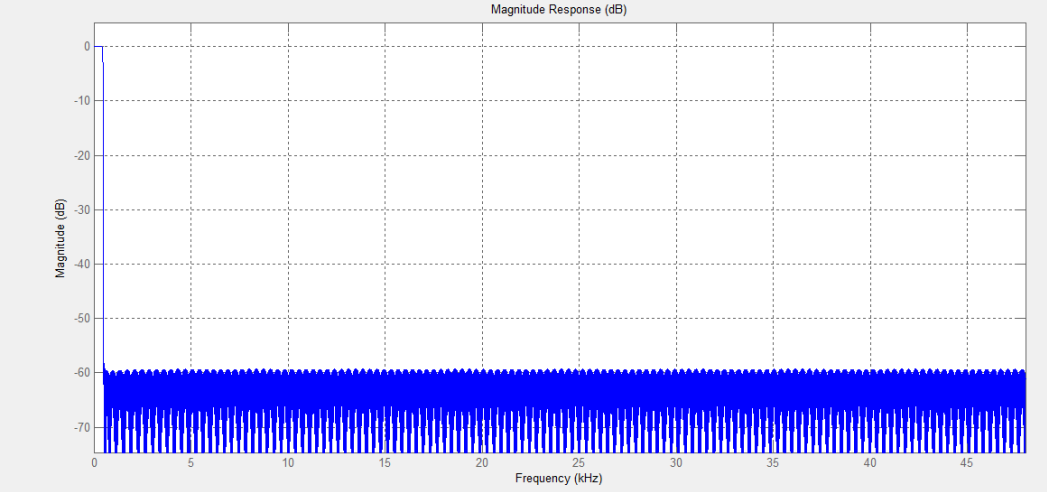

Fig. 15: Frequency Response of L.P.F. 3 of three stage decimator

D. Four Stage Decimator (I=4):

In this three stage FIR Filter model, the sampling rate of a signal x (n) is to be reduced by decimation from 96 KHz to 1 KHz in four stages. The optimum integer decimation factor for I=4 are M_1=4, M_2 =4, M_3=3 and M_4=2. The block diagram and filter specification and responses are given in figure

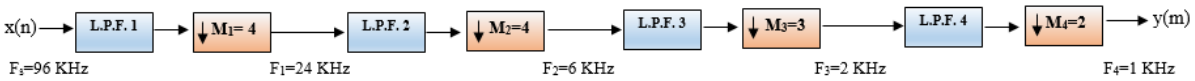

Fig. 16: Block diagram of four stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	4
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	23.50
5.	Passband Attenuation (linear)	0.0025
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	10

Table 7: Filter specification of L.P.F. 1 of four stage decimator

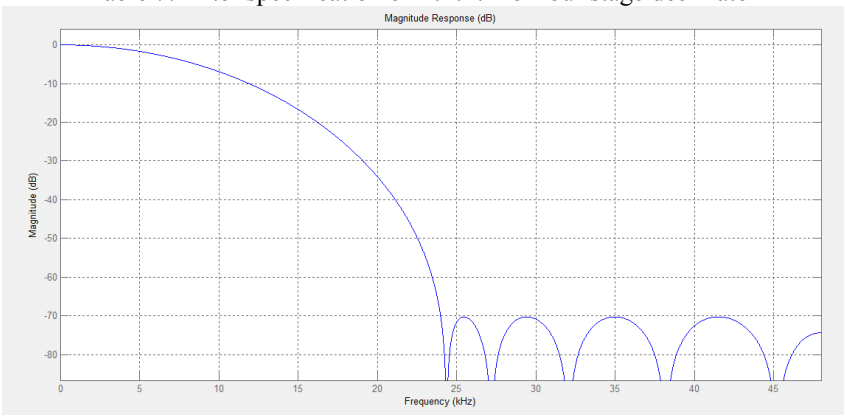

Fig. 17: Frequency Response of L.P.F. 1 of four stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	4
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	5.5
5.	Passband Attenuation (linear)	0.0025
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	12

Table 8: Filter specification of L.P.F. 2 of four stage decimator

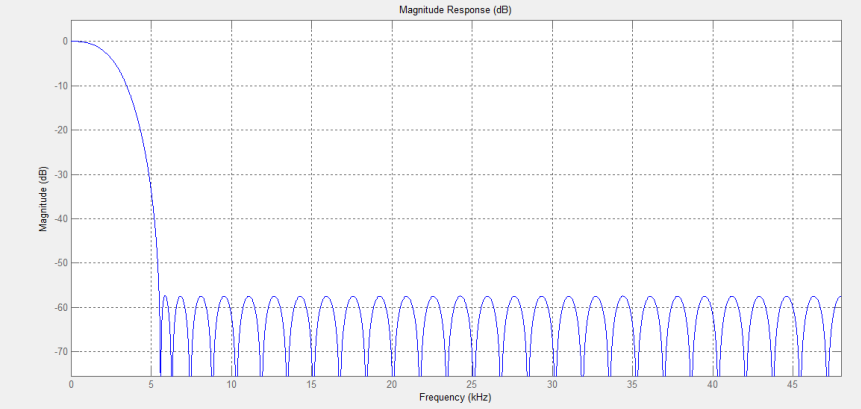

Fig. 18: Frequency Response of L.P.F. 2 of four stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	3
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	1.5
5.	Passband Attenuation (linear)	0.0025
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	16

Table 9: Filter specification of L.P.F. 3 of four stage decimator

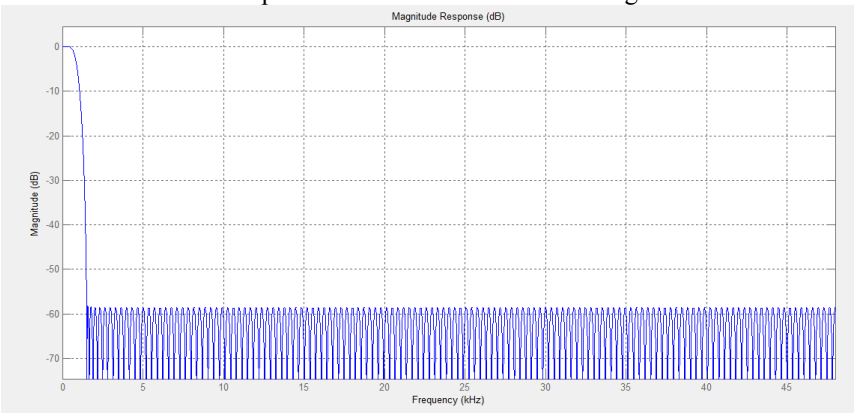

Fig. 19: Frequency Response of L.P.F. 3 of four stage decimator

S.No.	Filter Specification	Values
1.	Sampling Frequency (KHz)	96
2.	Decimation factor	2
3.	Passband edge Frequency (KHz)	0.45
4.	Stopband edge Frequency (KHz)	0.50
5.	Passband Attenuation (linear)	0.0025
6.	Stopband Attenuation (linear)	0.001
7.	Order of Filter	119

Table 10: Filter specification of L.P.F. 4 of four stage decimator

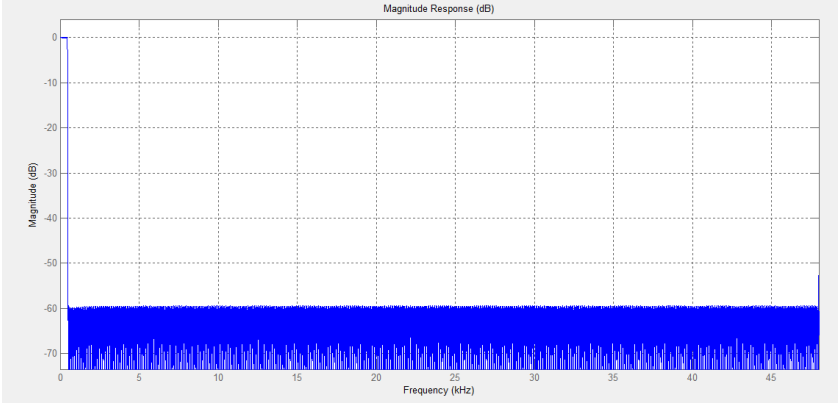

Fig. 20: Frequency Response of L.P.F. 4 of four stage decimator

III. CONCLUSION

No. of Stages	N_1	N_2	N_3	N_4	M_1	M_2	M_3	M_4	F_1	F_2	F_3	F_4	MPS	TSR
1	4881	-	-	-	96	-	-	-	1000	-	-	-	4881000	4881
2	131	167	-	-	32	3	-	-	3000	1000	-	-	560000	298
3	25	34	117	-	8	6	2	-	12000	2000	1000	-	485000	176
4	11	13	17	120	4	4	3	2	24000	6000	2000	1000	496000	161

Table 1: Conclusion

We can significantly reduce both the computation and storage requirement as compared to single stage design. At early stages the wide transition of filter causes the reduction in the order of the filter. On comparing the efficiencies of multi-stages filter design we can observe the computation (MPS) and storage (TSR) requirements are significantly reduced with the number of stages. The difference in the order of the filter is greatest on going from one stage decimator to two stages decimator. However, there are noticeable reductions in the storage requirement on switching from two stages to three stages decimation. But on going from three stages to four stages the computations are increasing. Overall three stages decimation is appearing as the best of available choices but while practically implementing hardware and software requirements should be kept in mind.

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