

# Design of Frequency Multiplier at 120 GHz for Sub-Millimeter Wave LO Development

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**Abstract**— In this paper we report the schematic design, layout and results of a high output power balanced tripler at 120 GHz, in which a pair of UMS BES schottky diode is adopted. The design process involves a systematic study of the various parameters such as anode size, diode doping, circuit configuration, circuit topology etc. Considering the present situation of domestic processing technology, the advantage of balanced tripler is this it cannot require any bias, means the design is a self-bias. Here we use antiparallel configuration of diode pair to design a tripler. This configuration has the distinct advantages that only odd harmonics are generated. So requirement and complexity to design a matching network is decreased in this design. The measured schematic results indicate that the output power is 1 dBm at 120 GHz when driven with 15 dBm at 40 Hz of input power. In general, this tripler has important practical value.

**Key words:** Schottky Diode, Frequency Multiplier, Harmonic Balance Technique, Submillimeter-Wave Multipliers

## I. INTRODUCTION

Currently there is a demand for wide bandwidth, high frequency and sufficient power source with outputs above 1 THz for use in submillimetre wave Heterodyne receivers. In astrophysics, heterodyne spectrometers are needed to measure Doppler velocities in the interstellar medium and star forming regions with resolutions typically around 1 km/s [2]. Measurements at frequency ranging from below 100 GHz to at least 5 THz are needed to identify the spectral signatures of a wide range of molecules, isotopomers, atoms and ions, as well as to measure such physical properties as the temperature, density, pressure, mass and dynamics of the systems observed [4]. To extract this information from the received RF signal, requirement is that to convert this high frequency to low frequency. For this purpose, the front end of a heterodyne receiver includes a down converting element and the local oscillator which provides the frequency to mix with RF signal of interest. In the drive to realize solid state heterodyne mixers for space applications at frequencies above 1THz, the provision of sufficient local oscillator power is a critical issue. To realize the LO from solid state sources cascaded frequency multiplier stages are a practical solution. Schottky diode based frequency multipliers play a vital role in developing all solid state power sources at Terahertz frequency range.

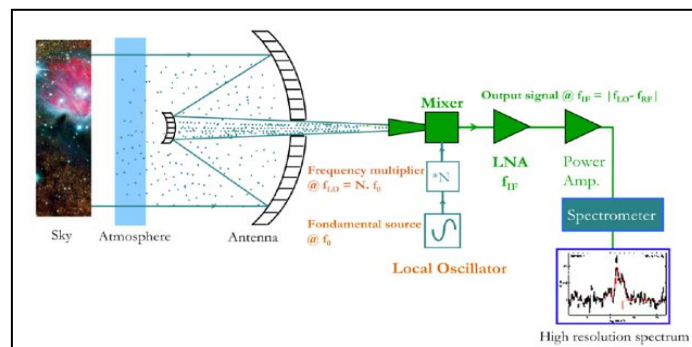


Fig. 1: (Heterodyne Receiver)

First multipliers are designed using whisker contacted diodes, frequency multipliers have recently been developed with the preferred, more reliable, more reproducible, and easier to assemble, planar MMIC technology. Improvements in GaAs processing technology, have allowed for the design of GaAs schottky varactor multipliers up to the higher end of the submillimetre-wave range. However, the development of local oscillators (LO) with the desired wide bandwidth and high power levels remains very challenging [4]. We believe that the work presented in this paper is a major step in meeting this challenge. This paper will address some of the constraints that are placed on designs for the high frequency tripler at 120 GHz and will address the methodology involved in designing circuit.

## II. SCHOTTKY DIODE BASED FREQUENCY MULTIPLIER

In the last several years, tremendous progress has been made in understanding and realizing diode frequency multipliers that can produce useful amounts of power in the terahertz range. Diode frequency multipliers utilize the reactive and/ or resistive nonlinearity of the diode to generate harmonics of an input signal. By providing appropriate impedance matching at each integer multiple of the input frequency, it is possible to design frequency doublers, triplers, or even quintuplers [2]. While

diode structures incorporating heterostructures have made significant advances, the GaAs schottky diode continues to be the dominant technology for terahertz frequency multipliers. This article will focus on this technology.

A number of related technologies advances have combined to make this progress possible. Firstly, device technology has moved away from discrete chips mounted on hybrid circuits to MMIC like circuits on thin semiconductor membranes. Secondly, the commercialization of accurate full 3-D finite-element-model(FEM) field simulators and fast harmonic-balance codes have made possible the design of broad-band, fixed tuned circuits featuring multiple anodes for improved bandwidth and power handling. To meet the need for broadband terahertz sources, GaAs Schottky diodes on membranes a few micrometers thick have been developed.

Frequency multiplier design mainly divide into 3 parts. (I) diode structure (II) input matching network and (III) output matching network. Here diode structure is the heart of the frequency multiplier, using these harmonics is generated.

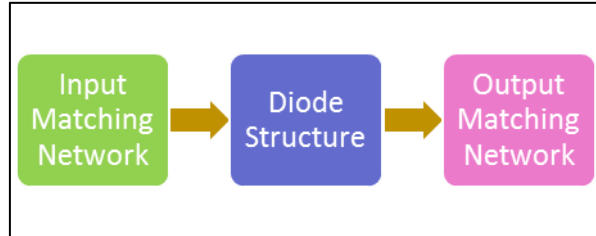


Fig. 2: (Frequency Multiplier Block Diagram)

### III. DESIGN METHODOLOGY

A common method employed to design and optimize diode multiplier circuits is to first optimize the diode parameters using nonlinear simulation tool such as harmonic balance. The diode impedance is then properly matched to the input and output circuits utilizing linear circuit synthesis. This approach is relatively fast and has shown to work very well with balanced triplers in the sub-THz range [4], since the input and output circuits can be optimized independently. However, in our approach we have exclusively used non-linear codes to simultaneously optimize the input, output and the idler frequency for designing of the triplers to 120 GHz. Though, these places further burden on the computational hardware, it allows one to simultaneously optimize the diode physical structure along with the embedding circuitry for maximum advantages. [4, 2]

#### A. Diode Model

The thumb rule of any circuit design is that the device used to design a circuit has a cut-off frequency three times higher than the operating frequency of the circuit. UMS foundries BES process schottky diode has a cut-off frequency 3 THz. Junction capacitance  $C_j(0) = 0.246 \text{ fF}$  and series resistance  $R_s = 21.9\Omega$ , in our design we are using this diode.

The practical limit of the output power of a frequency multiplier is typically either the power beyond which conversion efficiency drops off due to saturation effects or device lifetime becoming unacceptably short due to thermal or reverse breakdown effects. To increase power handling, the device doping can be optimized and the number of anodes per chip can be increased [8]. However, there is a practical limit to the number of anodes based on the chip size, the device impedance, and coupling efficiency. As the number of anodes is increased, compromises must be made between an optimum and even input coupling to the anodes, an optimum matching of each anode at the idler frequencies and optimum matching at the output frequency.

#### B. The Tools

An AD (Advanced Design System) was used for the non-linear simulation and optimization. Harmonic balance (HB) simulator is used for nonlinear circuit performance measurement to find out the solution in frequency domain.

#### C. Topology of Diode Structure

- 1) Common balanced tripler: In this configuration diodes are connected in series. Biasing network is required in this design topology.
- 2) Unbalanced tripler with bias: In this design configuration diodes are connected in parallel form
- 3) Balanced tripler without bias: In this design configuration diodes are connected in anti-parallel form.

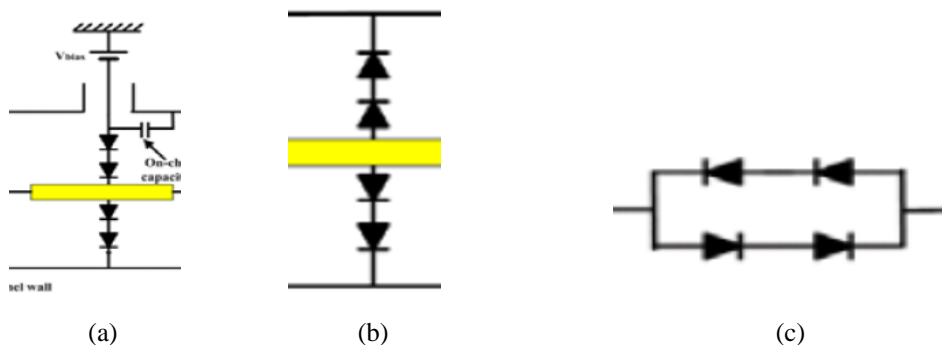


Fig. 3: block diagram of (a) common balanced tripler (b) unbalanced tripler(c) balanced tripler without bias

When input power applied to these all configuration and observe the output, then only in balanced tripler without bias (anti-parallel) configuration we get only odd harmonics. All the even harmonics are suppressed automatically inside the anti-parallel diode structure. So requirement of matching network and complexity in designing are reduced. So in our design we use this anti-parallel diode topology.

1) *Mathematical Analysis*

Diode I-V equation is given by,

$$I(V) = I_s \left[ \exp\left(\frac{qV_j}{\eta k T}\right) - 1 \right] \tag{1}$$

Where,  $\left(\frac{kT}{q}\right) = 25.8 \text{ mV}$  for  $T = 293\text{K}$

$V_j$  = junction voltage

$\eta$  = ideality factor (1.204)

$I_s$  = saturation current

Power series expansion of equation (1)

$$I(V) = I_s \left[ 1 + \frac{\left(\frac{qV_j}{\eta k T}\right)}{1!} + \frac{\left(\frac{qV_j}{\eta k T}\right)^2}{2!} + \frac{\left(\frac{qV_j}{\eta k T}\right)^3}{3!} - 1 \right] \tag{2}$$

Equation (2) can be written as,

$$I = av + bv^2 + cv^3 \tag{3}$$

When diodes are connected in anti-parallel form than, current at output side is

$I = f(V) - f(-V)$

$$I = 2av + 2cv^3 + 2ev^5 + \dots \tag{4}$$

From this equation we have seen that only odd harmonics are present at the output side.

2) *Input power*

Input power is a practical constraint that must be acknowledged for any high frequency multiplier design. In any high frequency multiplier design it is a fact that only limited amount of RF power will be available to drive the multiplier [5]. When the pump power of multiplier is small, the diode cannot be properly modulated. At the limit, the power conversion from the fundamental to the  $n^{th}$  harmonic follows a law that asymptotically tends to:

$$P_n \xrightarrow{P_1 \rightarrow 0} \alpha(f) \times P_1^n \tag{5}$$

Or when we applied log function than eq. (5) became

$$\log P_n \xrightarrow{P_1 \rightarrow 0} \alpha(f) + n \times \log(P_1) \tag{6}$$

Where,

$P_n$  = the power produced at  $n^{th}$  harmonic

$P_1$  = pump power

$\alpha(f)$  = coefficient that depends on the diode and frequency

Equation (6) shows that for a tripler ( $n=3$ ), dividing the pump power by two can divide the output power delivered by the diode by eight. This relationship is confirmed by simulation. In below figure different input power Vs conversion loss is given.

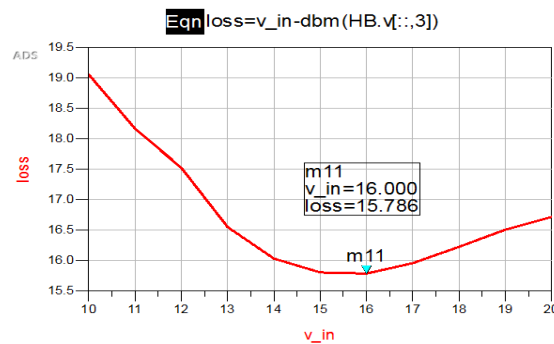


Fig. 4: (input power Vs conversion loss)

From this figure we seen that loss is minimum and constant for 15 to 16 dBm power

**Input Matching Network:** the input matching circuit had to match from the diode impedance at the first harmonic to the applied input impedance, together with providing a short at the third harmonic. This was done using a  $\lambda/4$  length Microstrip line at 120 GHz which pass only the 40 GHz frequency means 1<sup>st</sup> harmonic of input signal and act as a short circuit for 120 GHz. In cascade with this MIM capacitor 6.34 pF is connected, response of this capacitor is like a LPF at 40 GHz. This whole input matching network loss is 1.314

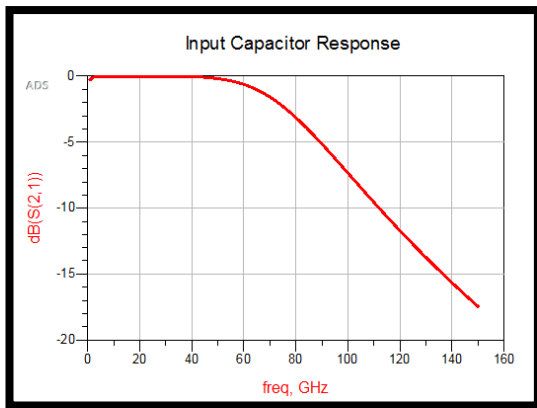


Fig. 5: (response of input capacitor)

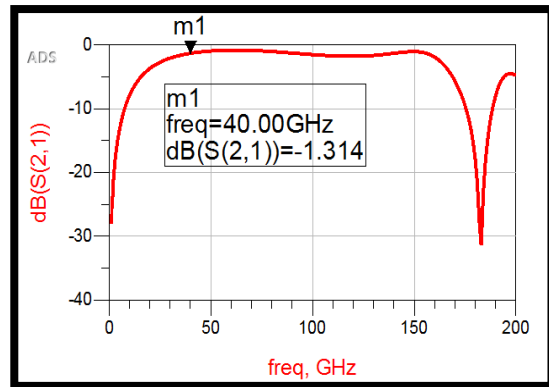


Fig. 6: [S(2,1)] of input matching network

### 3) Output Matching Network

At the output side all odd harmonics are generated but our desired one is 3<sup>rd</sup> harmonic which is at 120 GHz. So for that we required a matching circuit which had to match from the 3<sup>rd</sup> harmonic of the diode circuit output. For this we are using the bandpass filter at centre frequency 120 GHz. Here we design a bandpass filter using the co-planar waveguide type Microstrip line because it gives good response at this high frequency and loss of this particular section is

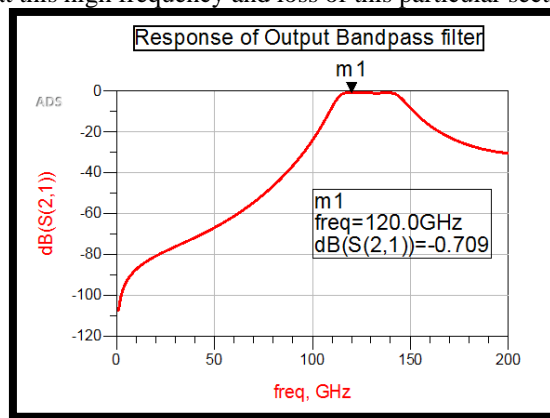


Fig. 7: (response of output matching network)

## IV. SIMULATIONS

Here we perform two type of simulation first one is schematic design simulation and second one is EM (Electro Magnetic) simulation. For schematic design simulation harmonic balance (HB) simulation tool is used.

To complete the simulations a value for input power needs to be determined. An input power of 15 dBm at 40 GHz is applied. There are three section in multiplier design input matching network, diode structure and output matching network. Till now we designed and simulate all this section separately. Now connect all this section in cascade form and applied the input power. In schematic design we use harmonic balance (HB) simulator and observe the output power.

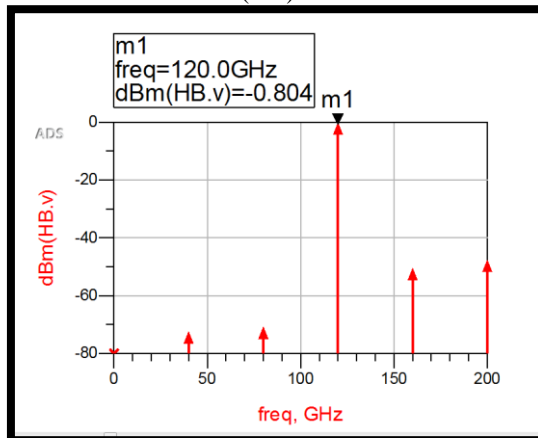


Fig. 8: (output response of multiplier schematic design)

After designing schematic we go with the actual layout design. EM simulation is used for layout design. For EM simulation there are two techniques MoM (Methods of Momentum) and FEM (Finite Element Method). MoM is a surface meshing approach so it is preferable for planer geometry which uses green function and coupling integral to find the solution. FEM is a volume meshing approach which is more appropriate for most 3-D arbitrary geometries. In this design we are

designing MMIC of Frequency Multiplier at 120 GHz. So for this we use FEM for EM simulation because at this high frequency FEM is more accurate than MoM.

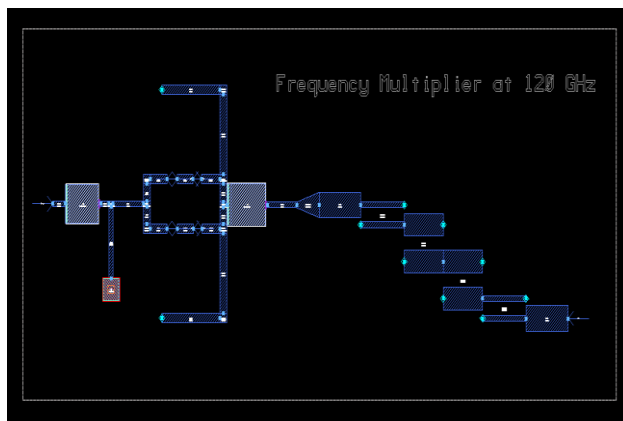


Fig. 9: (Layout Design)

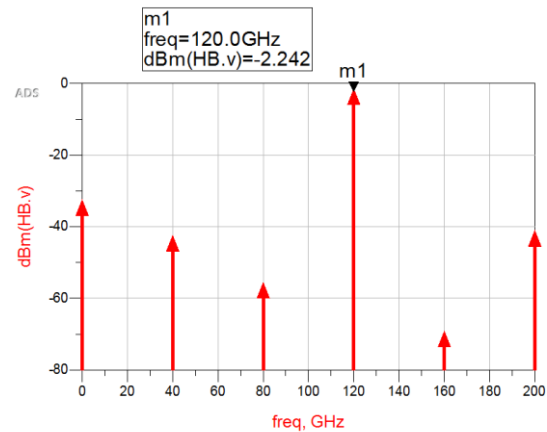


Fig. 9: (output response after FEM simulation)

## V. CONCLUSION

GaAs Schottky diode technology has advanced substantially in the last few years to enable power generation via frequency multiplication well into terahertz frequency range. Methodology for designing 120 GHz planar tripler has been presented in this paper. Simulation result indicate that if the tripler can be pumped with 15-16 dBm of input power it will be possible to get sufficient output power to pump mixer.

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