Implementation of Fir Filter Using XOR Based Vedic Multiplier

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Abstract— In this present world immense investigation goes inside the field of communication and signal handling applications. The FIR filter is generally utilized in filtering applications to improve the nature of the signals. In any processor, the presentation of the framework depends on the speed of the multiplier unit engaged with its activity. Since multiplier shapes the irreplaceable building block of the FIR filter framework. Its exhibition has contributed in deciding the execution of the FIR filter framework. Likewise, because of the colossal improvement in the innovation, numerous methodologies like array, Vedic techniques are made to speed up the multiplier calculations. The issue in speed up activity and resource usage of equipment with every one of the regular techniques because of the basic way discovered in partial products must be advanced utilizing proposed strategy. In this paper 16-bit carry select adder has been introduced utilizing modified XOR based full adder to lessen circuit area, power and delay. The modified full adder configuration required just two XOR gates and one multiplexer. The modified 16-bit carry select adder gives preferred outcome over traditional carry select adder concerning area, power utilization and delay. Utilizing this altered technique 16 bit CSA a Vedic multiplier is developed. An XOR based Vedic multiplier is utilized for FIR filter execution. The softwares utilized are XILINIX ISE simulator, MICROWIND and DSCH2. Coded using VHDL module.

Keywords: FIR, low power, area efficient, XOR based adder, carry select adder, Vedic multiplier, VHDL, MICROWIND, DSCH2

I. INTRODUCTION

The core of computer arithmetic is addition. Because of their simplicity of implementation, finite impulse response (FIR) digital filters are widely used in digital signal processing. The amount of computation required to process a signal through a FIR filter is the main disadvantage of FIR filters. In a FIR filter structure, multipliers are the most expensive operators in terms of area, delay, and power. However, some applications, such as software defined radio front ends, necessitate high speed parallel filters with constant coefficients. If a specialised Vedic multiplier is used, these applications can benefit from significant hardware reduction. Adders are unavoidable in processors and many other types of digital circuits. The time required to propagate a carry through the adder limits the speed of addition in digital adders.

In the rapidly expanding mobile industry, faster units, smaller footprints, and lower power consumption are major concerns. Area and power are critical factors in increasing the portability of mobile electronics. They are also concerned about increasing battery life. The main focus of research in VLSI systems is on area and power reduction. Faster addition and multiplication speeds are a fundamental requirement of high-performance processors. One of the most important research areas in VLSI system design is the design of area and high-speed data path logic systems. Addition widely the overall performance of digital systems and arithmetic functions. Adders are widely used in electronic systems and applications.

Adders, multipliers, and DSPs are used to execute various algorithms such as FFT, FIR, and IIR. Adders enter the picture whenever the concept of multiplication is mentioned. Microprocessors, as we know, perform millions of instructions per second. As a result, the most important constraint to consider when designing multipliers is speed of operation. Because of device portability, device miniaturization should be high and power consumption should be low.

Mobile phones, laptop computers, and other electronic devices necessitate a larger battery backup. As a result, a VLSI designer must optimize these three parameters in their design. These constraints are extremely difficult to meet, so a compromise between constraints must be made depending on demand or application. Ripple carry adders have the smallest design but the slowest speed. Instead of using dual ripple-carryadders, a carry-select adder can be implemented with a single ripple-carry adder and an add-one circuit. To reduce area while sacrificing speed, a multiplexer-based add-one circuit is proposed. Because of its small size and low power consumption, CSA is one of the fastest adders.

In CSA, two multiplexed RCA operate in parallel, assuming carry in, Cin = 0, and carry out, Cin = 1, and the final sum is selected via multiplexer. Full adders based on XOR, AND, and OR gates are used in conventional CSA. Because of the large number of transistors used in these gates, these adders take up more space on the chip, have a longer delay, and use more power. Because of the large number of transistors used in these gates, adders take up more space on the chip, have a longer delay, and consume more power.

A full adder, which is the main building block of n-bit adders, returns the result of addition with output carry while taking input carry into account. So, a one-bit full adder adds three one-bit numbers A, B, and Cin, where A and B are the operands and Cin is a bit carried in from the previous less-significant stage. A binary full adder implementation using two XOR gates and one 2:1 MUX. The main difference between conventional and XOR-based adders is that in the XOR-based adder, in addition to two XOR gates, only one 2:1 MUX is used, which requires only 6 MOSFETs, whereas in the conventional type adder, two AND gates and one OR gate are required, which requires at least 18 MOSFETs. Developed with a modified full adder and a 32-bit modified carry selector. A Vedic multiplier and FIR filter are gradually implemented.

II. RELATED WORK

Carry select adder, as described by Rajwinder Kaur [1], is a key hardware block in most arithmetic logic units, and

arithmetic logic is an essential unit of microprocessors, DSPs, and FIR filters, among other things. In the world of technology, it has become necessary to develop a number of novel design approaches in order to reduce area and power consumption. TG was used in this paper to create the proposed 64-bit CSA using AND, XOR, and OR gates. The main goal of this paper is to design a new CSA that outperforms conventional CSA designs in terms of delay and power dissipation.

R. Uma et al. [2] proposed that adders should be a nearly mandatory component of every modern integrated circuit. The adder must be fast first and efficient in terms of power consumption and chip area secondarily. This paper discusses the appropriate choice for selecting an adder topology with a tradeoff between delay, power consumption, and area. Ripple carry adder, carry look ahead adder, carry skip adder, carry select adder, carry increment adder, carry save adder, and carry bypass adder are the adder topologies used in this work. At 0.12m 6meta, the module functionality and performance issues such as area, power dissipation, and propagation delay are examined. The module functionality and performance issues such as area, power dissipation, and propagation delay are investigated using the micro wind tool at 0.12m 6metal layer CMOS technology.

According to Akshay savji et al. [3], ancient vedic mathematics consists of 16 sutras and 13 subsutras. These sutras provide an appropriate method for arithmetic calculations. The vedic formulas take less time to calculate than regular formulas or methods. A multiplier is a crucial component in many digital systems. The Urdhva Tiryagbhyam sutra of ancient vedic mathematics is used to create a 32-bit vedic multiplier in this paper. The 32-bit vedic multiplier is realised with the help of 16-bit multipliers and adders. The 16-bit multipliers are basic blocks in the design that multiply the input bits and add the results using adders.

Adders, as described by L. Shanigarapu et al. [4], are the fundamental building blocks of any processor or data path application. Carry generation is a critical path in adder design. To reduce the power consumption of the data path, we must reduce the number of transistors in the adder. Carry Select Adder is a fast adder that is used in a variety of data path applications. In the CSLA structure, there is an opportunity to reduce the area, power, and delay. For Cin=0 or Cin=1, the proposed design employs a D-latch instead of an RCA cascade structure. When compared to the Regular Carry Select Adder, this proposed design reduces power and delay by 10.8 percent and 4.6 percent for 8 bit, 17.73 percent and 49.3 percent for 16 bit, 20 percent and 44.5 percent for 32 bit, and 21.9 percent and 59.8 percent for 64 bit (CSA). When compared to the modified CSA adders, power and delay are reduced by 4.43 percent and 37.23 percent for 8 bit, 12.37 percent and 37.8 percent for 16 bit, 14.06 percent and 45.68 percent for 32 bit, and 14.43 percent and 50.57 percent for 64 bit (BEC). When compared to the modified CSA, the delay is reduced by 37.24 percent for 8 bit, 60.4 percent for 16bit, 61.6 percent for 32 bit, 14.43 percent for 32bit, and 56.74 percent for 64 bit.

According to D Khalandar Basha et al.[5], multipliers play an important role in digital filtering, digital communications, and spectral analysis. Currently, DSP applications are aimed at low-power, high-speed systems, and as a result, power dissipation has emerged as a major primary design constraint. This paper describes the design of Multiplier architectures in Vedic Mathematics using the Urdhva Tiryakbhyam Sutra. This sutra (algorithm) is used to create 4x4, 8x8, and 16x16 Vedic Multiplier architectures. These designs are created in three ways, each with a sub module design, for a total of six designs of each 4x4, 6x6, 8x8, and 16x16.

III. MODIFIED XOR BASED FULL ADDER

A full adder that is the primary constructing block of n-bit adders offers the end result of addition with output deliver taking enter deliver in to consideration. So, simply a one-bit full adder provides 3 one-bit numbers A, B, and Cin wherein A and B are the operands, and Cin is a carry carried in from the preceding much less-tremendous stage. The benefit of XOR primarily based totally adder is that it calls for smaller number of transistors.

Full Adders	Power(µw)	Area	Delay(Ns)
Conventional	65.660	7	1.45
XOR Based	64.73	5	0.863

Table I: Comparison table between Full adders

The major distinction among the traditional and XOR primarily based totally adders is that during XOR primarily based totally adder apart from XOR gates best one 2:1 MUX is used which wishes best 6 MOSFETs wherein as in traditional kind adder apart from XOR gates AND gates and one OR gate is wanted which calls for at the least 18 numbers of MOSFETs. So, there may be at the least 12 numbers of MOSFET financial savings in XOR primarily based totally 1-bit adders than traditional which in flip has much less region and electricity intake on the identical time there may be additionally a higher postpone performance.

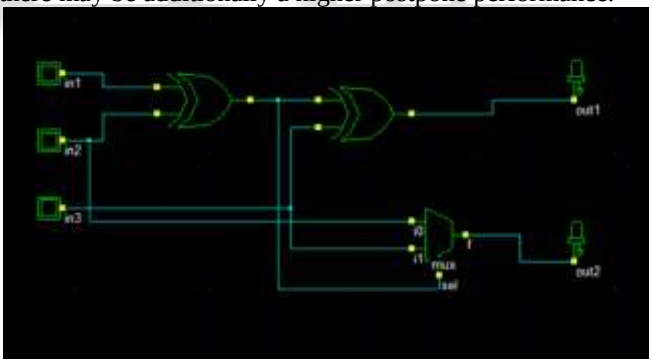


Fig. 3.1: XOR Based Full Adder Logic Diagram

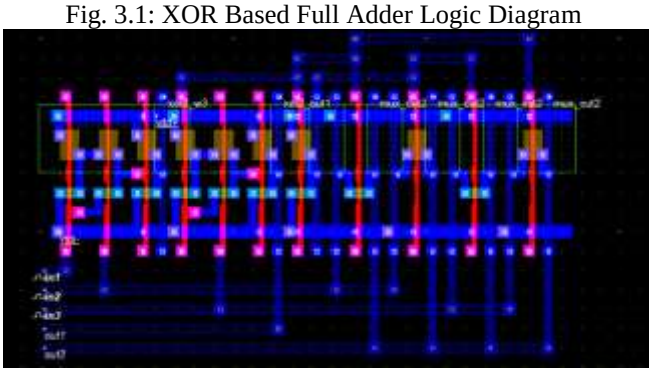


Fig. 3.2: Layout of XOR Based Full Adder

IV. CARRY SELECT ADDER

The CSA is built from two RCAs and a multiplexer. Addition of two n-bit numbers with CSA is nothing however adding two numbers taking input carry 1st as zero then victimization another adder taking input carry as one.

Once calculation of the 2 results reckoning on the proper carry-in the correct total furthermore because the correct carry-out is chosen with the multiplexer connected lastly to urge the ultimate output. A 16-bit CSA consists of 16-full adders with the carry signal that ripples from one full adder stage to the next.The simulation results of each standard and changed CSA (using XOR-based mostly adder) in terms of power, space, delay and power delay product (PDP). Each individual

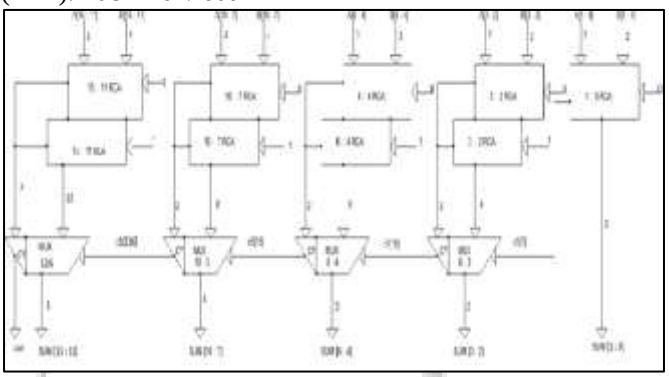


Fig. 4.1: 4 Bit Carry Select Adder

Fig. 4.2: 16 Bit Carry Select Adder Simulation Result

V. VEDIC MULTIPLIER

The goal The previous practices were reviewed from Indian Sanskrit works named as the Vedas, concerning 1911 notwithstanding 1918 by Sri Bharati Krishna Tirthaji and from (1884-1960) the Atharva Vedas. As demonstrated by his examination, most of the math is found with sixteen sutras, or word-recipe. These formulae depict the manners by which mind reasonably works and are thusly a surprising help with guiding the student to the right strategies for results. In the Vedic plan, testing inconveniences or immense entireties can consistently be addressed quickly by this technique. Numerous critical and striking procedures are only a piece of a whole plan of math which is a future new standard than the advanced strategy.

Vedic Mathematics displays the energetic and incorporated assortment of arithmetic and these techniques are reciprocal, immediate and basic. An attentiveness of Vedic arithmetic can be commendably improved in the event that it is remembered for designing learning. In future, every one of the premier institutes may set-up appropriate investigation communities to support research works in Vedic arithmetic. For his exploration, the entirety of the science is made on sixteen Sutras, or word-recipes . These formulae characterize the manner in which the astuteness totally works and are hence a limitless assistance in controlling the understudy to the reasonable strategy for arrangement.

In this Vedic plan, testing issues or immense wholes can regularly be settled promptly by the Vedic technique. These techniques are noticeable and more delightful to be a piece of a total arrangement of science which is more streamlined than existing strategies. It underwrites the unmistakable and bound together piece of calculations and this endeavor is combined, traditionalist and simple . The comprehension of Vedic science can be fused in designing to investigate and rouse research affiliation.

VI. URDHVA TRIYAKBHYAM

This strategy is a procedure in Vedic arithmetic to speed up and region boundaries of a multiplier used. Henceforth this calculation is utilized to deliver an incomplete item with its summation surveyed simultaneously to create a net outcome. This interaction is the best resource of this technique. The significant benefit of this multiplier with different multipliers is its consistency of calculation. This adaptable nature prompts the format plan with a straightforward and reasonable methodology utilized to a few types of duplications. In a Sanskrit the term Urdhva suggests vertical up-down, Tiryakbhyam infers left to right or the reverse way around. This strategy is an overall procedure and can be material to any occasions of duplication steps. This sutra is effective and related with the numbers which are nearer to the record like 10, 100, 1000. This relies upon a substitute and the basic idea for age of a wide scope of incomplete outcomes made at the same time.

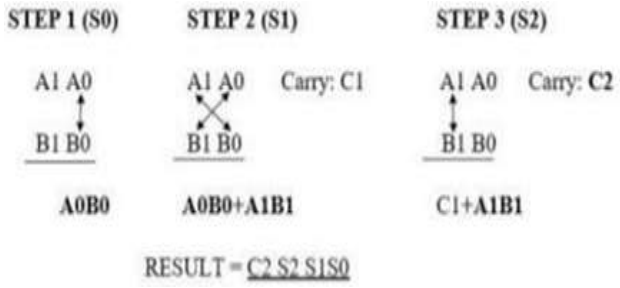


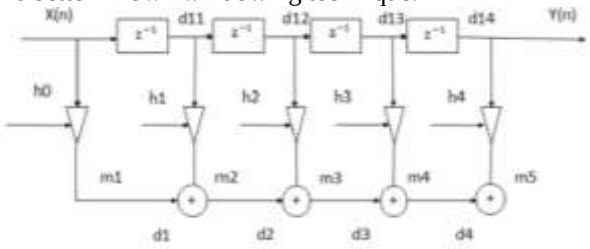
Fig 6.1: Algorithm of Vertical and Cross-Wise Multiplication

The main hindrance of the ordinary Vedic multiplier is its broad utilization of LUTs and cut registers; notwithstanding, these issues are tended to. The most inconvenience of show Vedic multiplier is its major utilization. Modified XOR based Vedic multiplier is the trade for the issue.

VII. FIR FILTER

In digital circuits, a FIR (Finite Impulse Response) filter will be viewed as a purposeful block, as shown. wherever N is that the variety of coefficients (or taps) of the filter, X is the input signal, Y the output signal, Y[n] the current output sample and H represents the filter coefficients. The coefficients of the FIR filter are obtained exploitation the separate Fourier

remodel (DFT) of the desired frequency transfer perform with some better-known windowing technique.



$$Y(n)=\sum_{i=0}^{N-1} H[i]X[n-i]$$

Fig. 7.1: FIR filter algorithm

FIR, filters are one among the first kinds of filters employed in Digital Signal Processing. FIR filters are mentioned to be finite as a result of they are doing not have associate in nursing feedback. Therefore, if we have a tendency to send an impulse through the system (a single spike) then the output can invariably become zero as shortly because the impulse runs through the filter.

The output of a non-recursive filter could be an operate solely of the signal. The response of such a filter to associate impulse consists of a finite sequence of M+1 samples, wherever M is that the filter order. Hence, the filter is understood as a Finite-Duration Impulse Response (FIR) filter. different names for a non-recursive filter embrace all-zero filter, feed-forward filter or moving average (MA) filter a term sometimes utilized in applied math signal process literature.

VIII. PROPOSED DESIGN

In this methodology, we plan a FIR filter by executing a proposed XOR based Vedic multiplier calculation. The ordinary FIR filter utilizes delay elements, which adds delay to the signal by certain worth by duplicating the upsides of the past strides with the comparing coefficient. A similar filter can be decreased by utilizing XOR based Vedic multiplier for figuring item between contributions with the coefficient by supplanting typical increase. The principle benefit of this proposed strategy is the utilization of less assets used to achieve a similar errand by diminishing area, power and delay viably.

IX. RESULTS AND DISCUSSIONS

The VHDL code is composed utilizing Urdhva Tiryagbhyam Sutra and it has been executed and tried on Xilinx ISE 14.7i. The code has been combined and reproduced effectively. The Vedic Multiplier is executed utilizing Carry Select Adder.FIR filter is also implemented using XOR based vedic multiplier. Slice utilization here is 1% .The below diagram shows the rtl diagram, tech view and simulation result of FIR filter using 16 bit XOR based vedic multiplier are shown.The comparison table is also depicted.

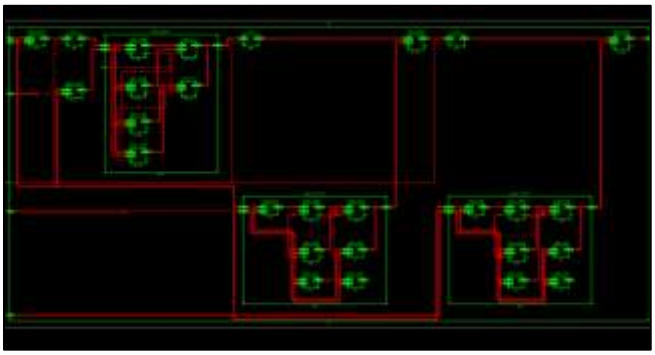


Fig. 9.1: RTL DIAGRAM of FIR Filter

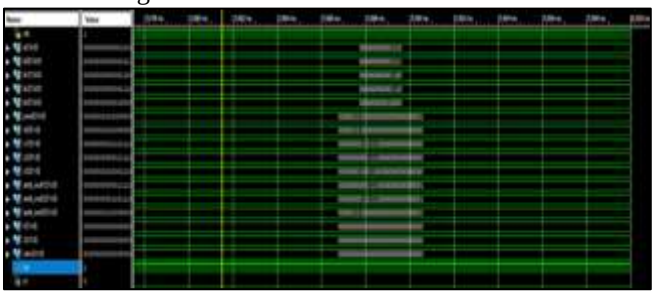


Fig. 9.2: Simulation Result of FIR Filter

X. CONCLUSION

In this paper, we have presented an extraordinary way to improve the presentation of the FIR Filter impressively by utilizing an XOR based Vedic Multiplier. This proposed multiplier gives improved execution boundaries less number of gates. Additionally, from the outcomes accomplished the postponement of this multiplier is moderately decreased contrasted with the other normal plans of multipliers. It's in this manner, concluded that the XOR based Vedic Multiplier based FIR filter configuration would be a decent decision for rapid DSP applications later on. Further examination can be performed with different calculations of Vedic science and to acquire proficient plan to be used in cryptography network for giving secure information move.

METHOD	DELAY	POWER CONSUMPTION
CONVENTIONAL FIR	13.363ns	1.063W
Design FIR filter using Urdhva Tiryakbhyam sutra	11.913ns	0.227W
Design FIR filter using Nikhilam sutra	10.889ns	0.171W
Design XOR based FIR filter using Urdhva Tiryakbhyam sutra	2.850ns	0.082W

Table II: Comparison table between different FIR filters

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