VEDIO PROCESSING ON Field Programmable Gate Array[FPGA].

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Abstract— Video/Image processing is a fundamental issue in computer science. It is widely used for a broad range of applications, such as weather prediction, computerized tomography (CT), artificial intelligence (AI), and etc. Video-based advanced driver assistance system (ADAS) attracts great attention in recent years, which aims at helping drivers to become more concentrated when driving and giving proper warnings if any danger is insight. Typical ADAS includes lane departure warning, traffic sign detection, pedestrian detection, and etc. Both basic and advanced video/image processing technologies are deployed in video-based driver assistance system. The key requirements of driver assistance system are rapid processing time and low power consumption. The Field Programmable Gate Array (FPGA)[3]is considered as the most appropriate embedded platform for ADAS. Owing to the parallel architecture, an FPGA is able to perform high-speed video processing such that it could issue warnings timely and provide drivers longer time to response. Besides, the cost and power consumption of modern FPGAs, particular small size FPGAs, are considerably efficient. Compared to the CPU implementation, the FPGA video/image processing achieves about tens of times speedup for video-based driver assistance system and other applications[4].

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I. INTRODUCTION

An FPGA is an integrated circuit Mostly digital electronics[11]

An FPGA is programmable in the field (=outside the factory), hence the name "field programmable"

- Design is specified by schematics or with a hardware description language
- Tools compute a programming file for the FPGA (gateware or firmware)
- The FPGA is configured with the design and electronic circuit is ready to use

A brief history[12]

- Logic circuits have been implemented in discrete elements (gates)
- Around 1960 a new idea was born: – Set up the gates and build controllable interconnections in between
- 1985 first FPGA-chip (XILINX)
- alternative: ASIC (Application Specific Integrated Circuit)

A. USES

With an FPGA one can build electronic circuits … … without using a bread board or soldering iron … without plugging together NIM modules … without having a chip produced at a Video/image processing is any form of signal processing for which the input is an video/image, such as a video stream or photograph. Video/image needs to be processed for better display, storage and other special purposes. For example, medical scientists enhance x-ray images and suppress accompanying noises for doctors to make precise diagnosis. Video/image processing also builds solid groundwork for computer vision, video/image compression, machine learning and etc. [7]This thesis focus on real-time video/image processing for advanced driver assistance system (ADAS). Each year millions of traffic accidents occurred around the world cause loss of lives and property. Improving road safety through advanced computing and sensor technologies has drawn lots of interests from researchers and corporations. Video-based driver-assistance system is becoming an indispensable part of smart vehicles. It monitors and interprets the surrounding traffic situation, which greatly improves driving safety. ADAS includes, but is not limited to, lane departure warning, traffic sign detection, pedestrian detection, etc. Unlike general video/image processing on computer, driver assistance system naturally requires rapid video/image processing as well as low power consumption. Alternative solution should be considered for ADAS rather than general purpose CPU[6]

II. EXISTING AND PROPOSED SYSTEM

With the industry pushing for higher-level of video quality, and the development of improved compression schemes, system processing rates have increased dramatically. At the same time, a new programmable logic devices, such as the Xilinx Spartan™-IIE FPGAs was introduced, which draw on the architectural heritage of the FPGA devices that are commonly used in professional broadcast equipment today.

As FPGA process development follows Moore's Law [10], the new products can perform the same functionality as their predecessors, with even higher performance and a much lower cost.

By developing systems using latest cost-effective FPGAs, one can bring unprecedented levels of professional, broadcast quality, video processing into areas of digital video technology such as high-end consumer products, security systems, industrial and machine vision applications, and frame-grabbers.

One driver of this trend, is the combination of networking, broadcast, processing and display technology, in what the industry has termed "digital convergence."

The need to send high bandwidth video data over extremely difficult transmission channels, such as wireless, while still maintaining an acceptable quality-of-service (QoS), is extremely difficult. This has lead to wide ranging research in how to improve error correction, compression and image processing technology, much of it based on advanced FPGA technology.

III. IMAGE COMPRESSION/DECOMPRESSION –DCT/IDCT

The main video compression scheme used in digital video systems today isMPEG2. It can be found at the heart of digital television, set-top boxes, digital satellite systems, high-definition television (HDTV) decoders, DVD players, video conferencing equipment, and Web phones, to name just a few [8]. Raw digital video information invariably has to be compressed so it can be either sent over suitable transmission channel, or stored onto a suitable medium such as a disc.

There are also a number of emerging standards, including most notably MPEG4.Most products based around this technology are still in development, although rampupto production is expected shortly. At the heart of the MPEG2 and MPEG4 algorithms is a function called the Discrete Cosine Transform (DCT)? The aim of the DCT is to take a square of pixel blocks and remove redundant information that is imperceptible to the viewer. To decompress the data, the inverse discrete cosine transform (IDCT) function is required.

While the DCT section of the MPEG algorithms is standardized and can be implemented very efficiently within FPGAs, MPEG encoding has a lot of blocks that are left undefined. It is within these undefined sections of the standard that a company can truly differentiate its product from its competition and develop its own proprietary algorithms. Many professional MPEG encoders use FPGAs in these sections, such as the motion estimation block, as shown in Figure 2[1]. Because FPGAs are reconfigurable, the equipment

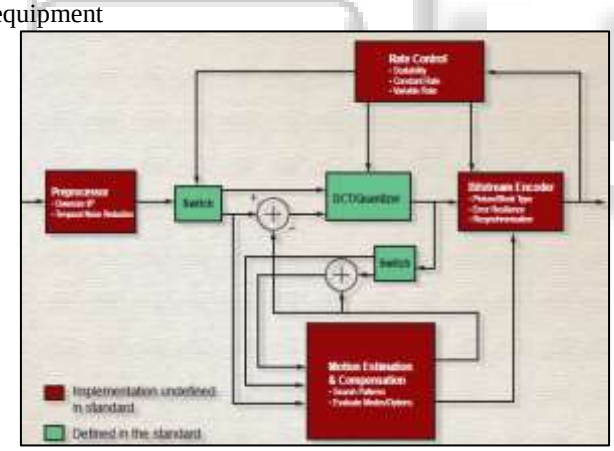

Fig. 1: Simplified Video encoder

Can be easily updated to incorporate new algorithms at all stages of development, including in the field after deployment.

Companies that rely totally on standardish solutions are limited in their ability to produce products that can make them stand out from the competition, and they therefore run the risk of being seen as just one of a number of similarly specified solutions in the market.

IV. COLOR SPACE CONVERSION

Another important part of a video system is the requirement for color space conversion, a process that defines how an image specified in one color format can be converted into a different color format.

Receptors in the human eye are only capable of detecting light wavelengths from 400 nmto 700 nm. These receptors are called cones and there are three different types, one for red light, one for green, and one for blue. If a single wavelength of light is observed, the relative responses of these three sensors allow us to discern what we call the color of the light. This phenomenon is extremely useful because it means we can generate arrange of colors by simply adding together various proportions of light from just three different wavelengths. The process is known as additive color matching, and is used in color television systems.

It's possible to represent colors of light by plotting the red, green and blue (RGB) components proportions on a 3-dimensionalcube, with black at the origin and white at the diagonally opposite corner.

The resulting cube is known as the "RGB color space," as shown in Figure 2.

Whether the final display medium is paper, LED, CRT, or plasma displays, the image is always broken down into an array of picture elements or pixels (HDTV, for example, can have 1920 x 1080 pixels). While the mechanics change slightly for each medium, the basic concept is that each pixel displays a proportion of red, green, or blue depending on the voltage signals driven to the display.

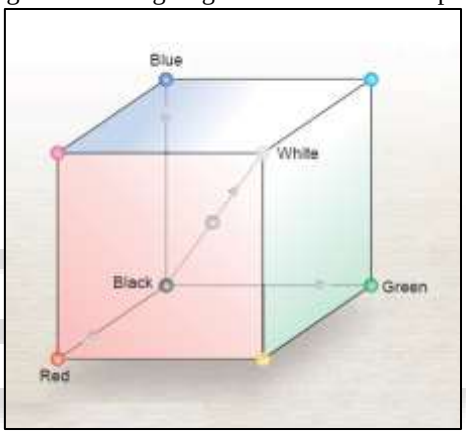

Fig. 2: Color space cube

Processing an image in RGB format, where each pixel is defined by three 8-bit or 10-bit words corresponding to each primary color, is certainly not the most efficient method. With such a format, every action on a pixel has to be performed on all thered, green, and blue channels. This invariably requires more storage and data bandwidth than other alternative color formats.

To address such issues many broadcast standards, such as the European PAL and North American NTSC television systems, use luminance and color difference video signals. A requirement therefore exists for a mechanism to convert between the different formats, and this is called "color space conversion."

Realizing these circuits in hardware is a relatively simple task, once the coefficients to map from one plane to another are known. One common format conversion is RGB to YCbCr (and conversely YCbCr to RGB).

See Figure 3. It has been found that between 60% and 70% of the luminance information (Y) a human eye can detect comes from the green color. The red and blue channels in effect duplicate much of the luminance information, and hence, this duplicate information can be safely removed. The end result is that the image can be represented as signals representing chrominance and luminance. In this format, the luminance is defined as having arrange of 16 to 235 in an 8-

bit system, and the Cb and Cr signals have a range of 16 to240, with 128 being equal to 0.

A color in the YCrCb space is converted to the RGB color space using the equations:

$$R' = 1.164\,(Y - 16) + 1.596\,(Cr - 128)$$

$$G' = 1.164\,(Y - 16) - 0.813\,(Cr - 128) - 0.392\,(Cb - 128)$$

$$B' = 1.164\,(Y - 16) + 1.596\,(Cr - 128)$$

R'G'B' are gamma corrected RGB values. A CRT display has a non-linear relationship between signal amplitude and output intensity. By gamma correcting signals before the display, the relationship between received signal amplitude and output intensity can be made linear. The output gain is also limited below certain thresholds to reduce transmission-induced noise in the darker parts of an image.

There are a number of possible implementations– memory, logic, or embedded multipliers – to perform the necessary multiplication functions. It is certainly possible to meet and exceed the 74.25 MHz data rate required for HDTV systems. It is also possible to try different design trade-offs, such as that between system accuracy and design area. For example, for a 3% error in luminance, the design size of an YCrCb-to-RGB color-space-converter can be more than halved. This may be unacceptable inmost display products but could be acceptable in other applications such as machine vision or security systems. By using an FPGA, you can tailor the algorithm for the application, thereby maximizing performance, efficiency, or both.

V. Real-Time Image and Video Processing Functions

Limitations in the performance obtainable with standard DSPs has led to the development of specially designed chips, such as media processors. However, these devices have often proved to be too inflexible in all but a narrow range of applications, and can suffer from performance bottlenecks. The limitations of a processor-based approach become especially apparent in high-resolution systems, such as HDTV and medical imaging. Fundamentally, a processor solutions restricted in how many cycles can be allocated to each tap of a filter, or each stage of a transform. Once the performance limits have been reached there is often no other way around the problem than to add extras parts.

An FPGA, [2] however, can be custom tailored to provide the maximum efficiency of utilization and performance. It's possible for you to trade off area against speed, and invariably perform a given function at a much lower clock rate than a DSP would require. For example, Vestcom Inc. found that fora median filter application a DSP processor would require 67 cycles to perform the algorithm. An FPGA needed to run at only 25 MHz, because it could realize the function in parallel. For the DSP to match the same performance, it would have to run at over 1.5 GHz. In this particular application, the FPGA solution is some 17 times more powerful than a100 MHz DSP processor.

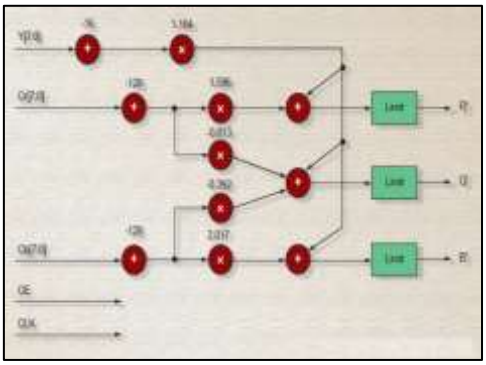

Fig. 3: YCrCb-to-RGB color space converter

VI. Conclusions and Future Work

With digital convergence, various standards and requirements into one homogeneous product need Tobe integrated –this demands flexibility in design and implementation.

FPGA technology is addressing the system requirements of new and emerging video applications, bringing with it the features and signal processing performance that have made it the preferred solution for video and image processing in the professional broadcast equipment market for a number of years. The latest generation of FPGAs can provide the same level of performance and functionality, at a fraction of the cost of the FPGAs that were designed into professional equipment just a few years before in comparison to ASSP and chipset solutions,

[14]FPGAs offer levels of flexibility that designers demand in today's products, while at the same time maintaining distinct performance advantage over conventional DSPs.

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