Building an AMBA AHB Compliant Memory Controller using VHDL

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Abstract— In this paper, the design and implementation of an AMBA based Memory controller is proposed. The AMBA based Memory controller gives an ease of integration for sub-frame extraction of various data structures in SOC. AMBA based interaction deals with role specific operation. It is majorly categorized in two dedicated feature i.e. decision (AHB MASTER) and response (AHB SLAVE). The Advanced Microcontroller Bus Architecture (AMBA) specification defines an on chip communications standard for designing high-performance embedded microcontrollers. This paper focuses on how to build an AMBA Advanced High performance Bus (AHB) based memory controller that can work efficiently in multi- master and multi- slave communication model.

Keywords: Advanced Microcontroller Bus Architecture (AMBA), Advanced High Performance Bus (AHB), system on a chip (Soc)

I. INTRODUCTION

The increase in computational capacity measured in recent years in all device electronic is bound to double flush with the miniaturization of components, and then with the integration of multiple structures on the same chip. Incorporating, for example, on the same die (the chip of semiconductor material that all enclosed inside of the package is the real CPU chip) the communication devices with the external (coprocessors, Ethernet controller, controller USB, memory controller etc.) allows at the same time to reduce in size and consumption but also to increase the overall performance of the overall system increasing the speed with which data can be transferred between the different structures integrated.

II. LITERATURE SURVEY

A. Shilpa Rao and Arati S. Phadke, "Implementation of AMBA compliant Memory Controller on a FPGA", IJETEE, 2013.

As microprocessor performance has relentlessly improved in recent years, it has become increasingly important to provide a high-bandwidth, low-latency memory subsystem to achieve the full performance potential of these processors. In the past years, improvements in memory latency and bandwidth have not kept pace with reductions in instruction execution time.

Caches have been used extensively to patch over this mismatch, but some applications do not use caches effectively. The result is that the memory access time has been a bottleneck which limits the system performance. A Memory Controller is designed to avoid this problem. The Memory Controller is a digital circuit which manages the flow of data going to and from the main memory. It can be a separate chip or can be integrated into the system chipset. This paper revolves around building an Advanced Microcontroller Bus Architecture (AMBA) compliant Memory Controller as an Advanced High-performance Bus (AHB) slave. The whole design is captured using VHDL, simulated with ModelSim and configured to a FPGA target device belonging to the Virtex4 family using Xilinx.

B. Jayapraveen. D and T. Geetha Priya, "Design of memory controller based on AMBA AHB protocol", Elixir International Journal, 2012.

The performance of a computer system is heavily dependent on the characteristics of its interconnect architecture. A poorly designed system bus can throttle the transfer of instructions and data between memory and processor, or between peripheral devices and memory. This communication bottleneck is the focus of attention among many microprocessor and system manufacturers have adopted a number of bus standards. Hence memory access time has been a bottleneck which limits system performance. Memory controller (MC) is designed to tackle this problem. The Advanced Microcontroller Bus Architecture (AMBA) specification defines an on chip communications standard for designing high-performance embedded microcontrollers. This paper focuses on how to build an AMBA Advanced High performance Bus (AHB) based memory controller that can work efficiently in multi- master and multi- slave communication model.

C. Hu Yueli; Yang Ben, "Building an AMBA AHB Compliant Memory Controller", IEEE, 2011.

Microprocessor performance has improved rapidly these years. In contrast, memory latencies and bandwidths have improved little. The result is that the memory access time has been a bottleneck which limits the system performance. Memory controller (MC) is designed and built to attacking this problem. The memory controller is the part of the system that, well, controls the memory. The memory controller is normally integrated into the system chipset. This paper shows how to build an Advanced Micro controller Bus Architecture (AMBA) compliant MC as an Advanced High-performance Bus (AHB) slave. The MC is designed for system memory control with the main memory consisting of SRAM and ROM. Additionally, the problems met in the design process are discussed and the solutions are given in the paper.

III. PROPOSED METHODOLOGY

Details of proposed methodology and work flow have been categorized in four different phases

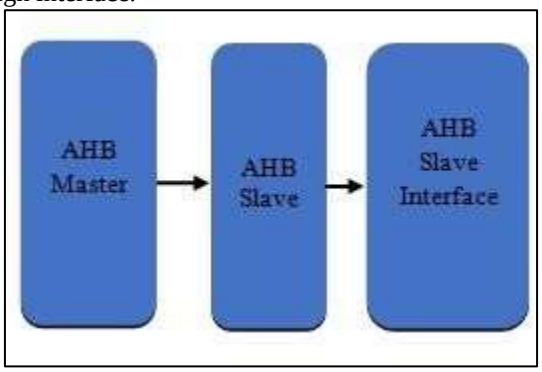
1) Development of AHB system compatible with AMBA2.0 protocol.
2) To develop memory controller and RAM, ROM, FIFO.
3) Development of the AHB system (Multiple Master) with memory controller compatible with AMBA 2.0 protocol.

4) In proposed research AHB system with memory controller application compatible with AXI 4.0 protocol.

IV. BLOCK DIAGRAM

A. Phase-1

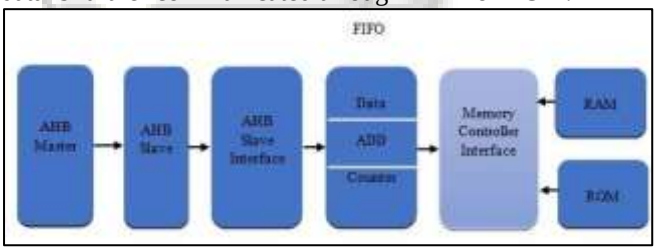
The data transfer is started by AHB master and is acknowledged by AHB slave. The communication is held through the slave-to-application interface. At first the master initiates the data and control signal but these control signals further cannot directly interact with memory. Therefore, data processing is carried out by slave and further forwarded through interface.



B. Phase 2

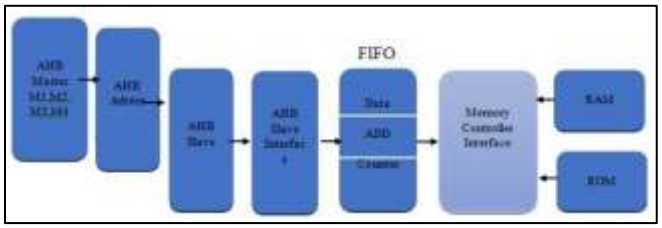
To develop memory controller and RAM, ROM, FIFO will be proposed in phase-2.AHB compliant's master's top architecture is depicted in Figure 5.3. In the proposed method FIFO is used for data and control buffering. This is done with the goals of assigning different clock cycles (CLK) to slave and memory which in turn gives a reliable communication and also decrease the complexity.

Depending upon the READ and WRITE operations data is further communicated through RAM or ROM.



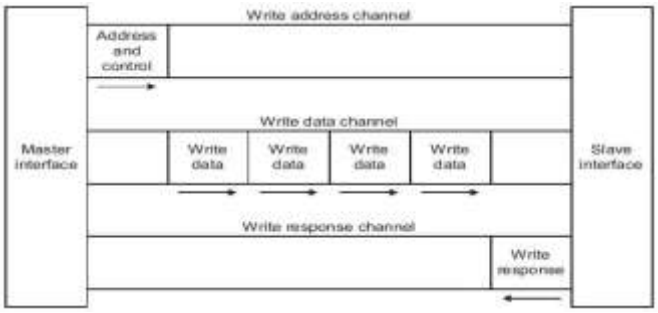
C. Phase 3

Development of the AHB system (Multiple Master) with memory controller compatible with AMBA 2.0 protocol is proposed in phase-3. The topmost architecture of multiple master AHB memory controller is shown in Figure 5.5. Data is initiated by master and granted by arbiter to carry the further communication through slave-to- memory interface. If multiple processors are interacting then arbitration requires. AMBA 2.0 supports the arbiter concepts at the cost of system complexity.

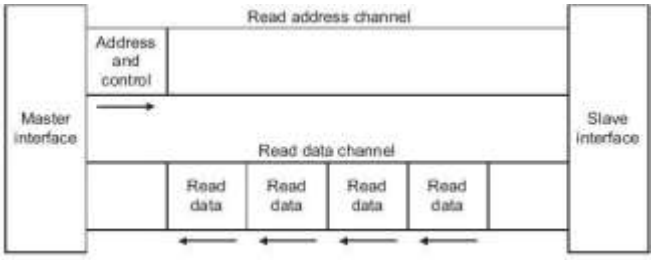


D. Phase 4

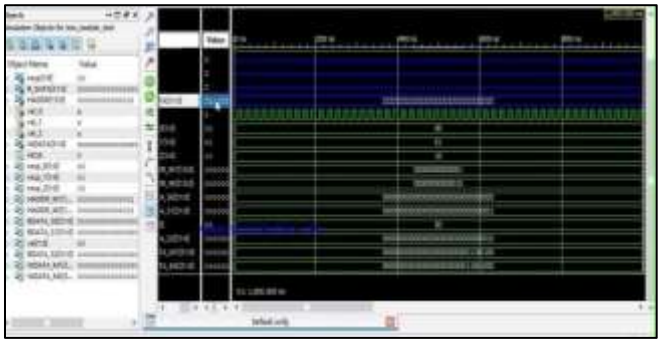
In proposed research AHB system with memory controller application compatible with AXI 4.0 protocol is proposed. In this as shown in figure 5.6 there are five different channels for communication in which three are for the writing and two for the reading purpose i.e. write address channel, write data channel, write response channel, read address channel and read data channel



Write Address Channel



E. Final Result



V. CONCLUSIONS

Carrying out literature review is very significant in any research project as it clearly establishes the need of the work and the background development. It generates related queries regarding improvements in the study already done and allows unsolved problems to emerge and thus clearly define all boundaries regarding the development of the research project. Plenty of literature has been reviewed in connection with the implementation of AMBA based Memory Controller and the significantly related ones have been discussed in this paper.

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