Design of Low Voltage High Speed Voltage Sensing Regenerative Latch Comparator for Biomedical Application

Manish Upadhyay[1] Vijendra K. Maurya[2]
[1]M.Tech. Scholar [2]Associate Professor
[1,2]Department of Mechanical Engineering
[1]RTU Kota, Rajasthan, India [2]GITS Udaipur, Rajasthan, India

Abstract— In biomedical healthcare instrumentation with the rising demand of low voltage and lower consumption circuit architectures. The biomedical signal processing has becomes the major concern, especially in biomedical field, the signal obtained are in the range of few milli-volt. As a result the processing of signal has become the major concern, which posse's stringent constraint on the performance of ADC. In order to upgrade the ADC performance, a proper selection of architecture associated with comparator is needed. Comparator, the critical building block of ADC considered as power consuming block and severely affects the overall performance of ADC converters. The accuracy of the comparator is determined the performance variables such as offset voltage, power consumption, operation speed, slew rate and noise. In this work I have designed the voltage sensing latch comparator based on regeneration using cross coupling mechanism. The design is implemented in 180nm technology operated at the supply voltage of 0.8V, the parameters obtained after simulation are as follows gain 56.20dB, Slew rate 625V/µsec, Power dissipation 6.13µW, IRN 1.01fV/√Hz and Delay of 0.24ns.

Keywords: Comparator, ADC, Power Consumption, Metastability

I. INTRODUCTION

Bioengineering is responsible for the research and development of biomedical implants and battery operated portable health care devices and determines the various procedures which can solve medical and problems related to the health with the combination of advanced knowledge in engineering, biology, and medicine in order to resort the improvement in human health with the help of cross-disciplinary activities which is capable enough to integrate science associated with the engineering to the biomedical sciences as well clinical research and practice.

With the advancement and researches in the field of microelectronics has pushed the growth in advancement of biomedical implants and portable battery operated medical health care diagnosis system, when such devices are concerned lifespan of the battery becomes the critical factor.

Such development and advancement in the medical recording/diagnosis system has demanded the development of various circuit techniques and architectures/topologies which precisely makes use of concept of low voltage and low power as result such architectures has become the basic building of portable/battery operated medical healthcare instrumentation.

A/D interfaces are considered as predominant part ICs which contains mostly digital hardware blocks for the Digital Signal Processor as well the control circuit. A/D converters are considered as important circuital element which is responsible for the conversion weak bio-potential analog signals obtained from the measurand and is converted into digitized form which is further processed by the DSP in order to retrieve successfully the information about the health status.

It is basically an interfacing circuitry between the world of bio-potential analog signals and digital world. The data extracted from the DSP is completely defined by the performance of ADC. So, in order to derive the data to be processed which carries information related to health status without any corruption in data is completely determined by the ADC.

In order to reduce the cost of ICs the multiple supply voltage for the circuits is needed to be eliminated. The higher voltage supply architectures to be avoided when it comes about portable biomedical devices such requirement have pushed the requirement of low voltage new generation ADC.

The comparators possess the crucial impact on the performance of A/D converters. Comparator is an electronic circuit which is responsible for making comparison between two analog signals or a reference signals as result produces binary bits. Any signal having continuum amplitude is analog signals. One or two values can be given by the binary signals in the strict sense. For the real world situations the concept of binary signal is too ideal, there exist a transition state between two binary states.

The comparator finds its wide application in conversion of analog signal to digital signal. In A/D is required to process the sample the signal the first. The signal sampled is then applied to the comparators combination in order to obtain the digital output which is equivalent to the analog signal. It is considered that comparator is 1 bit equivalent to A/D converter.

The converters employs large number of comparator in parallel so as to obtain the high throughput rate which is responsible to impose the tight constraints likewise delay, resolution, power dissipation, input voltage range, input impedance, and area of those circuits.

With incremental demand in the healthcare screening equipment's in order to process the analog signals, it resorts the design which can provide prominent class of performance efficient interfacing circuitry (ADCs).

II. ANALYSIS OF COMPARATOR BLOCK DIAGRAM

The high performance comparator is basically designed using the three stages which are shown in the figure 1. The comparators are basically classified as open loop comparators and regenerative comparator using positive feedback and the third type of comparator is consist of collective combination of regenerative and open loop type of comparator, which gives birth to extremely fast comparator.

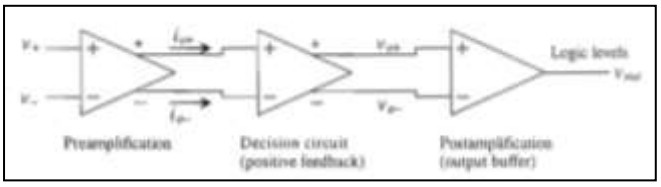

Fig. 1: Block Diagram of Comparator

The stages namely of which the block diagram is consisted are input pre-amplifier, decision stage and the output.

A. Pre-amplifier:

Itresponsible for the amplification of the input to increase the sensitivity of comparator and responsible for the isolation of input signal of the comparator from the kick back noise, positive feedback stage. The large input signal is determines at the positive feedback block. Decision circuit is responsible to propagate the signal to the output buffer and the signal is amplified and outputs the digital level is 1 or 0.Preaplifier is basically the differential amplifier having active load. The gain is basically determined by the trans-conductance stages of comparator.

B. Decision making circuit:

In this section, a part of the comparator is shown in figure 2 is presented which simply explain about the decision circuit, which is considered as heart of comparator.

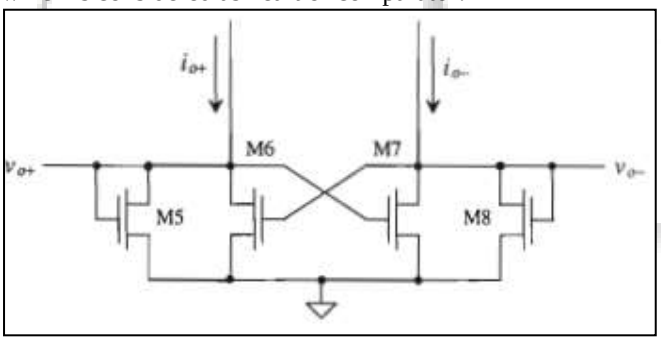

Fig. 2: Decision Circuit

The part of the circuit presented in figure 2 make use of positive feedback with the cross coupling connection of the M6 and M7 transistor in order to raise the degree of the gain of the decision circuit.

Let us consider the working of the circuit which simply elaborates the working, suppose in case I input $i_{0+} > i_{0-}$ as result M5 and the M7 is turned on and at the same time M6 and M8 transistors are turned off. It is assumed that the $\beta_5=\beta_8=\beta A$ and $\beta_7=\beta_6=\beta B$. The result can be represented by the equation 1

$$V_{0+}=\frac{\sqrt{2}i_{0+}}{\beta A} + V_{thn} \quad \text{.....(1)}$$

Let us consider the case II, if $i_{0+} < i_{0-}$ in which value of i_{0+} is raised and i_{0-} is decreased, as the switching is taken place when the drain source voltage(V_{ds}) of M7 = threshold voltage(V_{thn})of M6. M6 starts conducting at this point. The current through M6 can be given by the equation 2.

$$M7= I_{0-} = \frac{\beta B}{\beta A} \cdot I_{0+} \quad \text{.....(2)}$$

C. Buffer's Output:

The final component of the comparator is the post amplifier or output buffer. The post amplifier is employed in the circuit in order to convert the decision circuit output to the logical signal. The differential signals are accepted by the output buffer and has no slew rate limitation.

III. COMPARATOR CHARACTERIZATION

A. Static Characteristics

Basically binary output is produced by Comparator and is defined when two different analog signals are compared. When the inverting and non-inverting differences between the inputs is positive then the output obtained from the comparator is (V_{OH}) and when the differences in between the output signal is negative output is V_{OL}. But in the real world situation such type of behavior is impossible.

When the transition occurs in between the V_{OH} and V_{OL}. The state of output is changed from an input change of ΔV, where the ΔV tends to zero or approaches to zero. Such that it implies gain approaches to infinity can be given by equation 3

$$\text{Gain}=A_v= \lim_{\Delta V \to 0} \frac{V_{OH}-V_{OL}}{\Delta V} \quad \text{.....(3)}$$

There exist a difference between this model and previous one is basically about the gain which can be expressed by the equation 4.

$$A_V=\frac{V_{OH}-V_{OL}}{V_{IH}-V_{IL}} \quad \text{.....(4)}$$

Resolution, The differences in the voltage are represented by V_{IH} and V_{IL} at input in between V_p-V_n just required in orderto saturate the output at its lower and upper limit.

Gain, The operation of comparator is described by the gain for it happen if define about the minimum input change required to obtain the necessary output voltage that swingsthat occurs in between the two of binary states. The states obtained at the output are determined by the digital circuitry's input requirement which is responsible to drive the comparator's output.

Input Offset Voltage, The non-idealities that can be seen in the comparator circuits is input offset voltage V_{OS}. There is change in the observed when the input difference crosses zero. If there is no change in the output until the difference at the input has reached to V_{OS}. Offset varies from one circuit to other circuit from particular design it varies randomly. Figure 3 shows the transfer curve including the effect of offset voltage. The offset voltage of comparator shows the +/- signs observed as polarity of offset voltage V_{OS}.

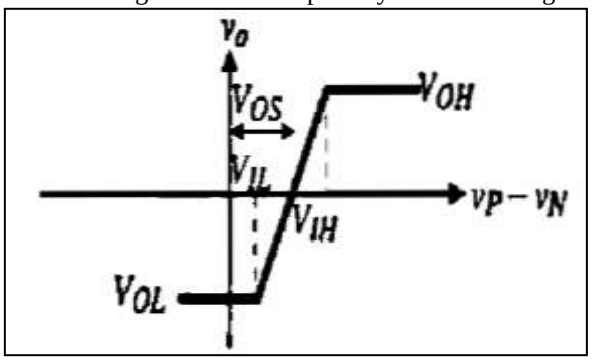

Fig. 3: Ideal Transfer curve for Comparator includes input offset voltage

ICMR, defined by the common mode range of voltages up to which normal behavior of the comparator is

obtained. In such a range all the transistors of comparator are defined to work in the saturation state. Even it may happen that the comparator is designed not to work in transition region between the respective binary states still noise is considered as critical parameter.

Noise, basically causes uncertainty in the transition as a result it produces jittering effect or noise in the phases in those circuits where comparator is used. The influence of noise in the circuit can be observed in the figure 4.

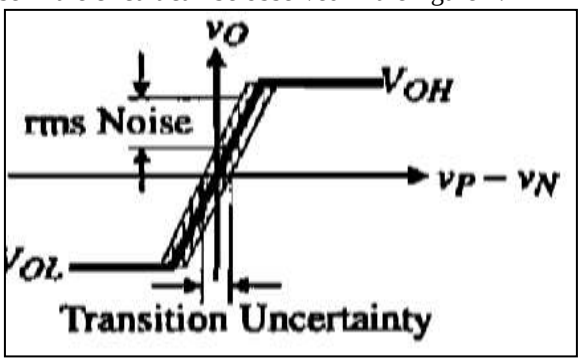

Fig. 4: The noise influence in comparator

B. *Dynamic Characteristics*

The small and large signal behavior both can be included into dynamic characteristics behavior of comparator. But although it is not known that how much time will the comparator take to respond the differential input. The time response of the comparator is defined by the delay that exists in between comparators input excitation and output transition. The response is illustrated in figure 5.Where the time is dependent on input

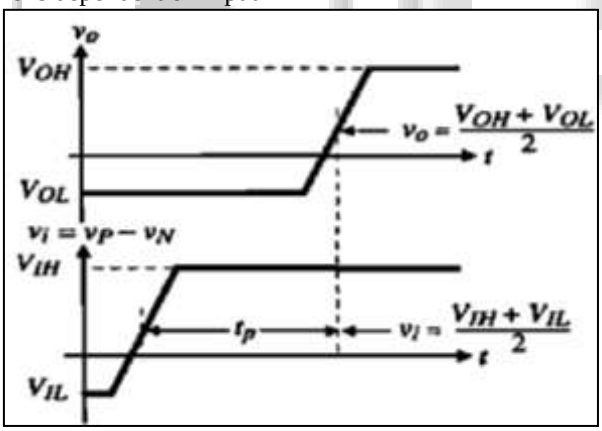

Fig. 5: Propagation delay of comparator

Delay, The delay existing between response at the output and the input excitation, this interval of difference in time is called propagation delay. It is considered as critical parameter since it is responsible to determine the speed of conversion rate of A/D converters. Comparators propagation delay time varies according to the amplitude of the signal or it can be said that it is function of amplitude. Larger the input cause's shorter time delays.

The delay equation can be given by equation 5.

$$T_p(max)=r_c\ln(2)=0.693r_c \quad \ldots\ldots(5)$$

Slew Rate, Actually there exists an upper limit such that further incremental change in input voltage is not going to affect the delay as a result such mode of operation is slew rate.

Resolution, defined by the comparator as the minimum change in the input voltage of comparator as a result the minimum input voltage to the comparator is given by the equation 6.

$$V_{in}(min)=\frac{V_{OH}-V_{OL}}{A_v(0)} \quad \ldots\ldots(6)$$

Larger the over-drive voltage applied at the comparator's input, lesser will be the propagation delay time. With the increase in the over-drive voltage eventually the comparator enter to the large signal mode operation. Due to limitedcurrent value to charge or discharge capacitors, slew rate will be limited under the large signal operation. With the help of propagation delay, slew rate can be given by the equation 7.

$$t_p=\Delta T=\frac{\Delta V}{SR}=\frac{V_{OH}-V_{OL}}{2SR} \quad \ldots\ldots(7)$$

In order to limit the value of propagation time, the comparators sourcing and sinking current capabilities can be raised to certain values.

IV. COMPARATOR PERFORMANCE PARAMETER

A. *Comparator Offset:*

There exists a mismatch between the input transistors such that the circuit exhibits different values of dc offset. The value of dc mismatch is basically decided by the input and output voltages. If the output voltage obtained at output is not zero w.r.t the input voltage $V_{in}=0$ as result circuit exhibits the mismatch and as well suffers with dc offset. The value of V_{out}tends to become equal to the offset voltage when the input voltage ($V_{in}=0$) is zero hence known as output referred offset.

B. *Kickback Noise:*

Latch comparator circuit makes use of positive feedback approach during the regeneration in order to scale the digital level. At the regeneration nodes voltage variations are coupled via parasitic capacitances to the inputs such that input voltage get disturbed, as a result this disturbance is called kickback noise which is responsible to degrade the performance of comparator.

C. *Noise in Comparators:*

There exist a random noise to which the circuit is vulnerable which is capable enough to drive the output in order to switch from one of the logic level to the other logic level even though the input of comparator input is tied at constant value. Hence when it is required to measure the input offset voltage in the presence of the circuital noise; it is required to consider the input voltage which is responsible to cause the output of comparator stage high and as well low with equal likelihood. By changing the input, the input referred noise is observed around this value with help of using output statistics assuming this for the example of Gaussian distributions.

D. *Parasitic Capacitance:*

in the analog design parasitic plays an important role. Parasitic basically affects the ac behavior of comparator. There exists a capacitance between two or four node associated with MOSFET. The figure 6 shows the MOS capacitance.

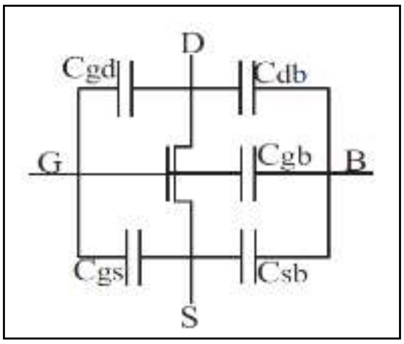

Fig. 6: MOSFET parasitic capacitance

The value of capacitance is dependent upon the gate voltage and values are changed in accordance to the region in which it is operating. The capacitances are overlapping in between source/drain and as well gate, depletion capacitance existing in between substrate and channel, oxide capacitance between substrate and channel as well the oxide capacitances existing in between the gate and channel and finally the junction capacitance existing in between source/drain.

E. Metastibility:

All the latching comparator suffers critically from the metastability which is occurred when the input is near to the decision point. When very small signals are appeared at the input of comparator which is very close to comparator decision point then occurs the metastability. Normally such kind of problem is faced by all comparators. As a result comparator fails to take decision as result of this output is latched to the stable point, which allotted period of time. The delay in the metastability is random as a result switches the output at false logical level when can cause the malfunctioning of system or even can cause the failure.

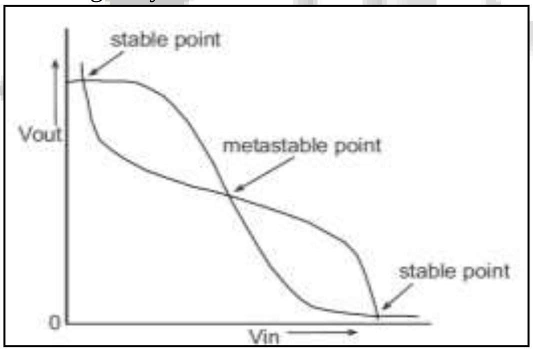

Fig. 7: Curve for inverters connected back to back

The figure 7, illustrates the voltage transfer curve for the two inverters connected back to back. The stable points of the inverter are V_{dd} or it can be ground. When the curves intercept each other at the mid points is known as metastbility. The MSP ideally attains the value $V_{dd}/2$ half the input range and the output of second inverter to driven to stable state.

F. Offset Error Voltage and DC Currents,

Operational amplifier, ideally is perfectly balanced that is $V_0=0$ and $V_A=V_B$. Due to unbalancing of the transistors there exist mismatch in between the transistor. Due to such type of mismatch the unequal biasing current flows at the input terminals and as a result also require the input offset voltage which is to be applied in between the input terminals in order to balance the amplifier output.

V. ROLE OF COMPARATOR IN ANALOG TO DIGITAL CONVERTERS UNITS

Biomedical signals are physically analog in nature, before the processing of analog signal, system require the ADC unit in order to get the digital signals, such that to take the benefits of sophisticated capabilities of digital signal processors. But how much the signals are to be processed before it is given to the ADC for the processing is basically depends on system to system optimization.

There are some characteristics on which performance of ADC depends such as bandwidth and the dynamic range as result the optimized system must take care of the ADC power, as a result it is considered a significant portion of the total power. It signifies that energy per conversion is considered important metrics of ADC and an incremental change can be observed with the increase in dynamic range and increased sampling rate. The power consumption of ADC to the nyquist sampling rate $F_s$and the dynamic range is normalized by the figure of merit (FOM) which can be expressed as 2^{ENOB} ,the figure of merit can be expressed by the equation 7. Where ENOB is regarded as effective number of bits output.

$$FOM=\frac{P}{F_S\, 2^{ENOB}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(7)$$

In accordance to the trends which are observed it considered as successive approximation register (SAR) and the oversampling ADCs is capable to attain the optimal value FOM in biomedical healthcare applications and other architecture like pipeline ADC has basically employed for the high biomedical applications.

VI. INTRODUCTION TO REGENERATIVE COMPARATORS

In order to attain the comparison in between the two signals a concept of positive feedback is used by regenerative comparators. The regenerative comparators are also known as latch or bi-stable. The simplest architecture of latch is given in the figure 8 and is comprised of two cross coupled MOSFET.

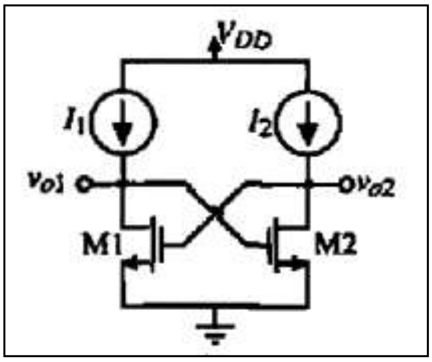

Figure 8: The design of NMOS latch

The dc currents in the transistors are identified by the current sink and sources. Normally latch is operated in two modes. In the first mode the positive feedback gets disabled and the input signal is applied to the terminals which are represented byv_{o1} and v_{o2}. During this modes the initially the voltage applied is given by 'v_{o1}' and 'v_{o2}'. In the second mode, generally the latch is enabled and depends relatively on the value of 'v_{o1}'&'v_{o2}'such that the one output will switched high and other one is switched to low. Different modes of operation are determined by the two phase clock.

It is required to such that the time is characterized as it switches the latch from initial state to final state, when the mode of operation is enabled. Let us consider the initial voltage value is the v_{o1} and v_{o2}which has been once established and now determine the time taken by latch. The model which is analyzed is shown in the figure 9.

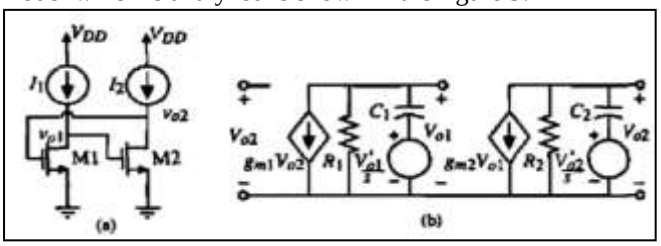

Fig. 9 (a): Restructured circuit of latch (b). Equivalent model of latch

There exit strong dependency of latch time constant on the length of channel, the time response of latch can be represented by the equation 8.

$$\tau_L=\frac{0.67WLC_{OX}}{\sqrt{2K'(W/L)I}} \quad \text{.....(8)}$$

The difference in between the output latch voltage ΔV_{out} at the time period't' after which the latch is enabled can be given by the equation 9. The difference between the output latch voltages ΔV_i can be given by V_{02} and V_{01} before the latch is enabled.

$$\Delta V_{out}(t)=e^{t/\tau}\Delta V_i \quad \text{.....(9)}$$

The most important point that is to be considered that ΔV_i do always have the value less than the propagation time delay (V_{OH}-V_{OL}) of the latch can be given by the equation 10.

$$T_p=\tau_L \ln\left(\frac{V_{OH}-V_{OL}}{2\Delta V_i}\right) \quad \text{.....(10)}$$

VII. DESIGN OF PROPOSED COMPARATOR

In this research literature I have proposed, Regenerative Latch Using Cross Coupling Mechanism is the proposed for the biomedical application, the design features the use of cross coupling along with differential input pair, in order to enhance the performance of comparator which can process the low voltage signals along with the reduced power consumption providing considerable reduction in noise. The design is operated at 0.8V implemented in 0.18um technology.

The section deals with operation of the circuit, The comparator's transistors are biased to drive them in the saturation region in order to reduce the mismatching in between the transistors. Input circuitry of the comparator is consisted of nMOS_4, nMOS_3, nMOS_6 and nMOS_5. The pair of source coupled transistor is formed by nMOS_4 and nMOS_5 to which the latch circuit is directly connected, hence the latch is formed by the combination various transistors including tail transistor also like pMOS_1, pMOS_3pPMOS_2, pMOS_4,pMOS_6,pMOS_5 ,nMOS_2, nMOS_1 and nMOS_7.In order to make the switchable current sources, the transistors are directly connected to the supply voltage(nMOS_1, nMOS_3,pMOS_2, pMOS_5,pMOS_4,pMOS_6).

When the V_LATCH signal is low i.e V_LATCH=0, the transistor responsible for the current sourcing is driven in to the off state and no current is draining path exist from the V_{DD}. In addition for the output to be reset OUT_2 and OUT_1 as well the nodes NODE_1 and NODE_2, the combination of the transistors required are pMOS_2, nMOS_1 and pMOS_5, pMOS_6. When the latch signal V_LATCH goes high i.e V_LATCH=V_{DD}, the tail transistor or current switching transistor is driven to the ON state and the outputs OUT2 and OUT1 gets disconnected from the V_{DD}.

The biasing current of transistors at the input NMOS_4, nMOS_3, nMOS_6 and nMOS_5 is basically defined by the tail transistor nMOS_7. The positive feedback producing transistors namely NMOS_4 and NMOS_5 which are connected in cross coupling mechanism is responsible to switch output at fast rate. The witching is basically determined by the input voltages VIN1 and VIN2.

When the positive input voltage VIN1>VIN2, in comparison of the MOS nMOS_6, the drain voltage of NMOS_3 rolls down the faster rate. Once the positive feedback is initiated by the cross coupled transistor nMOS_5 and nMOS_4. The node voltage NODE_1 starts to drops down very quickly and output voltage OUT2 is driven low.

Although the comparator total offset voltage is mainly the function of mismatching of the transistors, the load resistance and the dimension of the transistors Δβ. The relation for the offset voltage can be given with the help of equation 11.

$$V_{os}=\Delta V_T+\frac{V_{gs}-V_T}{2}\left(\frac{\Delta R_L}{R_L}+\frac{\Delta\beta}{\beta}\right) \quad \text{.....(11)}$$

The mismatching in between the transistor is responsible for dominating the offset voltage, the more the mismatch higher will be offset voltage which degrades the performance of comparator. There is the considerable effect of the threshold voltage V_T, offset voltage is found to be low in case if the common mode voltage is low.

The differential input pair overdrive headroom is determined by the MOS nMOS_3.NMOS_4,nMOS_5,nMOS_6 and nMOS_7 which has the proportional relation with V_{gs}-V_T .The transistor Level Implementation of Comparator Architecture using Regenerative Latch with Cross Coupling Mechanism is shown in the figure 10.

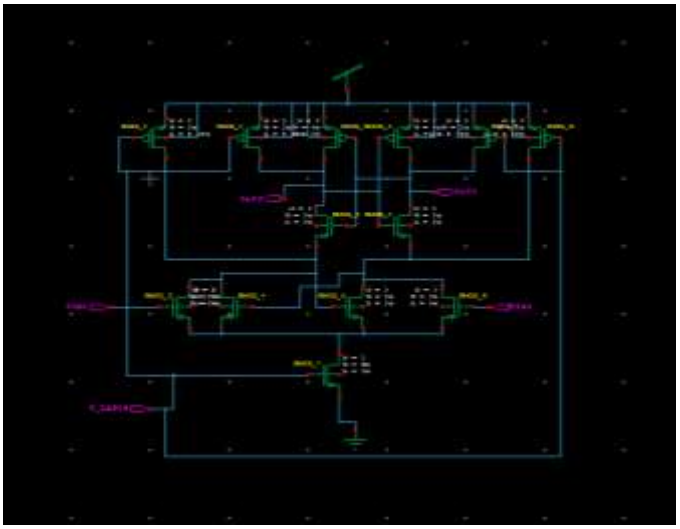

Fig. 10: Comparator Architecture using Regenerative Latch with Cross Coupling Mechanism

VIII. SIMULATION OF PROPOSED COMPARATOR

The section deals with the waveform obtained after simulation the comparator design, implemented in 180nm technology with the operating voltage of 0.8V, such that in the design the negative VIN2 input voltage has remained fixed at 700mV for the reference comparison with the biomedical signal obtained from the subject low in amplitude which lies in the range ofmilli-volts. The comparator output waveform is shown in the figure 11. The noise analysis of the comparator is exhibited in the figure 12. And the AC response of the comparator is exhibited in figure 13.

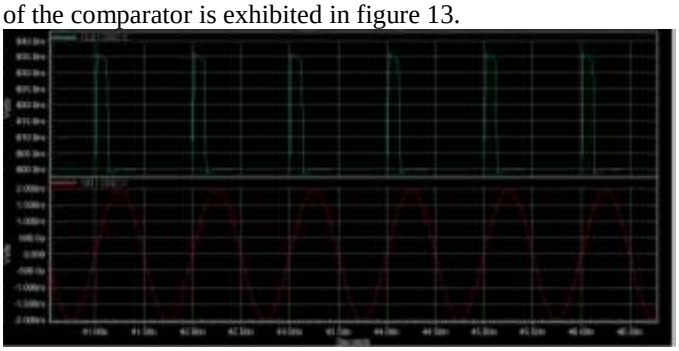

Fig. 11: Output Simulation waveform of the Comparator Architecture based on Regenerative Latch Using Cross Coupling Mechanism

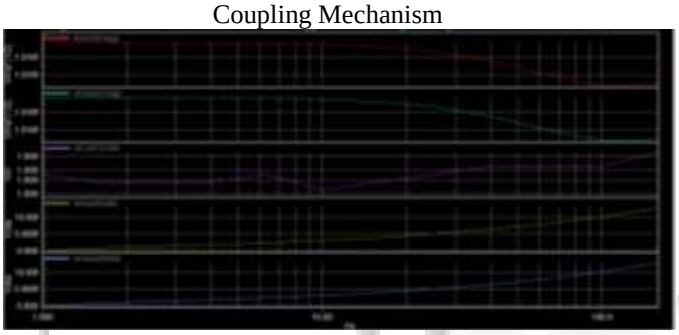

Fig. 12: Noise AnalysisWaveform of Comparator Architecture based on Regenerative

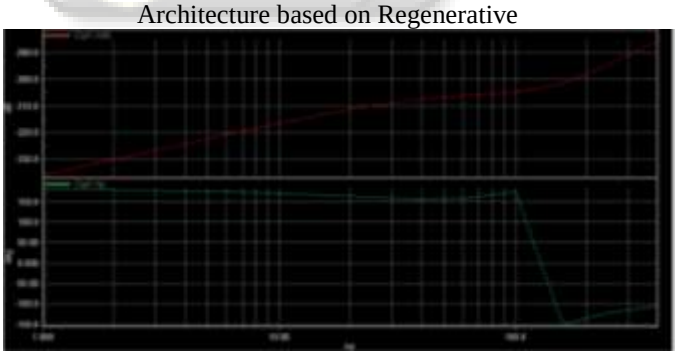

Fig. 13: AC Response waveform of Comparator Architecture based

IX. SIMULATION RESULTS

In this section, summary of performance and analysis of comparators based different topologies Regenerative Latch Using Cross Coupling Mechanism is shown in table 1.

S.No	Parameters	Units	Regenerative latch Comparator using cross coupling mechanism
1.	MOS Technology	nm	0.18
2.	Supply Voltage	V	0.8
3.	Gain	dB	56.20
4.	Phase Margin	degree	150
5.	Power Delay Product(PDP)	J	1.226f
6.	Figure of Merit(FOM)	J/conv	0.0239f
7.	IRN	V/√Hz	1.01f
8.	Power Dissipation	W	6.13x10^-6
9.	Current drawn	A	220f
10	Delay	sec	0.2n
11	Input Offset Voltage	mV_{rms}	20.40
12	Total noise	V	10f
13	Resolution	bits	8
14	Slew Rate	V/µsec	625

Table 1: Comparison between Various Parameters

X. CONCLUSION

So in this work I have proposed the design which is "Dynamic comparator with regenerative latch using cross coupling mechanism" which consumes the power in micro-range of 6.13µW. Since the comparator are always remained the power thirsty block of the ADC and it is very clear that the ADC should be optimized in order to get improved performance, as result the power has considerably reduced.

Input offset voltage, it is desired to have the comparator with the minimal value of input offset voltage, it is desired that the bio-medical signal obtained via sensor should be faithfully provided to the comparator after being detected and amplified by the op-amp, parameter value obtained is 20.44mV_{rms}.

Delay, is considered as the most important specification of comparator, it basically the time taken by the signal to propagate from the input to the output. The value of parameter is 0.2ns which is very small metric obtained.

Slew Rate, The speed of the comparator is basically indicated the metric known as slew rate which signifies how fast the comparator which in turn shows speed of transition either it can be from low to high or high to low. The value of this parameter is 625V/µs.

IRN, The noise is considered as the predominant source of error in the functioning of comparator. The noise associated with the comparator deeply affects the performance of SAR ADCs. Input referred noise, when the noise contains both types of noise flicker and thermal noise as result of it the IRN is propagated along with the biomedical signal which in turn reaches the input SAR ADC such that performance is degraded. The IRN obtained from the simulation is 58.21 pV/√Hz.

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