# Implementation and Analysis of Current Reuse Technique based Stacked Inverter for AFE Cardiac Amplifier, Bio-Signal Recording System (ECG)

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*Abstract*— The paper is focused on novel design of current reuse technique based stacked inverter stage-4 amplifier .In order to achieve high performance amplifier and to achieve efficiency in terms to obtain refined signal quality, low noise and low power consumption, the architecture is proposed as analog front end instrumentation amplifier which plays vital role in determining overall efficiency of bio-signal recording system (ECG). The four stage stacked inverter design is based upon stacking of four inverters in which same bias current is shared. The common gates branches originating from the stacked amplifiers, such that current signal is aggregated from all eight pairs. Thus the overall trans-conductance of the circuit obtained is 8gm. The design is operated at 1-V power supply and implemented in 0.18 micron technology which showcase the gain of 49.57dB, CMRR is 85.29dB, noise is 150uV/√Hz @300Hz and obtained power efficiency of 1.89x10^-11W.

***Keywords:*** BMI (Bio-Medical interface), Current Reuse, Stacked Inverter, IRN (Input Referred Noise), Weak Signal, Low Voltage, ECG, Power Efficient and Bio-inspired

## I. INTRODUCTION

A dramatic change is observed in the field of healthcare equipments which focuses on curing patients essentially that has manifested an ailment in hospital environment. Healthcare industries is much more concerned about the monitoring and improvement in people's health condition those who are yet not caught by any disease and helping them to fight against disease even out of the hospital.

Microelectronics plays very important role in the medical industry efficient in monitoring the health status of people which enables the practitioner to analyze and extract the desired information about the ailment. As an example the measurement of electrical activity of the heart which is indicated by the "bio-potentials". [2]

Bio-potentials are defined as generation of voltage in turn produced from the electrochemical activity of specific cells. This activity can be obtained from cells of the nervous system, may be a muscles or glandular tissue. Electrocardiogram (ECG), Electroencephalogram (EEG), Electromyogram (EMG) waves amongst which the action potentials obtained from neuron and as well local field potentials are considered as common bio-potential signals which are deliberately recorded in modern clinical practices and daily life [3]

An ECG is a cardiac signal recording system which is responsible to measure heart's electrical activity, whereby the action potentials are propagated throughout the heart during each cardiac cycle. In which polarization takes place in one portion and depolarization another portion due to which electrical activity is generated that can be measured and captured.

An electrocardiogram (ECG) is a device which is responsible to measure the electrical activity changes of the heart such that the action potentials are propagated throughout the heart during each cardiac cycle. Whereas
One portion of heart is polarized and the other part is depolarized, which results in an electrical activity that can be measured and captured.

The battery operated portable healthcare equipments, which causes need of low voltage power supplies in CMOS circuit applications meanwhile not compromising with the power consumption. There is demand of more and more advancement in the application circuitry required to record the ultra-low amplitude cardiac signal for measurement module. Interfacing circuitry at the first stage of recording system posses the stringent constraints for the measurement of weak signals as a result monitoring of bio-potentials has become an interesting topic, since it carries health information which plays a vital role in diagnosing the cardiac related ailments used by practitioners to combat the diseases. The overall performance of signal acquisition or signal recording system can be enhanced by simply improving first stage, which comprises of instrumentation amplifier or LNA which picks the weak bio-potential and forward it to the succeeding stages.

The amplitude of cardiac signal ranges from few micro-volts to few milli-volts as result the cardiac signal at the first stage is very weak, in order to analyze the signal parameters properly, a proper architectural design of instrumentation amplifier is needed which is capable enough to boost the amplitude of weak cardiac signal, being a weak signal it's obvious of the signal being corrupted by noise and as result proper diagnose of ailment will get failed as result rejection of noise required as well as common mode voltage.[4]

The predominant parameters which decides the performance of system first is power consumption as battery operated portable ECG recording system widely used, which demands for lower power, second parameter is CMRR which is very crucial parameter for the front end amplifier in order to eliminate the interfering common mode signals in order to extract the proper signal, third parameter is gain of amplifier as it is known that the ECG signals are weak so in order to extract the information from the signal effectively it is necessary to raise the gain, fourth parameter is noise being weak ECG signals are extremely prone to external noise as result after getting coupled with signals it get corrupted and loses the information as result it becomes difficult to interpret the signals properly and analyze in order to diagnose the disease and fifth architectures are selected to operates at decreased supply voltages of 1volts in regard for portable applications.[7]

 

## II. ANALYSIS OF INVERTER CIRCUITS

In this section details of inverter is showcased which is the basic gain stage of opamp. Basic gain stage f the CMOS circuits is inverter. Common source configuration is used by the inverter with either an active load is considered as a load or either current source/ink is considered as load. The inverters include active PMOS load inverter, CS load inverter and push pull inverter which will briefly introduced in below section.

### *A. Active Load Inverter CMOS Circuit*

In many cases it is desired to achieve inverting stage which has low gain and possess required small and high signal characteristics. One of such configuration is shown in figure 1.

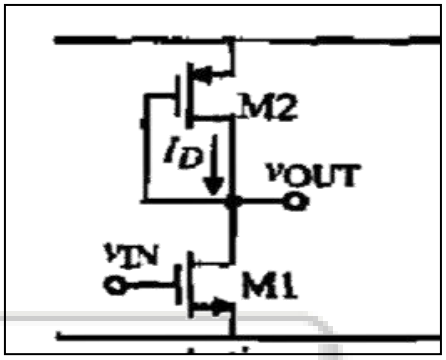


Fig. 1.CMOS circuit of Active PMOS Load Inverter [1]

The active resistor load line M2 is simply the trans-conductance characteristics reversed and subtracted with $V_{DD}$. The inverting type amplifier has low output voltage range and low gain

### *B. Current Source Inverter CMOS Circuit*

The type of amplifier is required when there is need to achieve high gain in comparison with active load inverting amplifier. The current source inverter is high gain amplifier shown in figure 2. Current source is acting as load instead of using PMOS as load.

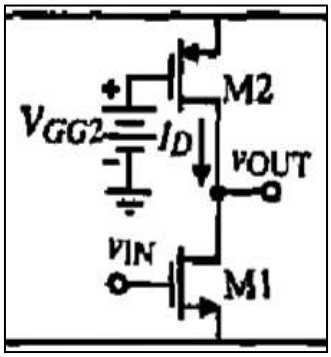


Fig. 2. CS Load Inverter [1]

The current source is basically the CG configuration obtained by making use of p-channel transistor which is connected to the dc biased voltage $V_{GG2}$. With regard to the current and voltage output characteristics for M1 obtained. In accordance to the curve $V_{in}$ is same as that of $V_{gs1}$ which is superimposed on the output characteristics of M2 with $v_{OUT} = V_{DD}-v_{SD2}$. With the analysis it is observed that there is significant rise in gain with decrease in current. As a result output conductance is proportional to the bias current and transconductance which is in proportionate to the bias current square root. There is rise in gain as $I_D$ decreases proves to be true till current reaches the sub-threshold region.

### *C. Push Pull Inverter CMOS Circuit*

If the gate of M2 is connected to the gate of M1 results in push pull inverter shown in figure 3, from the plot of push pull inverter it is found to be similar to the current source inverter. When push pull is compared to current source inverter it is observed from the graph the push pull have high gain assuming the identical transistor another advantage is that push pull produces output swing suitable for the operation from rail to rail. On comparing this topology with the previous topology is that largest gain is obtained when hen transistors are operated in saturation region. Push pull inverter small signal performance depends on the operating region and if M1 and M2 are operated in saturation region maximum voltage gain is achieved.

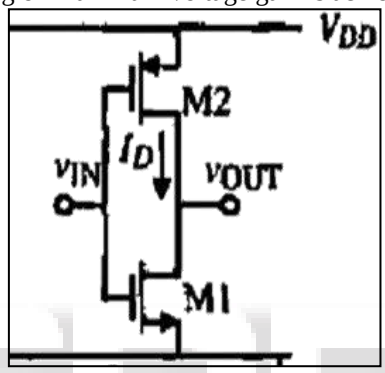


Fig. 3. Push Pull Inverter CMOS circuit [3]

### *D. Noise Analysis of Inverter Circuits*

In this section noise performance of the inverters is analyzed. First considering the active load inverter shown in the figure 4. The approach is to assume mean square of input voltage noise spectral density $e_n^2$ in series with gate of each device and then output noise is calculated $e_{out}^2$.

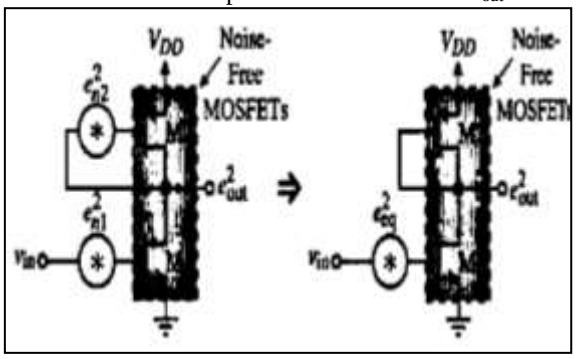


Fig. 4: Noise Modal for active load inverter [5]

Dividing $e_{out}^2$ by the voltage gain square of the inverter which is responsible to give equivalent to noise spectral density of input voltage illustrated in equation 1.

$$e_{out}^2 = e^2_{n1}(gm1|gm2)^2 + e_{n2}^2 \quad \ldots\ldots\ldots\ldots (1)$$

In accordance to the above mentioned equations if the length of M1 is considered as small as that of M2, the M1 is dominated by input 1/f noise. In order to minimize the noise of M1 its width must be reduced. In some processes it s observed that the PMOS attains low 1/f noise than that of NMOS. In such cases PMOS is employed as input stage.

 

If the trans-conductance of both MOS is made equal $g_{m1}$ and $g_{m2}$ the noise contribution is divided by 2. The noise associated with the circuit can be minimized only by the noise contributed each of the MOS individually. If the voltage source drives the inverter then the frequency response obtained is consists of single dominant pole. The small signal gain of inverter with current sink or source loads has inverse relationship to current square root which leads high gain.

## III. CIRCUIT IMPLEMENTATION OF PROPOSED CARDIAC FRONT END AMPLIFIER

### *A. Brief Introduction to Current Reuse Technique*

The noise of the amplifier and product of the power is the goal of this research work. There exist a vice versa relationship in which, power can be reduced for same noise or for same power amplifier noise can be reduced. These two parameter scenarios are interchangeable. The idea is without increasing the bias current $I_D$, to boost the overall trans-conductance of the amplifier. The design technique involves in biasing the MOS in such a way to drive MOS in weak inversion region to maximize the $g_m/I_D$.

In order to increase the trans-conductance $g_m$ , the input pair of PMOS can be stacked on the on to the NMOS input pair in order to obtain inverter based input stage, as result of the setup the overall amplifier $g_m$ get doubled but without any need of extra biasing current, since it shared by both of the pairs.

With vertical stacking of N number of inverters, 2N time current can be reused by single input channel. There is only N number, output branches of current responsible which are combined, causing exponential dependence into very less linear dependence as result power of the circuit reduced which is responsible to boost the overall efficiency of the circuit. In closed loop capacitive feedback system the amplifier fits properly. In order to minimize the requirement of power supply voltage, the tail current sources existing between stacked inverters are eliminated without making any compromise in regard to PSRR and CMRR.

### *B. Implementation of Current Reuse Technique Based Stacked Inverter-4 Amplifier*

In this proposed design of amplifier, four stage stacked inverter design is based upon stacking of inverters tend to share the same bias current. The common gates braches originating from the stacked amplifiers tends to aggregate the current signal from all the eight pairs. Thus the overall trans-conductance of the circuit obtained is $8g_m$. The approach behind designing of this amplifier is to embed it in between the capacitive feedback loop.

The input pairs are separated such that they can be biased at different voltage levels. There are total eight input pairs, as result this is known as stacked amplifier version-4. The circuit shown in figure 4.1 employs eight common gate transistors which are PMOS_ (8/10), NMOS_ (8/12), PMOS_(9/11) and NMOS_(9/13) in order to aggregate the signal obtained from the input pairs.

Small signal behavior can be analyzed, such that the total trans-conductance $g_{mt}$ of the amplifier can be given by equation 2.

$$g_{mt} = \frac{gm}{ID}(4I_D + 4I_D) \sim 8g_m \quad \text{..... (2)}$$

$I_D$ is the input bias current of the transistor; it is assumed that all the transistors have identical $g_m/I_D$ and the intrinsic gain is shown by $g_m r_o$ for all the MOS in circuit is greater than 1.

The open loop gain DM, $A_{DM}$ is given by equation 3.

$$A_{DM} = g_{mt} r_{ot} \quad \text{..... (3)}$$

The differential mode gain (DM) is the square of the intrinsic gain, which can be compared to telescopic or folded cascode amplifier. The amplifier is the combination of folded cascode amplifier and telescopic amplifier. If lower end of amplifier is considered NMOS_10 and NMOS_11 and rest of the inputs are dc biased then amplifier overall structure behave like same as telescopic amplifier and if we consider the lower end PMOS circuit input pair PMOS_12 and PMOS_13, its input and output relationship is similar to the folded cascode amplifier topology. The same consideration will be considered for the upper pair of the MOS transistors.

The amplifier input referred 1/f noise can be given by the equation 4.

$$N_{PSD} = \frac{K_f}{C_{ox}.4\,W\,L}.\frac{1}{f} \quad \text{..... (4)}$$

$K_f$ is considered as process dependent parameter, W and L are the width and length of the transistor, 1/f noise associated with the circuit can be minimized by increasing the size of the input transistor, as result in band noise will be dominated by thermal noise.

The CMRR of the circuit topology can be calculated, as CM input is applied and output DM is derived in the presence of mismatch can be given by the equation 5.

$$CMRR = \frac{A_{DM}}{A_{CM-DM}} \quad \text{..... (5)}$$

In above mentioned equation 4, $A_{CM\text{-}DM}$ expresses the CM to DM gain. The PSRR of the circuit can be illustrated by the equation 6.

$$PSRR = \frac{A_{DM}}{A_{VDD-DM}} \quad \text{..... (6)}$$

$A_{VDD-DM}$ denotes the voltage gain from $V_{DD}$ to $V_{DM}$. In order to minimize the requirement of supply voltage the dc bias voltage tends to be different. The lower end of the NMOS and PMOS pairs of circuit is quite simple to bias, in case if small deviation does exist causes minimal influence on operation of amplifier. PMOS (8/10) ,NMOS(8/12),PMOS(9/11) and NMOS(9/13) is responsible to form cascode transistors which is responsible to provide low impedance node at the drain of MOS pairs can be given as PMOS_2,NMOS_1;PMOS_3,NMOS_2;PMOS_4,NMOS_3 ;PMOS_5,NMOS_4;PMOS_6,NMOS_5;PM OS_7,NMOS_6 , PMOS_12,NMOS_10 and PMOS_13,NMOS_11. The current induced due to the mismatches between the bias and input transistors tends to flow in the CG transistors.

The transistor level implementation of current reuse based inverter stacking amplifier is implemented using 0.18µm technology shown in figure 5, from the obtained simulation it can be observed that only 2mV of weak input cardiac signal is applied to the input stage of amplifier which result in large output voltage swing which is 603mV

 

at the output node, the resulting amplified signal will further be processed by the signal conditioning circuitry. The circuit is operated at the supply voltage of 1V.

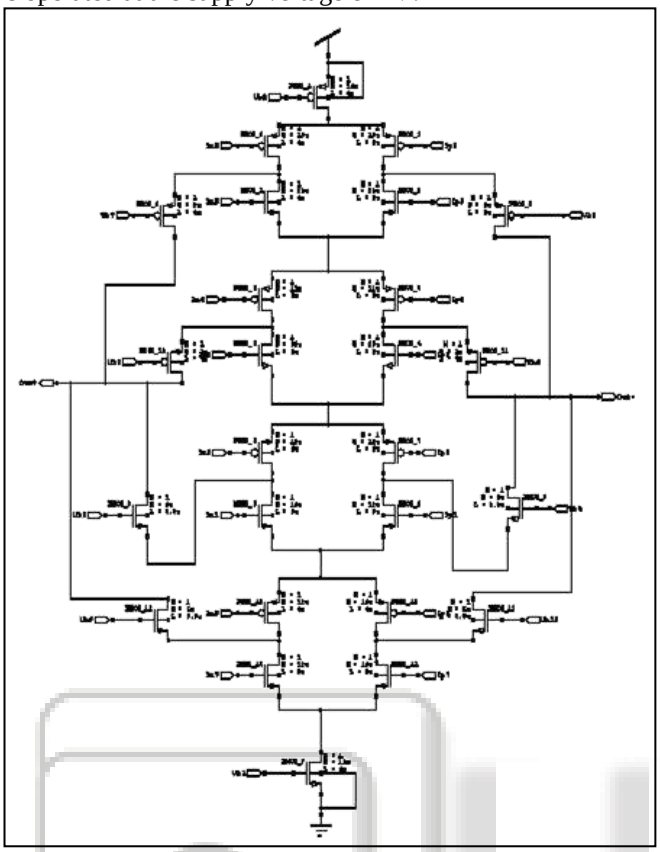

Fig. 5: Schematic Implementation using Current Reuse Technique based Inverter Based Stacked Amplifier

The dc response is shown in the figure 6, The AC response plot is illustrated in figure 7 and Noise analysis is shown in figure 8, in which magnitude of input noise (inoise), output noise (onoise) and total noise (totnoise) is represented.

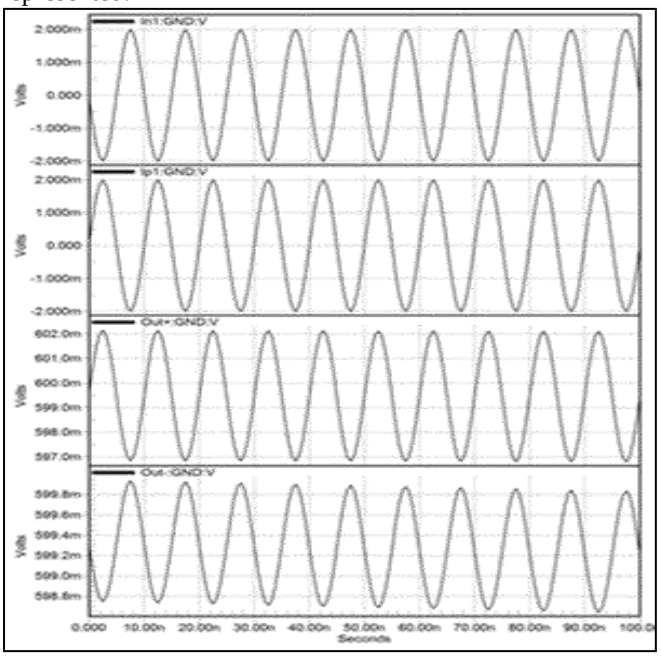


Fig. 6: Simulation Waveform Current Reuse technique based Stacked Inverter Amplifier

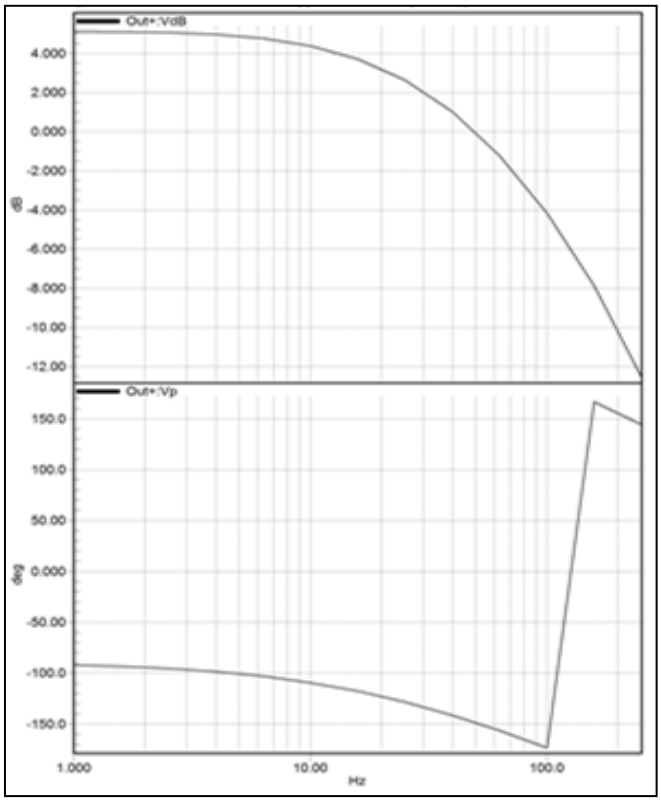


Fig. 7: AC response of Op-amp (a).Magnitude Response (dB) (b).Phase Response (Deg)

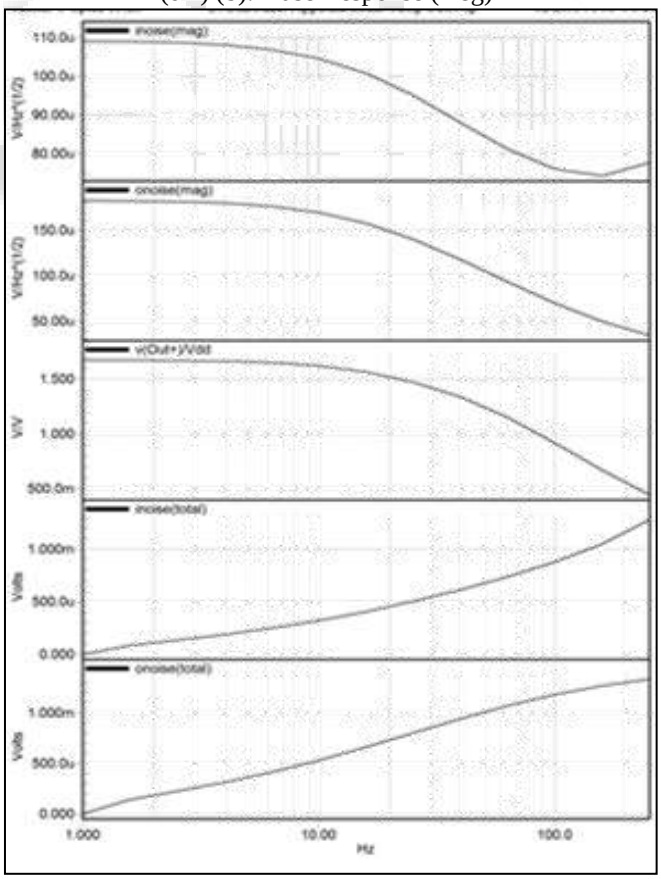


Figure 8: Noise Analysis Response of Inverted Stacked Amplifier (Using Current Reuse Technique)

*C. Performance Analysis of Current Reuse Technique Based Stacked Inverter-4 Amplifier*

| S.No | Parameters | Units | Simulated Results |
|---|---|---|---|
| | | | Inverter Stacked-4 Amplifier |
| 1. | MOS Technology | nm | 0.18 |
| 2. | Supply Voltage | V | 1 |
| 3. | Gain | dB | 49.57 |
| 4. | Phase Margin | degree | 90 |
| 5. | NEF | NA | 1.5 |
| 6. | CMRR | dB | 85.29 |
| 7. | PSRR | dB | 45.22 |
| 8. | IRN @ 300Hz | V/√Hz | 150u |
| 9. | Power Dissipation | W | 1.89x10^-11 |
| 10. | Current | A | 74f |
| 11. | GBW | Hz | 90.45k |
| 12. | Frequency | Hz | 300 |
| 13. | Figure of Merit | $NEF^2V_{dd}$ | 2.25 |

Table 1: Various Performance Parameters Analysis

*D. Discussions*

Gain, Cardiac signal is first extracted with the help of transducer which is basically the Ag-Cl electrode, as result of which ECG is converted to the electrical voltage low in amplitude lies in the range of 1mV-5mV. The succeeding stage is the analog front end bio-potential amplifier, which is considered as predominant part of the whole signal conditioning circuitry, plays crucial role in order to determine the overall performance of recording system. The gain associated with both topologies is compared; the inverter stacked amplifier with current reuse technique reflects the gain of 49.57dB with 2mV voltage at the input node of amplifier.

CMRR, Amplifier's ability to reject the common mode signals can be determined by the common mode rejection ratio, the extracted signal get distorted when coupled with noise originated from ac sources, external noise and electrode noise due to which the performance of system get disturbed and ECG signal loses the obtained information from heart. The CMRR obtained from the Inverter stacked amplifier is 85.

PSRR, The change in the output voltage of the amplifier due to change in the supply voltage is determined by the PSRR. Cardiac potentials are weak signals posses low amplitude, if such signals need proper amplification the variation in the supply voltage must be eliminated. Such disturbances detroit the performance of the recording system. The PSRR obtained from the inverter stacked amplifier using current reuse technique is 45.22dB. In order to amplify the weak bio-potentials rather than variation in supply voltage fact that such variation in supply voltage are large enough than weak bio-potential signals, it is necessary that topology must attain the high PSRR

IRN (Input referred Noise), The front end amplifier of bio-signal recording system is highly prone to noise, which is another important factor that dominates the performance and functionality of recording system. Cardiac system being weak and low frequency signals get easily contaminated with the noise. There are two types of noise which predominately affect the whole system is thermal and flicker noise are combinely know as input referred noise IRN. Thermal noise is generated by the electrode for recording and MOS of the amplifier. The IRN performance obtained from the architecture is the inverter stacked amplifier using current reuse is 150u V/√Hz .The noise should low in order to avoid debasing of weak cardiac signal. So, that the useful signal can be collected to extract the information.

Phase Margin, The parameter that determines the stability of opamp is phase margin (P.M); in order to attain proper stability of op-amp adequate phase margin is required. The more value of P.M signifies lesser amount of ringing effect, but too much P.M again causes ringing. So P.M should be at least 45 degree, preferably opamp should have 60 degree. The P.M obtained after the simulation of Inverter stacked-4 amplifier is $90^0$. Power Dissipation, The lower power consumption circuitry finds its application in battery operated portable screening devices; the bio-potential screening devices are quite bulkier and are not portable which makes it quite difficult for ongoing diagnostics and causes discomfort. Power consumption is also related to the frequency. The low power consumption is desired, else causes the excessive tissue heating also which causes discomfort in diagnosis. The power consumption exhibited by the inverter stacked-4 amplifier is 1.89x10^-11W.

Noise Efficiency Factor, NEF defines the performance of the front amplifier considered as figure of merit, NEF describes the how many times the noise of associated with the system and bandwidth is higher when compared to the ideal polar transistor. NEF depend upon the current consumption, with the low value of current good NEF is obtained. The NEF obtained from the inverter stacked-4 amplifier is 1.5.

*E. Conclusion & Future Work*

In this research paper, I have designed and demonstrated Front End Cardiac Signal Amplifier for ECG system. The first and predominant stage of the signal conditioning circuitry AFE, which is decision making circuit which defines the overall functionality and performance of system. The front end bio-potentials amplifiers or Low noise amplifier are preferred responsible for observation and amplification of weak low frequency and amplitude signal as well rejection of noise which get coupled with cardiac signal which becomes the limiting factor. The crucial parameters identified which posses constraints on design of amplifier, such as gain, NEF, noise, CMRR, PSRR and power dissipation have been optimized to obtain the considerable values. Architectures selected satisfy the above mentioned parameters.

With vast examination of bio-inspired circuit topologies which makes use of current reuse technique, I have proposed, Inverter Stacked-4 amplifier (without increasing current $I_d$, the $g_m$ is boosted up).Amplifier is implemented in 180nm technology and simulated; parameters obtained were analyzed and compared. As a result the design of inverter stacked-4 amplifier proves to achieve the better performance for the input stage of ECG recording system.

 

Performance further can be improved of front end amplifier in accordance to need of desired detection signals of heart related ailments by some techniques as mentioned is Noise cancellation techniques can be employed when need to detect precisely ultra-low voltage, in which signal current flows through path are in same phase but noise current are in 180 degree out of phase results in cancellation of noise.
Feedback techniques can be implemented while designing bio-potential amplifiers which are responsible to shift optimum noise impedance to desired point; it reduces the non-linearity of circuit.

Recording system in future should be completely implantable in order to avoid the infection risk, such that without any intervention of human tuning can be done.
In future, ECG recording system should be compact, so that they can be directly integrated with sensing electrode.

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