

# 5-Level Symmetrical Cascaded H-Bridge Multilevel Inverter with Level Shifted PWM Techniques

Mr. Sachin Kapadiya<sup>1</sup> Mr. Arpan Patel<sup>2</sup> Mr. Kaumil Shah<sup>3</sup>

<sup>1,2</sup>M. Tech Student Scholar <sup>3</sup>Assistant Professor

<sup>1,2,3</sup>Sankalchand Patel College of Engineering, Visnagar, Gujarat, India

**Abstract**— This paper aims to extend knowledge about the performance of Multicarrier Based Level Shifted Pulse Width Modulation Using Symmetrical Cascaded H-Bridge Multilevel Inverter. Multilevel Inverters are having more importance in renewable energy applications. Multilevel inverter utilization has been increased since the last decade due to the drastic improvement in the harmonic profile and increased power rating of MLI made them highly popular and high-power applications. Due to the abilities to synthesize waveforms with better harmonic spectrum these inverters are suitable various High-Voltage and High-Power Applications. Asymmetrical type Multilevel Inverter is used for reducing the number of DC sources, Gate Drive Circuits and Bridges. Among the carrier-based pulse width modulation (PWM) techniques, phase-shifted PWM (PS-PWM) is preferred for cascaded H-Bridge (CHB) Multilevel inverters.

**Keywords:** Cascaded H-Bridge (CHB) Multilevel Inverter, Asymmetrical Multilevel Inverter, Symmetrical Multilevel Inverter, PWM Techniques, Multilevel Based Sinusoidal Pulse Width Modulation

## I. INTRODUCTION

In this modern era there is a huge power requirement in industries and other areas. Multilevel inverters (MLI) has become very popular to fulfill power requirement [1] due to the advantage of high-power quality waveforms, low electromagnetic combability. Also, multilevel conversion reduces the output variables harmonic distortion and sometimes, despite the devices count increment, the conduction losses can also be decreased by increasing the number of levels [2].

The main conception of multilevel inverter (MLI) is to achieve higher power by using the number of power switches with several low voltage dc sources. It can produce output voltage waveform in steps which are closer to a sine wave and reduces total harmonic distortion. Important points regarding the topological structure of multilevel inverter [3] are:

- It should have fewer switching devices as far as possible.
- It should be capable of enduring very high input voltage such as HVDC transmission for high power applications.
- Each switching device should have a lower switching frequency owing to the multilevel approach.

Recently multilevel inverters have been used in various industrial applications like distributed generation, adjustable speed drives, flexible ac transmission system, HVDC, electrical vehicles, etc. due to noticeable advantages like high-quality output voltage using low switching frequency, low harmonic contents, low electromagnetic interference, less voltage stress on power switches, more

efficiency and low  $dv/dt$  stress on load [4] – [9]. Improvement in these advantages is possible by increasing the number of levels of output voltage waveform but it requires a large number of switches that make the circuit complex. It also raises the cost and size of the circuit [3].

The multilevel inverter has three types [10]:

- Diode clamped multilevel inverter
- Flying capacitor multilevel inverter
- Cascaded H-Bridge multilevel inverter

The most commonly efficient inverter is a cascaded multilevel inverter. It provides higher output voltage and power levels. It is one of the methods used for drive applications that meet the requirements such as high-power rating with reduced THD and switching losses [10]. The advantages of CHB inverters over other multi-level inverters are

- 1) It doesn't require diodes or capacitors for clamping.
- 2) It doesn't need any filter since the output waveform is nearly a sine wave.

There are so many techniques available namely Sine PWM (SPWM), Space Vector PWM (SVPWM) [11] to generate pulses to the switches in these multilevel inverters so that the output voltage is nearly sinusoidal and contains less number of harmonics. The SPWM technique can be extended to multilevel inverters by using multiple carrier signals so it is called a Multi-Carrier PWM technique.

There are two types of DC sources which are Asymmetrical DC source and Symmetrical DC source. Asymmetrical DC source has an unequal magnitude of voltage and Symmetrical DC source has an equal magnitude of voltage. Asymmetrical cascaded MLI has less number of DC source voltage and switches as compared to symmetrical cascaded MLI.

## II. CASCADED H-BRIDGE MULTILEVEL INVERTER

Cascaded H-Bridge Multilevel Inverter consists of series-connected H-Bridges and each H-Bridge is supplied by an isolated DC source of identical value on its DC side and connected in series on their AC side [12].

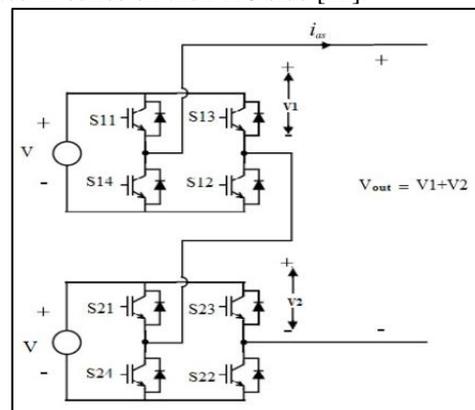


Fig. 1: Single Phase Cascaded H-Bridge (5 – level MLI)

Fig – 1 presents the total output voltage is the addition of voltage produced by each H-Bridge connected to from circuit. There are three voltage levels state as a positive voltage level, zero voltage level and negative voltage level. These voltage levels can be achieved by various arrangements four switches of H-Bridge.

If ‘m’ number of H-bridges are joined in series then total voltage across the load is,

$$(V_{an}) = (V_0)_1 + (V_0)_2 + \dots + (V_0)_m$$

$$(V_{an}) = \sum_{k=1}^m (V_0)_k \quad (1)$$

### III. SYMMETRICAL CASCADED MULTILEVEL INVERTER

In cascaded H-Bridge Multilevel Inverter, each cell supplied by the same magnitude of DC source is called symmetrical cascaded H-Bridge multilevel inverter.

The magnitude of the DC source can be given by

$$V_k = V_{dc} \quad k = 1, 2, \dots, m. \quad (2)$$

$$V_1 = V_2 = \dots = V_m = V_{dc}$$

The total number of output voltage levels ‘n’ in symmetrical multilevel inverter is given by

$$n = 2m + 1 \quad (3)$$

where ‘n’ is the number of power cells used for cascaded structure the maximum voltage generated by this arrangement is

$$V_M = m * V_{dc} \quad (4)$$

For example, if  $m = 2$  as shown in Fig. 1 it generates 5 level voltage with maximum voltage  $2V_{dc}$ .

### IV. CONTROL SCHEME

Pulse width modulation technique helps in maintaining a constant voltage and to get information about the train of pulses, the information is encoded in the width of each pulse [13].

A popular approach to control the CHBMLI is to employ a carrier-based PWM technique where the high-frequency carrier signals are compared with reference wave (usually sinusoidal wave) of the fundamental frequency. Carrier-based modulation schemes are mainly divided into two categories: level-shifted (LSPWM) and phase-shifted (PSPWM) methods. Both of these have several variations, which differ by the allocation of module carriers concerning each other [14].

In carrier-based modulation of multilevel, each level in phase requires its carrier. An m-level cascaded h-bridge inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers and they are in same frequency and magnitude

There are three kinds of level shifted multicarrier modulation techniques,

- Phase Disposition
- Phase Opposition Disposition
- Alternative Phase Opposition Disposition

In Phase Disposition (PD), all the carriers are in phase across all the bands. This gives rise to the lowest harmonic in the higher modulation indices as compared to the other disposition methods. In Phase Opposition Disposition (POD) the carriers above the reference point, are out of phase with those below zero, by 180 degrees. In the Alternative Phase Opposition Disposition (APOD), the

carrier of adjacent bands is phase shifted by 180 degrees. Fig. 2, Fig. 3 and Fig. 4 show the arrangement of the carrier waveform concerning the reference waveforms for PD, POD and APOD techniques, respectively [15].

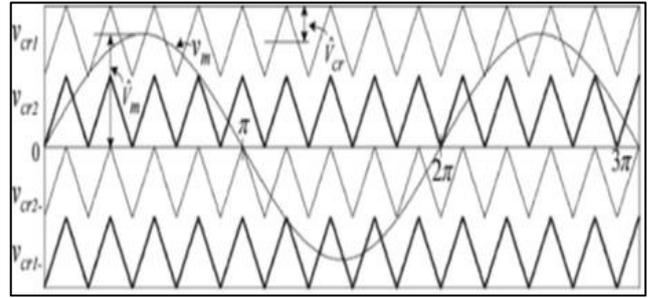


Fig. 2: Carrier Arrangement of PD [15]

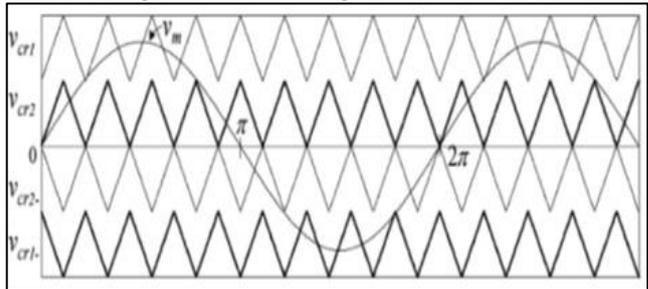


Fig. 3: Carrier Arrangement of POD [15]

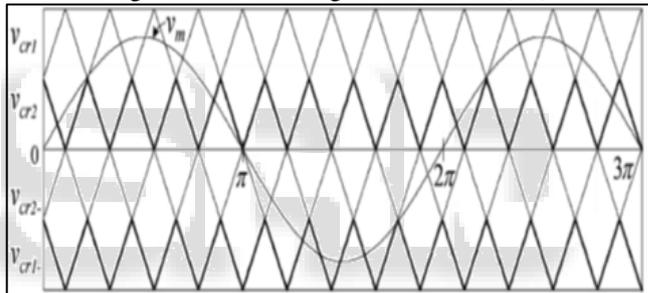


Fig. 4: Carrier Arrangement of APOD [15]

### V. SIMULATION RESULT

All the three multicarrier techniques are applied to 5 – level cascaded h-bridge multilevel inverter. Simulation is carried out in PSIM simulation software by using the following parameters.

Parameter	Value
DC Voltage	120v
R1	220ohm
L1	0.25H
Reference freq. (fr)	50Hz
Carrier Freq. (fc)	1000Hz
Modulation Index (m)	1
Frequency Modulation Ratio (mf)	20
Number of DC source	2
Number of switches	8
Number of H-Bridge	2
Voltage level	5

Table 1: Parameter used in Simulation

When the reference waveform is more than the carrier wave, a pulse is produced. The pulses produced by the comparison of a reference sine wave with upper and lower carriers, are given to the H-bridge 1 and the pulses

produced by the comparison of a reference sine wave with the middle two carrier waves, are given to H-bridge 2. The simulation circuit is shown in fig. 5 and the circuit for the three-phase is constructed by taking the reference sine wave with a phase shift of 120 and 240 degrees for the other two phases.

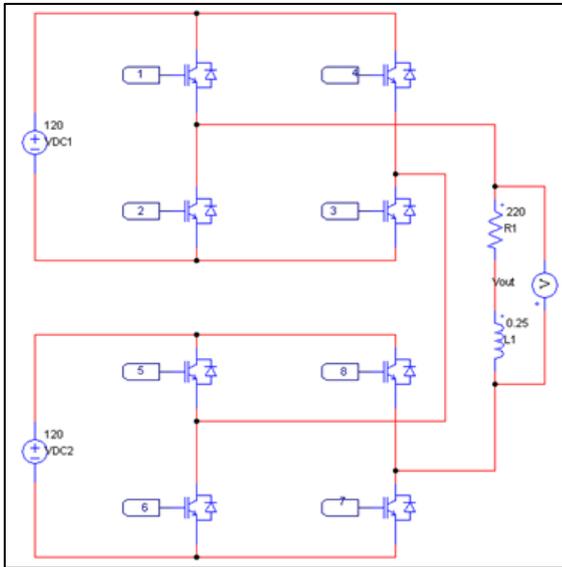


Fig. 5: Simulation Diagram of CHB-MLI for PWM technique

The output voltage and corresponding Harmonic pattern are taken. Fig. 6 to fig. 11 shows voltage and corresponding harmonic pattern also shows PD-PWM, POD-PWM and APOD-PWM applied to 5-level cascaded h-bridge multilevel inverter when modulation index is one.

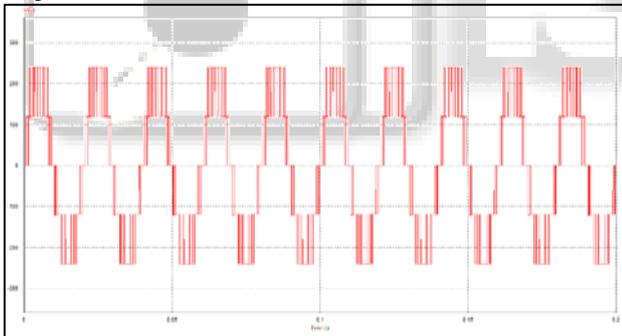


Fig. 6: Phase voltage for PD-PWM technique applied to 5-level CHB when m=1

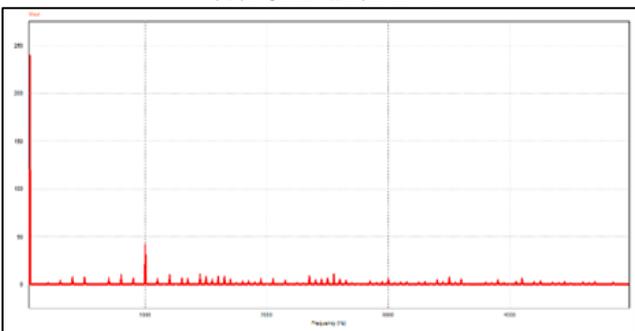


Fig. 7: Harmonic order for PD-PWM technique applied to 5-level CHB when m=1

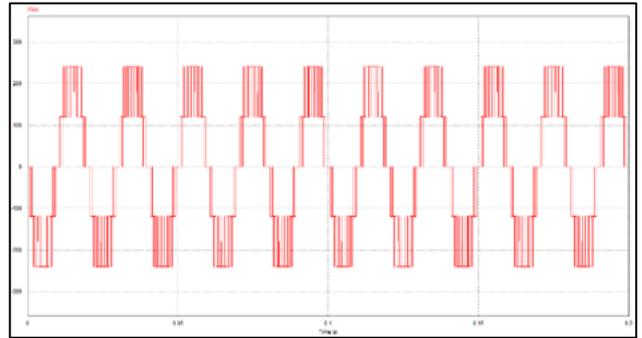


Fig. 8: Phase voltage for POD-PWM technique applied to 5-level CHB when m=1

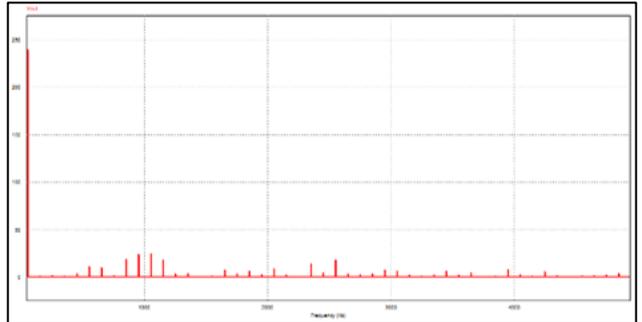


Fig. 9: Harmonic order for POD-PWM technique applied to 5-level CHB when m=1

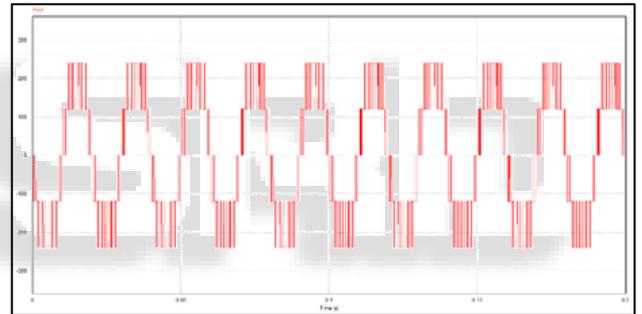


Fig. 10: Phase voltage for APOD-PWM technique applied to 5-level CHB when m=1

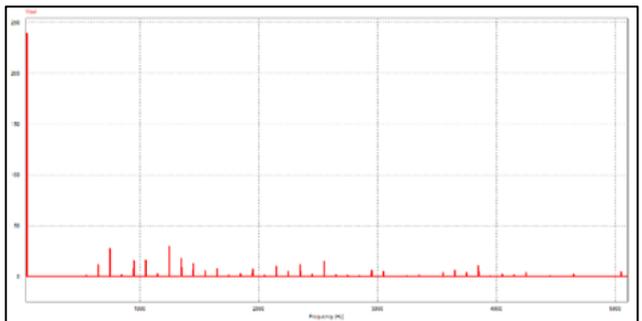


Fig. 11: Harmonic order for APOD-PWM technique applied to 5-level CHB when m=1

PWM Technique	Modulation index m=1		
	Peak of fundamental voltage	Fundamental Frequency	%THD
PD-PWM	235.44v	50Hz	26.81%
POD-PWM	235.32v	50Hz	26.31%
APOD-PWM	235.44v	50Hz	28.07%

Table 2: Output voltage and Percentage Harmonic for modulation index m=1

## VI. CONCLUSION

The paper deals with the three types of multicarrier PWM techniques (PD-PWM, POD-PWM and APOD-PWM) that have been applied to the cascaded H-Bridge multilevel inverter. The phase and corresponding harmonic order are shown for the modulation index  $m=1$ . Cascaded H-Bridge multilevel inverter is best based on FFT analysis observed from simulation results. Based on cost and switching losses with single DC source, Cascaded H-Bridge Multilevel inverter is better than another multilevel inverter.

## REFERENCES

- [1] Rashid, M. H, 2004. "Power Electronics: Circuits, devices, and applications". Third Edition, Prentice-Hall.
- [2] K.N.V. Prasad, G. Ranjith Kumar, T.Vamsee Kiran, G. Satya Narayana, "Comparison of Different Topologies of Cascaded H-Bridge Multilevel Inverter" International Conference on Computer Communication and Informatics (ICCCI -2013), Jan. 04 – 06, 2013, Coimbatore, INDIA.
- [3] Prayag, Aparna, and Sanjay Bodkhe. "Performance Evaluation of Symmetrical and Asymmetrical Cascaded H Bridge Multilevel Inverter Topology." International Journal of Engineering Research and Applications, vol. 07, no. 07, 2017, pp. 20–24., DOI:10.9790/9622-0707102024.
- [4] J. Rodriguez, J-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Industrial Electronics, Vol. 49, No. 4, pp.724-738, Aug. 2002.
- [5] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," IEEE Trans. Ind. Appl., Vol. 35, No. 1, pp. 36-44, Jan./Feb. 1999.
- [6] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [7] A. Nabae, I. Takahashi, H.Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. App. vol. IA-17, No.5, pp 518-52, Sept/Oct. 1981.
- [8] F. Z. Peng and J. S. Lai, "Multilevel cascade voltage-source inverter with separate DC source," U.S. Patent 5 642 275, June 24, 1997.
- [9] T. A. Meynard, H. Foch, "Multilevel conversion: High voltage choppers and voltage source inverters," IEEE-PESC Conference Record, pp.397-403,1992.
- [10] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel Inverters: A survey of topologies, controls, and applications," Industrial Electronics, IEEE Trans. Ind. Electronics, Volume 49, no. 4, pp. 724-738, 2002
- [11] Satya Venkata Kishore, Dhana Prasad Duggapu "Hardware Implementation of 3-Phase Three Level Diode Clamped MLI Using SVPWM Technique", International Journal of Emerging Trends in Electrical and Electronics, ISSN: 2320-9569, Vol. 12, Issue. 9, September-2016.
- [12] Farid Khoucha et al," A comparison of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives," IEEE Trans. on Energy Conversion, vol.. 26, no. 1, Mar.2011
- [13] P.T.Josh, Jovitha Jerome, Arul Wilson, The Comparative Analysis of MultiCarrier Control Techniques For SPWM Controlled Cascaded H-Bridge Multilevel Inverter" 978-1-4244 7926-9/11 ©2011 IEEE.
- [14] Jannu Ramu, S.J.V. Prakash, K. Satya Srinivasu, R.N.D. Pattabhi Ram, M. Vishnu Prasad2 and Md. Mazhar Husain, "Comparison between Symmetrical and Asymmetrical Single Phase Seven Level Cascade H-Bridge Multilevel Inverter with PWM Topology", International journal of multidisciplinary sciences and engineering, Vol. 3, No. 4, April 2012.
- [15] High-Power Converters and ac Drives, By Bin Wu © 2006, The Institute of Electrical and Electronics Engineers, In