Fault Detection in Analog VLSI Circuits using Signal Flow Graph: A Review

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Abstract— The purpose of this paper is both a review and an assessment of techniques presently available for fault detection in analog circuits. Analog circuits have been extensively used in industrial systems and their failure may make the systems work abnormally and even cause accidents. So if these faults cannot diagnose and remove at early stage it will cause problem. There are various faults occur in analog VLSI circuits during manufacturing of any analog circuits and if these faults are not diagnose at initial stages they will make changes in the output of the circuit and overall cost will increase. In this paper an approach is taken to remove parametric and catastrophic faults. A very simple, efficient and structural approach is taken which is based on signal flow graph. In this back-tracing is done using inverted signal flow graph which is used to calculate tolerance of the component. This approach is applicable to various linear analog VLSI circuits. For the detection of faults integrator circuit is used. All the circuits are simulated with the help of MATLAB/Simulink tool.

Keywords: Parametric Fault, Catastrophic Fault, Analog VLSI Circuit, SFG, Reverse Simulation, Analog Back-Tracing

I. INTRODUCTION

Now a day in semiconductor industries those circuits are more preferred which are faster, designed in shorter times at lower cost. Due to this there is a remarkable change in the field of Integrated Circuits which demands high speed VLSI Integrated Circuits. Integrated Circuits incorporating both digital and analog functions are popular in semiconductor industry. However, the methodologies for testing and fault diagnosis are well established in digital circuits. Most previous work in test generation focuses on digital circuits using the classical stuck at fault model since most potential physical faults can be mapped to a node stack-at a logical 1 or 0[3]. The fault diagnosis in analog VLSI circuits are relatively less explored and it is very difficult task due to complexity nature if analog VLSI circuits. Due to various reasons analog circuits are not proper tested like their complex electrical nature, lack of proper fault model of the devices operating in the continuous time domain, multiple value of the signal at each node of the circuit etc.[1] However, there is no simple fault model for testing analog circuits as there in digital circuits. There are several open challenges for the design, simulation and testing of analog VLSI circuits.

Fault simulation is an aid in generating tests for faults, provides support for diagnostics, and analyzes the circuit in presence of fault for reliability studies. This is popular method for distinguish the good chips from faulty ones. There are two categories of fault model: Soft or Parametric Fault and hard or Catastrophic Fault. Parametric faults are defined as the variation in component values and hard faults are open or short circuits. The parametric fault cause due to change in component value due time and environment. Most of the research proposals are for parametric faults detection because parametric faults lead to system performance degradation and are hard to detect. Catastrophic Fault there is large deviation at output due to large variation in component values (due to short or open circuit). [4] Catastrophic failure is a complete, sudden, often unexpected breakdown in a machine, electronic system, computer or network. Such a breakdown may occur as a result of a hardware event such as a disk drive crash, memory chip failure or surge on the power line. Catastrophic faults are easy to test but parametric faults are difficult to test. The testing of analog circuits consumes 30% of total manufacturing cost of product. This huge cost occurs in testing of analog circuits because large number of functional measurements is required for testing, which consumes a lot of time for testing a single circuits. To solve this problem Structural analog circuit testing is preferred, which consume less time and does not require large number of functional measurement. In Structural analog circuit, test waveform is generated which verify which components or ratio of components are within specification. The application of such method is amplifier and filtering circuits, which contain blocks in cascaded form to obtain transfer function.

In this paper fault detection of analog circuit is done using signal flow graph technique. First the analog circuit which is to be tested is taken and its transfer function is computed. Than its signal flow graph is constructed. Than its Laplace domain equation is build and then continuous Laplace domain is transformed to the discrete Z-domain[3]. Then finally fault coverage of the circuit is done. Fault coverage refers to the percentage of some type of fault that can be detected during the test of any engineered system. We simplify the problem of test generation and fault definition to one of reverse simulation by inverting a circuit path from a primary input (PI) to primary output (PO) in the SFG and working backwards from the PO with good and bad outputs to find component tolerances as well as to calculate test inputs. This process is known as analog backtrace. In this paper we proposed a test generation and fault modeling of analog VLSI circuits using signal flow graph.

The final paper but after the final submission to the journal, rectification is not possible.

II. PROBLEM DEFINITION IN ANALOG VLSI CIRCUITS

Problem occur in analog VLSI circuit testing are [1],[4]

- To determine when a circuit is faulty as well as when a component is faulty.
- Complex relationship between input and output.
- Lack of simple analog fault model.
- The infinite range of analog values as opposed to the Boolean digital values.

These problems are narrow down with the following characteristics[1],[4]:

- They are linear in nature and first order blocks are easily designed using signal flow graph.
- Second order circuit can easily realizable by cascading first order blocks.
- Blocks of higher order than second are extremely sensitive to component deviations and are very rarely used

III. SIGNAL FLOW GRAPH AND ITS INVERSION

A signal-flow graph or signal-flow graph (SFG), invented by Claude Shannon, but often called a Mason graph after Samuel Jefferson Mason who coined the term is a specialized flow graph, a directed graph in which nodes represent system variables, and branches (edges, arcs, or arrows) represent functional connections between pairs of nodes. Thus, signal-flow graph theory builds on that of directed graphs (also called digraphs), which includes as well that of oriented graphs. Nodes can be source nodes, with outgoing edges only; sink nodes, with incoming edges only; [5]. The value of graph node (state variable) i is

Value (i) = Σ (parent node value) × (incoming edge weight) (1)

Consider equations as an example of SFG

$x_2 = a.x_1 + b.x_3$ (2)

$x_4 = -c.x_2$

SFG of these equations is in fig 1

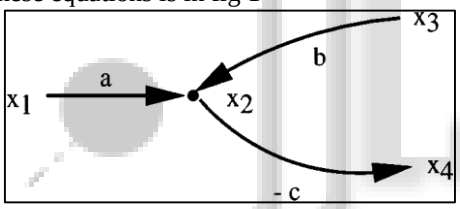

Fig. 1: Signal flow graph of Eq. (2)

A. Inversion Algorithm of SFG[1][4]

- Select a path from primary input nodes through intermediate nodes to primary output node.
- Start at the primary input $x_1$node, a source node with only outgoing edges.
- Reverse the direction of the outgoing edge from x_1 to x_2, and the new weight 1/a is the reciprocal of the old weight a. x1 becomes a sink node (with incoming edges only).
- Redirect all edges incident on x_2 to x_1, multiply the original weights by the new weight 1/a on the reversed edge from x_2 to x_1, and change the sign.
- Repeat Steps 3 and 4 for all source nodes x_i on the path from PI x_1 to PO x_n, until x_n becomes a source node. At this point, since all of the graph edges point towards the input, the graph is inverted.

Consider equations:

$x_2 = a.x_1 + b.x_3$

$x_4 = -c.x_2$

Only incoming edges have any effect on the value of a node, so x_4 has no effect on node x_2. So equation becomes:

$x_2 = a.x_1 + b.x_3 + c.x_4$ (3)

Signal flow graph of this equation is in fig 2 (a)

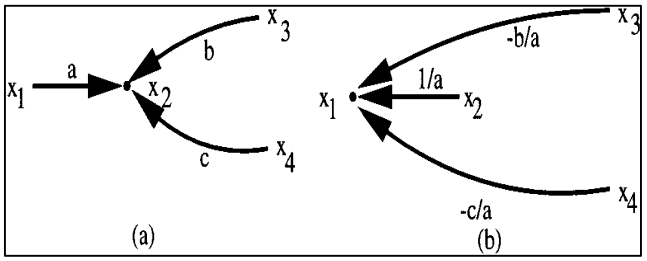

Fig. 2: Signal flow graph of (a) Eq. (3) and (b) Eq. (4).

Balabanian's [13] approach describes to convert source node to sink and vice-versa. So by changing source node to sink and sink node to source we obtained ISFG of equation (4) as shown in figure.

$$x_1 = \frac{1}{a} x_2 - \frac{b}{a} x_3 - \frac{c}{a} x_4$$

B. Implementation of Inversion Algorithm using analog VLSI circuits [1],[4]

Consider the integrator circuit in fig 3, its consecutive SFG are formed in fig 4 and the equivalent Eq. (5)

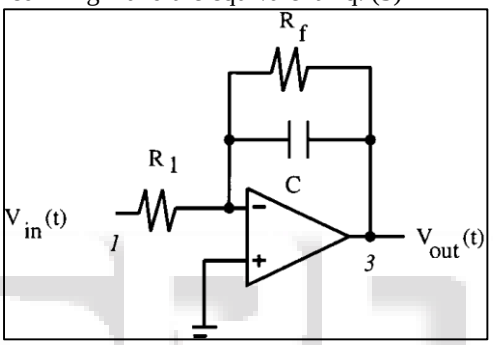

Fig. 3: Real Integrator circuit.

$$Z_f = \frac{Rf\frac{1}{sC}}{Rf+\frac{1}{sC}} = \frac{Rf}{s\,Rf\,C+1}$$

$$Vout(s) = -Vin(s)\frac{Zf}{R1} = -Vin(s)\frac{1}{sR1C+\frac{R1}{Rf}} \quad (5)$$

Nodes 1 and 3 of the SFG correspond to the circuit voltage input and output, respectively. Figure 4(a) shows the original SFG of the integrator, with a self-loop on the output. Node 2 in Fig. 4(b) is a dummy node introduced to avoid a self-loop on the output node—it has a weight of 1/s that was common to both edges in the original graph. Differentiation (represented by the s operator) is a linear operation. Hence, multiple edges with non-zero s weights in the SFG of a single first-order block can be combined to produce multiple edges with ordinary numerical weights and one edge with non-zero s weight. This helps in reverse simulation, as numerical differentiation, an expensive operation, done only once.

After Steps 3 and 4 of the algorithm, we have the intermediate SFG in Fig. 4(c). The edge with weight -1/R1C has been reversed and its new weight now $-R_1C$. The edge from the output, with weight $-1/R_fC$, has been redirected to the input node, and its new weight is $-(-R_1C\times-1/R_fC) = -R_1/R_f$. There remains only one more edge to be inverted: the intermediate edge to the output with weight 1/s. It is inverted with the new weight becoming s; at this stage we stop, the output having become a source node and the input a sink node [1][4]. Figure 4(d) shows final inverted graph and is equivalent to the equation:

$$Vin(s) = -R1C \times s\left(Vout(s)\right) - \frac{R1}{Rf} Vout(s) \quad (6)$$

All cycles in the original SFG are broken in the inverted graph, which is now a feedforward network. All of node is parents in the inverted graph will be closer to the circuit output than i. In SFGs, input and output are merely labels, and are interchangeable. We can simulate the inverted SFG with a chosen output to find the original network input. The s operator in the Laplace domain corresponds to differentiation in the time domain. We start with a set of output samples. The inverted graph weights are all either numerical scalars or s, the differential operator that can be numerically approximated. We can find all inverted graph node values using Eq. (1). This process finds the input corresponding to a given output, but non-linear networks must have a non-linear block input constrained to a constant before a SFG can be built for reverse simulation. We may have to search among many possible constant inputs to find an acceptable test. We provide a new ability to work backwards in an analog circuit during test generation.

We took original sample from MATLAB model in time domain to perform reverse simulation. Most samples were equally spaced apart in time domain and is set of samples taken. Then second order differentiation is done using this formulae

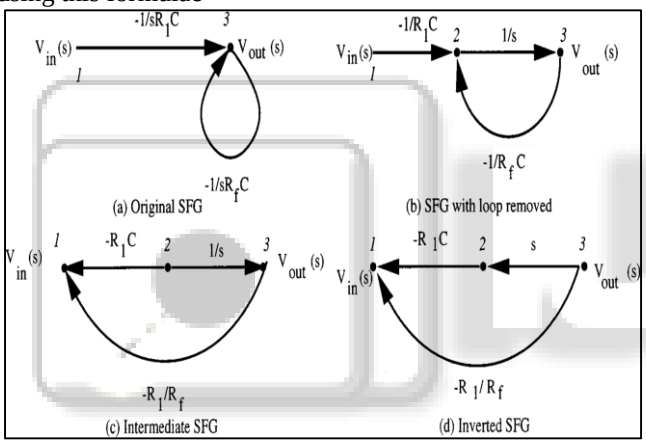

Fig. 4: Original and modified signal flow graphs of the integrator.

IV. FAULT MODELLING

There are various types of faults[11] :

- Deviation Fault: The value of a parameter deviates in a continuous manner with time or with environmental conditions up to an unacceptable value.
- Catastrophic Faults: Those faults caused by a sudden and large variation of a parameter (e.g., short, open, break-down).
- Parametric Faults: Those faults where a component value varies with time and/or environment, causing unacceptable circuit behavior.
- Single Faults: Those faults concerning only one parameter or a component at a time.
- Multiple Faults: Those faults concerning simultaneously several parameters or components.
- Independent Faults: Two or more faults are independent when the occurrence of one does not cause the occurrence of the others.
- Dependent Faults: Occurrence of one fault causes occurrence of the others.
- Permanent Faults: Those faults as long as they are not repaired (e.g., short, open).
- Intermittent Faults: Those faults occurring only temporarily (e.g., bad contact sensitive to vibrations).
- Stray Faults: Those faults occurring only once and whose effect is self-repairing (e.g., self-healing of isolation losses in some types of capacitors).

For analog circuits mostly two faults are given importance: catastrophic or hard faults and parametric or soft faults. Catastrophic faults are those which [5] completely change the output of circuit this cause the structural deformations like short or open circuits which change the circuit topology or cause large variations in design parameters. These are random faults.

Parametric faults are those where an analog R, L, C or transistor trans-conductance value changes sufficiently that it moves outside its tolerance box and cause unacceptable performance degradation of the analog circuit. Because the values of component is increase or decrease to the certain value. This type of fault we can remove with the help of knowing the tolerance of component. These faults are also caused by process gradients which produce device mismatch.

V. ANALOG BACKTRACING USING SFG

Reverse simulation algorithm can be for fault diagnosis, we use analog back trace method. We start from output voltage waveform tolerance [1] and go backward to find Good and Bad value of outputs. By using this we calculate the tolerance value of components.

By using this method we can calculate [4] the parameter of the circuit components (during manufacturing process) to ensure that output waveform remain within designer specification. Integrator circuit is used for analog back trace method. In this we assume that R1 resistor is faulty and it changes the characteristics of circuit. Now bad value of faulty resistor R1 is calculated which causes change in output waveform. Here faulty edges are shown by dash edges

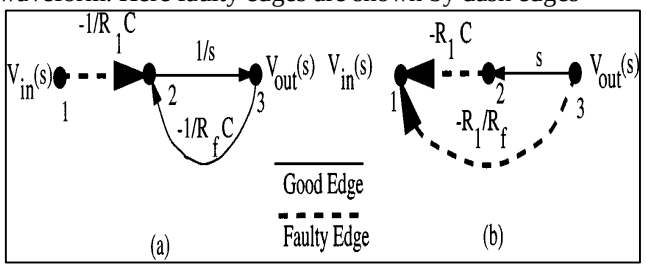

Fig. 5: Original and inverted SFGs for integrator.

By using [4] fig 5 we write the equation of good value and bad value

$$\text{Good value (1)} = -\text{R1 C Bad value(2)} - \frac{\text{R1}}{\text{Rf}} \text{ Bad value (3)}$$

This can be arranged

$$\frac{\text{Good value (1)}}{-\text{R1 C}} + \frac{\text{Bad value (3)}}{-\text{Rf C}} = \text{Bad Value (2)}$$

$$\text{Bad value (R1)} = \frac{-\text{Good value(1)}}{\text{C (Bad value (2)} + \frac{\text{Bad value(3)}}{-\text{RfC}})}$$

$$\text{Good Value(R1)} = \frac{-\text{Good Value(1)}}{\text{C(good value(2)} + \frac{\text{good value (3)}}{-\text{RfC}})}$$

$$\text{Tolerance} = \text{Good value(R1)} - \text{ Bad Value(R1)}$$

The good values are those values which are original values and bad values are those which have some deviation from the original. By using these equations we are able to find out maximum deviation for R1.

Each component tolerance value is calculated using different values of good and bad node.

VI. Implementation of Algorithm

The algorithm for fault modeling and detection is constructed with the help of MATLAB and Simulink. [7] The entire algorithm to compute fault in circuits is shown in Fig. 8. With the help of given algorithm we can easily detect the fault in analog VLSI circuit. In this paper we applied our algorithm to an integrator circuit. Before the implementation of testing method, the method should be applicable to the circuit.

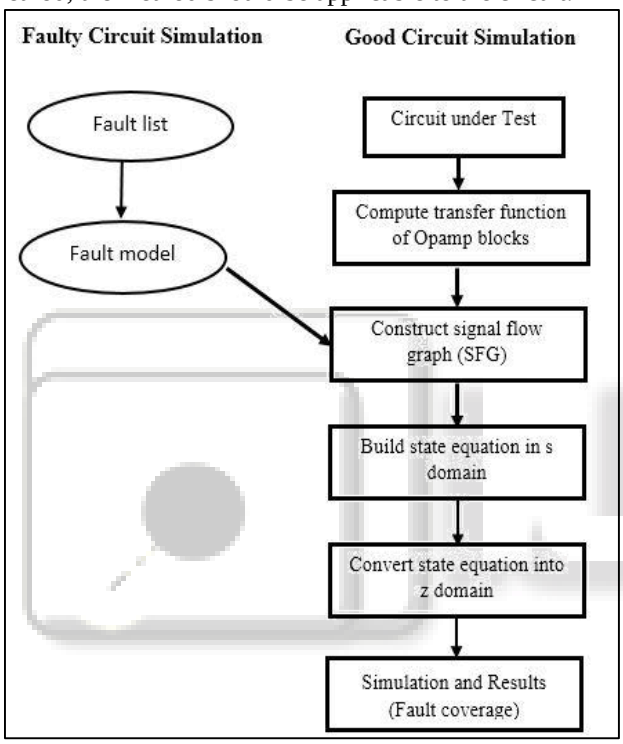

Fig. 6: Algorithm used for fault simulation [7]

VII. Conclusion

A test approach which is based on new reverse simulation method for backtracing in analog VLSI circuit to locate catastrophic or parametric faults in linear analog circuits is proposed. The fault in analog circuit is defined in terms of magnitude deviations and developed a fault definition strategy for analog circuit component. Reverse simulation method does not either required a large time of span and neither expensive in nature because this operation is done only during test waveform generation. This method generates more effective test waveforms and also structural in nature which does not required functional testing as DSP based techniques required. This method is highly accurate and has the capability to reduce the number of measurement required during analog testing; hence it reduces testing time also. This approach is applicable to second order blocks which existing methods does not handle. y. In this paper all the simulation and calculation for transfer function ,state equation in s domain as well as z domain are done with the help of MATLAB and all model for algorithm are construct with the help of SIMULINK.

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