Implementation of Multilevel Inverter Topology for Removing THD and Improving Cost Function

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Abstract— The paper presents the performance analysis of multi-level inverter under various loading conditions. The multilevel topology proposed is series connected H-bride type and the modulation techniques are evolved to produce level shifted PWM in a way to get pulses with low component requirement to get the high level output. The THD analysis is also done for verifying the performance of the proposed topology. The designed topology of cascaded MLI is obtained for both single phase and three phase. The same loading analysis for THD is done for both single phase and three phase system. And the comparative analysis is done with reference to the conventional topologies.

Keywords: Multilevel Converter, Total Harmonic Distortion (THD), Neutral Point Clamped, Cascade H-Bridge (CHB), Level Shifted Pulse Width Modulation (LSPWM)

I. INTRODUCTION

As the field of high voltage, high power applications, is increasing day by day there has been a great demand of Multi level inverter (MLI) since the two level inverters has high harmonic content. In MLI switching frequency has to be limit upto1 KHz, even with the high voltage insulated gate bipolar transistor (HVIGBT) and gate commutated thyristors (GCT), due to the increased switching loss. So the harmonic reduction by raised switching frequency of a two-level inverter becomes more difficult in high power applications. In addition, as the dc link voltage of a two-level inverter is limited by voltage ratings of switching devices, the problematic series connection of switching devices is required to raise the dc link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult. From the aspect of harmonic reduction and high dc-link voltage level, multi-level approach seems to be the most promising alternative. The harmonic contents of a MLI are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage. The more the level of output voltage of MLI lesser will be the THD. For example seven level has less THD than five level consequently nine has low harmonics than the seven [1].

However, the increased level of inverter has inherent cost addition feature since more number of components are required. It also increases the complexity of the inverter topology and a bulky PWM technique is also required.

So many PWM strategies have been proposed to solve this problem [2], [3], [5]. But many of them are focused mainly on the neutral-point potential control method, while still using the complicated dwelling time calculation and the switching sequence selection method.

In literature numerous MLI topologies are proposed which can increase the level of output voltage as much as desired. This paper presents a simple cascaded MLI topology for eleven level inverters using various level shifted modulation techniques. The proposed PWM strategies solve the problem of component requirement and harmonic content. Dwelling time calculation and switching sequence selection are easily done like conventional MLI topologies. The proposed MLI is designed for both single phase system and three-phase system. The THD analysis for single-phase and three phase loading conditions.

II. CHBMLI WITH PULSE WIDTH MODULATION TECHNIQUES

Cascaded MLI or series H-bridge inverter is a very popular MLI topology especially for high and medium voltage range. In 1975 the series H -bridge inverter are introduced. CHBMLI has been utilized in a vast range of applications. Due to its flexibility and modularity it is widely used in high-power applications, especially series or shunt connected FACTS controllers. The CHBMLI produces its output same as sinusoidal voltage waveforms by combining number of isolated voltage levels. As the number of H-Bridge converter increases it increases the VAR without redesign the power stage. This in turn reduces the converter failure. The combination of single phase full bridges makes a phase for the inverter. Phase-shifted transformers can also supply the cells in medium-voltage systems in order to provide high power quality in the utility connection.

The switching devices connected in CHBMLI are triggered using numerous PWM techniques which are available in literature. In this paper level shifted carrier based PWM techniques is employed to provide gating pulses to the power semiconductor devices. Level shifted PWM techniques are broadly of four types; phase opposition disposition, alternate phase opposition disposition, carrier overlap, variable frequency. In this paper the proposed CHBMLI topology is tested for various loading condition using all the four above mentioned level shifted PWM techniques.

III. PROPOSED WORK

In the proposed work a reduced count CHBMLI is designed using total eight number of switches and three DC voltage sources to generate a 11 level multilevel inverter as shown in Fig.1. The three DC voltages are connected in series with each other. The value of the DC voltage sources is Vdc, 2Vdc and 2Vdc. That means if Vdc is 100Volts then the other two voltages will be 200volts. Four PWM techniques are used to obtain the result. Fig. 2 shows a Matlab/Simulink model of a three-phase MLI for 11 level output voltage.

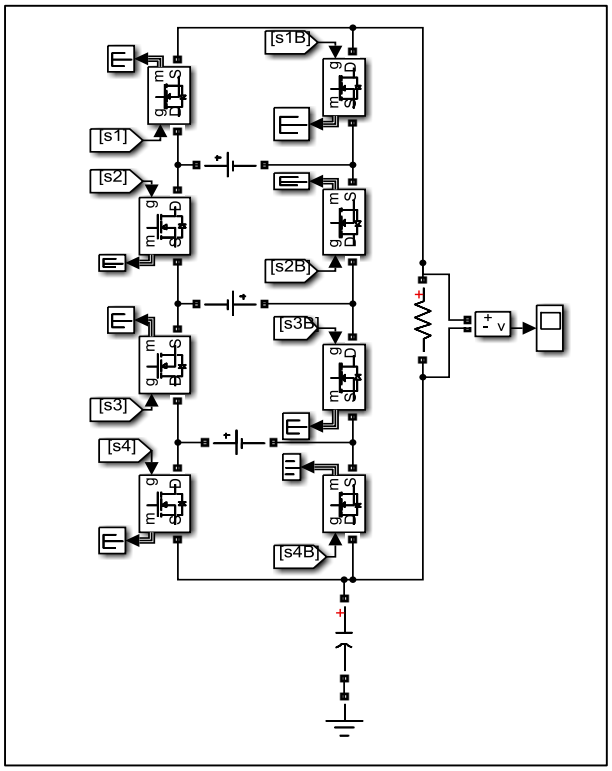

Fig. 1: Proposed configuration of single-phase CHB-MLI

It consists of eight switches which are turned ON simultaneously in order to generate 11 level output voltage. The switches are triggered using gate pulses as shown in figure 3. These pulses are obtained using level shifted PWM techniques which are designed using ten triangular signal and one sinusoidal carrier signal. The switches used are MOSFET due to their numerous advantages such as:-

1) Inexpensive.
2) Requires less maintenance.
3) Long life.
4) Easy avaibility.

Other type of switches can also be used in place of MOSFET such as IGBT, GTO etc.

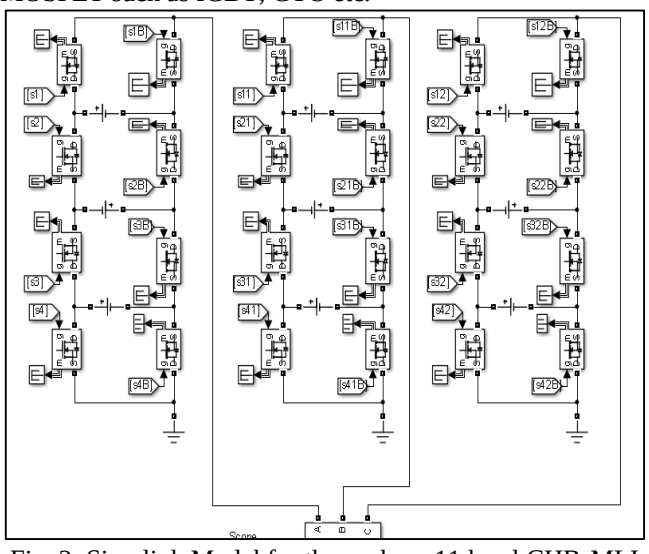

Fig. 2: Simulink Model for three-phase 11 level CHB-MLI

IV. RESULT AND DISCUSSION

Four different PWM techniques are used and they are In-phase disposition (IPPWM), Alternate phase Opposition disposition (APODPWM), Carrier Overlap (COPWM) and variable frequency (VFPWM). Triangular wave generators are used to produce these methods. Simulation results of a three phase 11level inverter are shown using four different PWM techniques and also their Total Harmonic reduction is shown. A comparison between these methods is also discussed. The simulation is performed using MATLAB. The proposed topology is tested for R and RL load for both single phase and three phase system. THD of the output voltage and current waveforms are analyzed for all the operating conditions. The simulation results for the proposed topology are presented in this chapter. The table for parameter selection is shown in Table 1 below. The FFT analysis tool is used to evaluate the performance of the proposed topology. The THD of source voltage and load current are calculated for three loading conditions mentioned above. The results obtained are filtered using LC filter and the THD are compared using with filter and without filter topology.

Components	Ratings
R load	124 ohms
RL load	115 ohms and 182mH
switching frequency	10khz
LC filter	1e-3 H and 1e-6 F
frequency=50 Hz	0.96mH
input voltage	450 V

Fig. 4 shows the output waveform of the proposed topology when connected with R load. Fig. 5 shows the output voltage waveform when connected with the RL load of single phase 11 level inverter. Fig. 6 shows the output voltage waveform of three-phase proposed MLI topology when connected with R load. Fig. 7 shows the output current waveform of three-phase proposed MLI topology when connected with R load. The THD analysis for various modulation techniques using single phase MLI is presented in Table 2 and for three phase MLI is presented in Table 3.

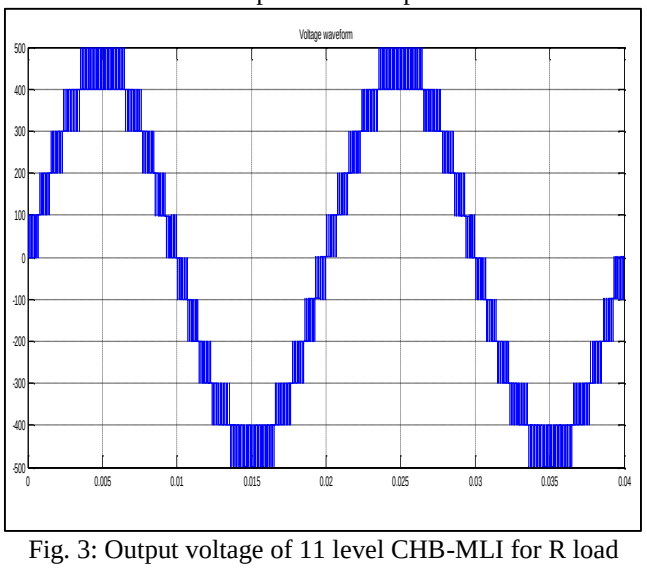

Fig. 3: Output voltage of 11 level CHB-MLI for R load using APOD PWM.

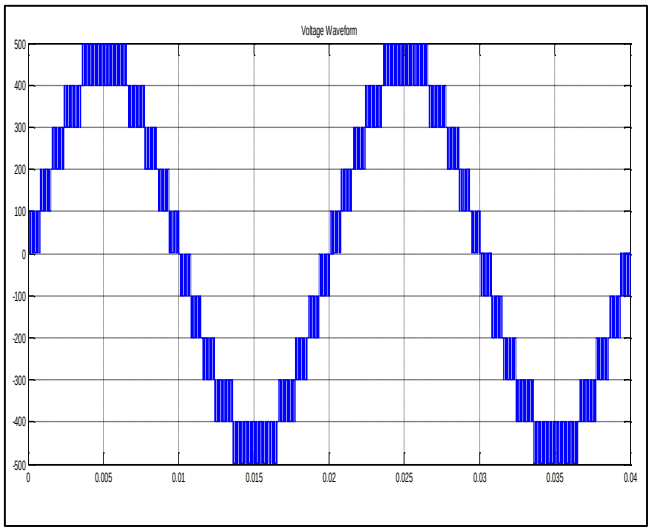

Fig. 4: Output voltage of 11 level CHB-MLI for RL load using CO PWM

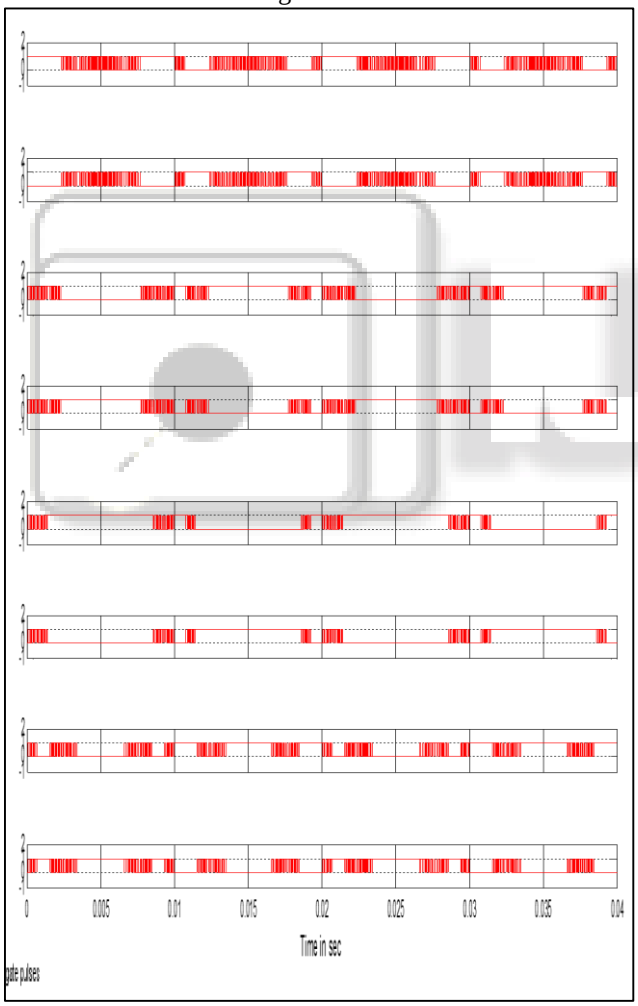

Fig. 5: Output voltage of 11 level CHB-MLI for IM load using CO PWM

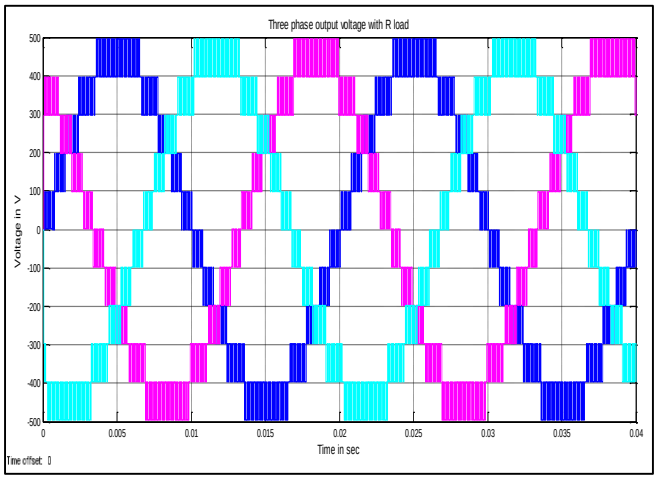

Fig. 6: Output voltage of 11 level three-phase CHB-MLI for R load

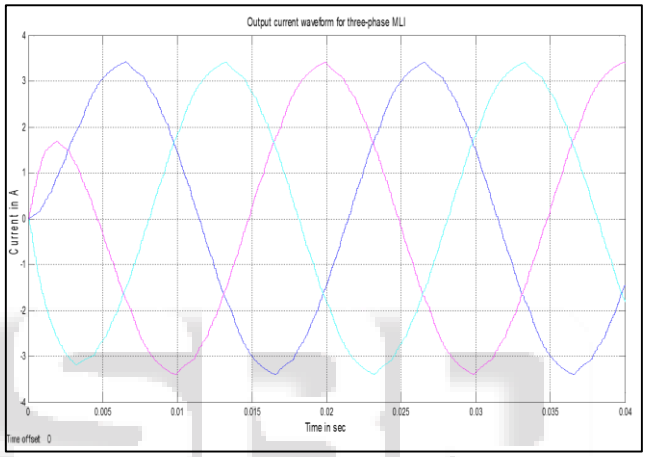

Fig. 6: Output current of 11 level three-phase CHB-MLI for R load

Level Shifted PWM techniques	Without Filter		With Filter	
	R load	RL load	R load	RL load
IPD	0.22	0.27	0.27	0.27
APOD	0.36	0.37	0.25	0.37
CO	1.80	1.81	1.80	1.81
VF	0.47	0.47	0.38	0.47

Table 2: comparison of THD for output voltage using different PWM techniques

Level Shifted PWM techniques	RL load		
	Phase a	Phase b	Phase c
IPD	1.8	2	2.3
APOD	1.7	2	2.3
CO	1.9	1.9	2.25
VF	2.4	2.4	3

Table 3: comparison of three phase system THD for output voltage for R load

V. CONCLUSION

Level shifted PWM control is implemented in this paper to design the hybrid MLI for different 11 levels at various loading conditions. It is observed that the proposed inverter has superior features compared to conventional multilevel inverters in terms of the component count, control requirements, cost, and reliability. The efficiency of the inverter is also better as compared to conventional topologies.

It is possible because of generating only positive carriers for pulse width modulation control. As the hybrid inverter requires low rated dc sources, fuel cells, photovoltaic arrays can also be used as dc sources.

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