Design and Implementation of High performance 5T SRAM

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Abstract— The paper describes the thorough overview of DRAM. The review discusses basic introduction of DRAM, DRAM architecture and its support circuitry. The paper also focuses on the study of four transistor DRAM cell, two transistor DRAM cell and one transistor DRAM cell. Read and write operations of different types of DRAMs are explained with help of control signal waveform. The comparison between two basic types of memories i.e. SRAM and DRAM is also discussed in the paper. Semiconductors memories are most important in today's aera. As the scaling large memories are fabricated on a single chip. It is possible to store large amount of data on and retrieve it at very high speed. The design of more memories on a single chip which increases power dissipation. The proposed design based on 5T SRAM with standby startup circuit which reduces power dissipation and reduction in leakage current. The circuit is design in 45nm CMOS technology file.

Keywords: 5T SRAM, 6TSRAM

I. INTRODUCTION

Today, systems on Chip are always a fast growing market. They embedded more and more complex functions that require an increasing memory capacity. The Static Random Access Memory SRAM is the mostly used solution where either bandwidth or low power, or both are principal considerations. SRAM is a type of semiconductor memory where the word static indicates that, unlike dynamic RAM (DRAM) [1], it does not need to be periodically refreshed, as SRAM uses bistable latching circuitry to store each bit. SRAM exhibits data remanence, but is still volatile in the conventional sense that data is eventually lost when the memory is not powered. SRAM is also easier to control (interface to) and generally more truly random access than modern types of DRAM. An SRAM cell has three different states it can be in: standby when the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have read- stability and write-ability respectively. Both conditions become difficult to satisfy in advanced technologies because of the high degree of variability in thin CMOS transistor parameter, essentially technologies beyond 45nm. Increasing the memory size makes the required degree of reliability hard to please. This makes the first challenge for the SRAMs in advanced technology nodes. The power consumption increases with the advanced CMOS technologies. CMOS scaling requires not only very low threshold voltages to retain the device switching speeds, but also RAM ultra-thin gate oxides to maintain the current drive and keep threshold voltage variations under control when dealing with short-channel effects. Low

Modern microprocessors employ on-chip caches, which can effectively reduces the speed gap between the processor and main memory to boost system performance. These on-chip caches are usually implemented using arrays of SRAM cells. A six transistor (6T) SRAM cell, shown in Fig. 1, is conventionally used as the memory cell. However, the mismatch in the strength between transistors of 6T SRAM cell due to process variations can results in failure during read operation, i.e. flipping of the cell data while reading, especially at lower levels of VDD [3]. Therefore, conventional SRAM cell shows poor stability at very small feature size. In addition, as CMOS technology scales down, an increase in total leakage current of a chip is observed.

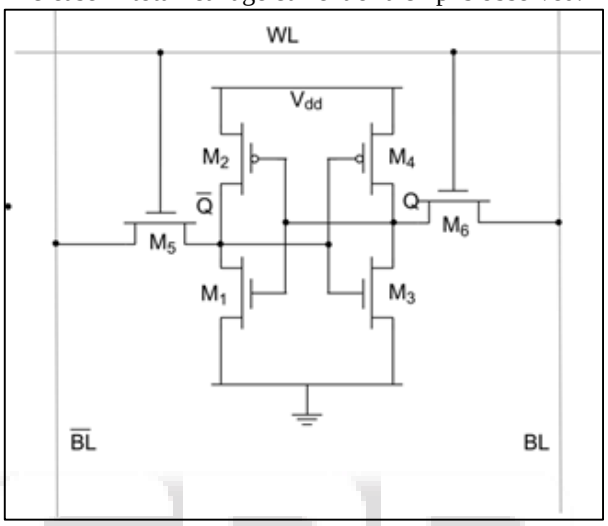

Fig. 1: Conventional 6T SRAM Cell

Moreover, the total leakage current of chip is proportional to the number of transistors on the chip. Since the SRAM includes large number of transistors on a chip, the SRAM leakage has also become a more significant component of total chip leakage in scaled CMOS technology. Hence, stability during read operation and leakage current of SRAM cell are two most prominent parameters in designing of SRAM cell in nano-scale CMOS technologies. A novel 5T SRAM cell [4] has been previously proposed as an improvement to the standard six transistor (6T) SRAM cell model in various aspects. This 5T SRAM cell, as shown in Fig. 2, comprises two inverters, connected back-to-back and one additional transistor that is used to access the cell for read and write. Here both the bit-lines are precharged to *VDD* to retain the data during standby mode. However, the speed of a cell, which characterizes the performance of the cell, is still to be improved to reduce the speed gap further between processor and main memory.

An SRAM cell has three modes of operation, namely read, write and standby. The data stored in the cells may be corrupted when the cells are read. This problem arises from the fact that a higher voltage on the bitline is coupled to a lower voltage in the cell, causing the bit line voltage to drop and the cell voltage to rise. For instance, when a logic '0' stored initially, the voltage rise in the cell may corrupt the data stored. Further, a concern associated with the write operation is that it is relatively difficult to write a logic '1' to the cell if the cell currently stores a logic '0'. Accordingly, the SRAM cell should provide less likely to be corrupted when the cell is read and more reliable when the cell is written. Memories take up 80% of the die area in high

performance processors. Therefore, there is a crucial need for a low leakage and highly robust SRAM design. Static random access memory (SRAM), the most widely used embedded memory, typically occupies the largest portion of SoC die area, and often dominates the total chip power. In order to maintain performance, however, this has required a corresponding reduction in the transistor oxide thickness to provide sufficient current drive at the reduced supply voltages. To further reduce the leakage current, we can use high threshold transistors. The transistors have been lowered which also contributes to reduced leakage currents and hence reduces the power consumption. The low power reduction techniques based on the dependencies of the tunneling currents on the terminal voltages, the gate oxide thickness, and the type of the transistor. Various efficient techniques which gives overall best performance over existing SRAM design approaches that allow the analysis and simulations of different parameters at 90nm technology successfully on the basis of the power dissipation, speed and area efficiency of the circuit.

II. LITERATURE SURVEY

A new single-port five-transistor (5T) Static Random Access Memory (SRAM) cell with integrated read/write assist is proposed. Amongst the assist circuitry, a voltage control circuit is coupled to the sources corresponding to driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. Specifically, during a write operation, by means of sizing [1]

The newly developed CMOS five-transistor SRAM cell uses one word-line and one bit-line during read/write operation. This cell retains its data with leakage current and positive feedback without refresh cycle. The new cell size is 18% smaller than a conventional six-transistor SRAM cell using same design rules. Simulation result in standard 0.25J.1m CMOS technology shows purposed cell has correct operation during read/write and idle mode. The average delay of new cell is 20% smaller than a six-transistor SRAM cell.[2] A novel five-transistor (5T) static memory cell is presented for applications in high-speed, low-power cache. The 5T design in 0.18pm bulk CMOS exhibits 57% faster operation speed, a 12% reduction in power, and a 6% reduction in area with respect to the standard 6T cell design.[3]

This paper is based on the observation of a CMOS five-transistor SRAM cell (5T SRAM cell) for very high density and low power applications. This cell retains its data with leakage current and positive feedback without refresh cycle. This 5T SRAM cell uses one word-line and one bit-line and extra redline control. The new cell size is 21.66% smaller than a conventional six-transistor SRAM cell using same design rules with no performance degradation.[4]These paper describes a 5-transistor (5T) SRAM bitcell that uses a novel asymmetric sizing approach to achieve increased read stability. Measurements of a 32 kb 5T SRAM in a 45nm bulk CMOS technology validate the design, showing read functionality below 0.5V. The 5T bitcell has lower write margin than the 6T, but measurements of the 45nm 5T array confirm that a write assist method restores comparable writability with a 6T down to 0.7 V.[5]

III. PROPOSED 5T SRAM CELL

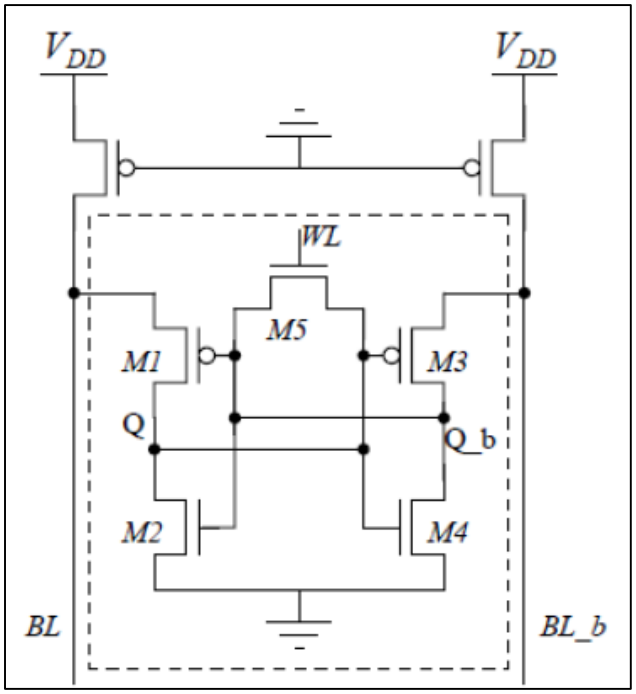

Fig. 2: Novel 5T SRAM Cell

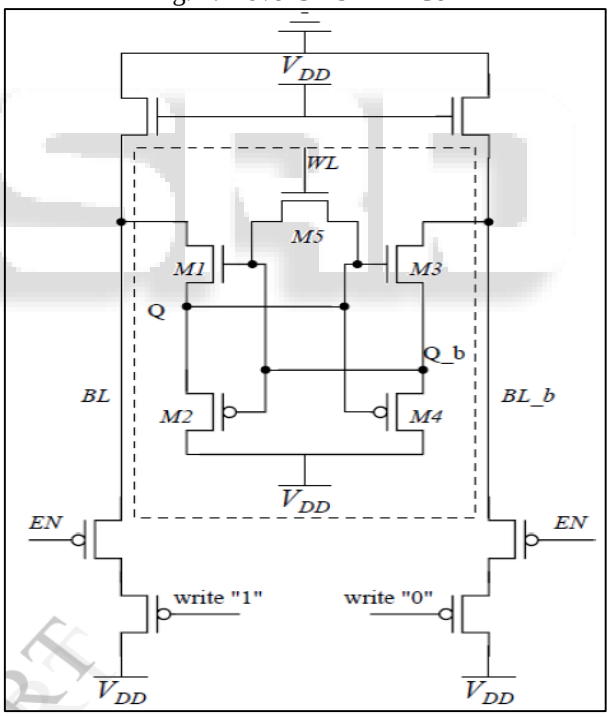

Fig. 3: Proposed 5T SRAM Cell

Fig. 3 shows the proposed five transistor (5T) SRAM cell. In this cell, Inverter NMOS transistors (M1, M3) are directly connected to the bit lines, PMOS transistors (M2, M4) are connected to power supply voltage (VDD), and there is an additional transistor M5 coupling the inverters. Unlike standard cell, no word line transistors are needed to provide access during the read and write cycles. In contrast to novel 5T cell, bit lines of the proposed cell are precharged to ground.

A. Standby Mode

Before discussing the operation of proposed SRAM cell, operations of the previously introduced novel 5T cell will be reviewed to clarify the difference between former and later. In the novel 5T cell, introduced earlier [4], when the cell is in a stand by cycle, M5 is turned off by keeping word line (WL) at ground, the bit lines are precharged to VDD, and the data is preserved by the cross-coupled inverters. In the proposed 5T cell, as shown in Fig. 3, during stand by period (precharge stage) the word line (WL) associated with M5 is set to low, which turns off M5, and bit lines are precharged to ground so that the data which was written during write operation is retained by the cross-coupled inverters.

B. Write Operation

The write operation is accomplished by effectively asserting the word line (WL). Simultaneously, depending on Fig. 3. Proposed 5T SRAM Cell the state already stored in the cell, either write "0" or write "1" signal is activated to push one of the bit lines to approximately 2/3 VDD so that the contents of the cell will flip to reflect the bit line data. Consider the situations for the two possible write operations that can be performed on the cell: Write "0" Operation

Assume that initially, i.e. before write "0" operation, the values of the Q and Q_b of the cell are at "1" and "0" respectively. In this stage, transistors M2 and M3 are in the triode region, and M1 and M4 are in cut-off. The operation of write "0" is accomplished by forcing BL_b to approximately 2/3VDD by turning on both the PMOS transistors associated with write "0" and EN signals. Now the source voltage of the NMOS transistor M3 is at approximately 2/3 VDD rather than "0", and there is a charge transfer between input terminals of the inverters because of turn on transistor M5. Thus Q_b is getting charged towards VDD due to M3, which is conducting in the triode region. When the voltage at Q_b exceeds the threshold voltage of M1, the voltage at Q starts discharging towards "0". This initiates a regenerative effect between the two inverters [5]. Eventually, M2 turns off and the voltage at Q falls to "0" due to the pull-down. Simultaneously, M turns on and the voltage at Q_b rises to VDD due to the pull-up action of M4. When the cell finally flips to the new state, the word line associated with M5 is returned to its low stand by level. The write cycle begins by applying the value to be written to the bit lines. If we want to write a 0, we would apply a 0 to the bit line, i.e. setting to 1 and BL to 0. This is similar to applying a reset pulse to a SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit WL is then active and the value that is to be stored is latched.

IV. Difference between DRAM verses SRAM

SRAM and DRAM are two basic types of RAM. The term SRAM stands for Static Random Access Memory and DRAM stands for Dynamic Random Access Memory. SRAM is made up of transistor and DRAM is made up of capacitor. Therefore a SRAM stores the binary bit inform of voltage; 5v represent 1 and 0v represents 0. DRAM stores binary bit in form of charge; presence of charge represent 1 and absence of charge (discharge) represent 0. The charge on the capacitor naturally leaks in few milliseconds. Therefore a DRAM need to be recharged (called refreshing a DRAM) periodically generally every 2 milliseconds. For this, a DRAM need a special refreshing circuit. DRAMs are cheaper than SRAMs and have high packing density. A DRAM consumes less power than a SRAM. They have lower speed than SRAMs. Cheaper DRAM is used in main memory while SRAM is commonly used in cache memory.

V. Conclusion

The growing market of portable electronic devices and demand of the very low power dissipation, longer battery life and compact system, this paper have analyze a SRAM cell circuit which have very low power dissipation as we know that the static random access memory is used in high speed application such as cache memory in SOC and occupies about 90% of silicon area. Difference between SRAM and DRAM is Thus study of 5T SRAM and 6T SRAM is studied. The area is reduced in 5T SRAM.

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