

Design Cascoded Transistor Based Second Stage Operational Amplifier on 180nm Technology

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Abstract— This paper shows operational amplifier based on cascoded transistor second stage which is very important stage for any operational amplifier. Cascoding increases the gain as well as reduces the channel length modulation problem with increase in output swing. With this operational amplifier, 75 dB of gain, 173 dB of CMRR, 98 MHz of UGB and 110 V/us of slew rate is achieved.

Keywords: Operational amplifier, Cascoded, Gain, UGB, GBW, CMRR

I. INTRODUCTION

Operational amplifier (op-amp) has paramount significance inside the analog ic's. Two stage cmos op-amp is broadly acceptable for its easy simple design topology and robustness overall performance. An op-amp designer should take care of the dc gain, gain bandwidth, slew rate, settling time, phase margin, power dissipation. Furthermore, other topology based totally on enhancing and focusing on specific parameter of op-amp have also been mentioned [1]–[4]. But, two stage cmos op-amp with miller capacitance compensation is the maximum handiest and effortlessly tunable design topology of op-amp. Aspect ratios of mosfets additionally play main position in determining the op-amp performance parameters [5].

In this work , cascoding of PMOS and NMOS in second stage is shown which helps to increase the gain as well as reduce's the channel length modulation problem.

II. DESIGN

Figure 2.1 show operational amplifier consist twelve transistor, two capacitor- one is compensating capacitor and load capacitor. Input transistor consist of PMOS followed by two NMOS and two PMOS are connected in mirror form. Second stage consist of two PMOS connected near to the vdd and two NMOS near to the ground in stack form.

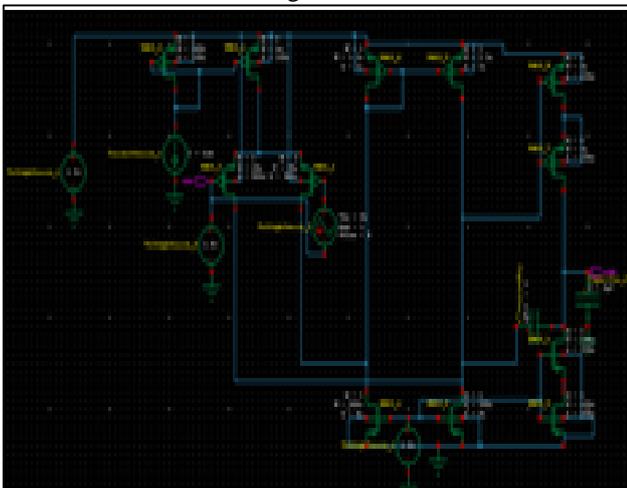


Fig. 2.1: operational amplifier.

III. SIMULATION RESULT

The simulation done on Tanner Eda tool using 180 nm technology. The whole circuit consume 22 uW.

– Gain, UGB, GBW

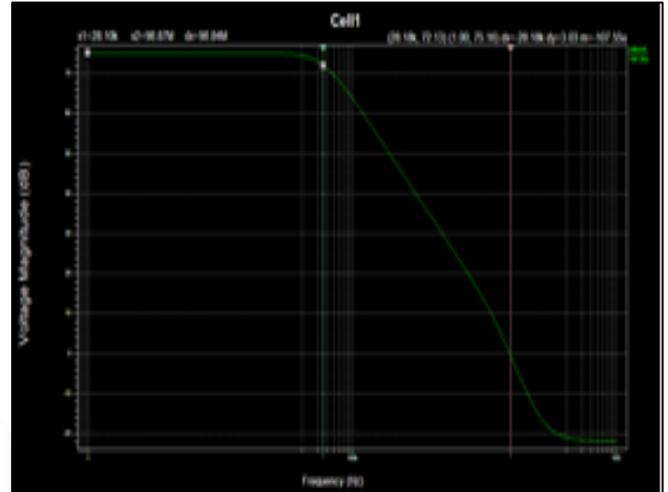


Fig. 3.1: Frequency Response

Figure 3.1 shows the frequency response in which gain is of 75 dB, UGB is 98 MHz and GBW is 28 kHz.

– CMRR(Common Mode Rejection Ratio)

The differential gain(A_d) obtained from this operational amplifier is 7 dB and common mode gain (A_{cm}) is -166 dB. So the CMRR is the difference between A_d and A_{cm} [5] and it is 173 dB which make this operational amplifier good candidate for bio-medical applications.

	Previous op amp[6]	Proposed op amp
Process	22nm	180nm
Supply-Voltage	0.8V	1.8
DC gain	69dB	75dB
Power	43uW	22uW
UGB	29MHz	98 MHz
CMRR	59dB	173 dB

Table 1: Comparison Table

IV. CONCLUSION

This paper shows operational amplifier with cascade stage in which second stage is cascade. In this, PMOS and NMOS are connected in stack form. This arrangement gives gain of 75 dB, UGB of 98 MHz and CMRR of 173 dB with power consumption of 22uW.

REFERENCES

- [1] J. Mahattanakul and J. Chutichatuporn, "Design procedure for twostage cmos opamp with flexible noise-

- power balancing scheme,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 52, no. 8, pp. 1508–1514, 2005.
- [2] M. Taherzadeh-Sani and A. A. Hamoui, “A 1-v process-insensitive current-scalable two-stage opamp with enhanced dc gain and settling behavior in 65-nm digital cmos,” IEEE Journal of Solid-State Circuits, vol. 46, no. 3, pp. 660–668, 2011.
- [3] H. Huang and E. I. El-Masry, “A fast settling cmos operational amplifier,” in Circuits and Systems, 2003. ISCAS’03. Proceedings of the 2003 International Symposium on, vol. 1. IEEE, 2003, pp. I–I.
- [4] J. Yan and R. L. Geiger, “A negative conductance voltage gain enhancement technique for low voltage high speed cmos op amp design,” in Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on, vol. 1. IEEE, 2000, pp. 502–505.
- [5] Yadav, “Design of two-stage cmos op-amp and analyze the effect of scaling,” International Journal of Engineering Research and Applications (IJERA), vol. 2, no. 5, pp. 647–654, 2012.
- [6] Edward Yang and Torsten Lehmann, “High Gain Operational Amplifiers in 22 nm CMOS,” IEEE, 2019.

