FPGA Implementation of the Hybrid Model of Direct Digital Synthesizer (DDS) using LUT

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Abstract— The DDS have been experimentally implemented in Field Programmable Gate Array (FPGA) that synthesis the waveforms like sine wave, triangular, Saw tooth and Square wave using Look up Table (LUT). A Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) based ROM is designed using embedded RAM of the Xilinx Spartan - 6 FPGA chip. A VHDL based counter is also designed which works as address generator to continuously supply the address of ROM to read the stored sample values from the LUT. The digital part consists of a Phase Accumulator (PA) and a LUT. The 16-bits Phase Accumulator is implemented by means of a register along with an adder and feedback loop. LUT is implemented using VHDL code. The size of LUT is reducing by storing quarter of sine wave in the ROM. This design was tested with various tuning frequencies and the result shows that the output frequency is directly proportional to the tuning input frequency. The sample values are converted into continuous signals using a Digital to Analog Converter (DAC). The VHDL program is downloaded into FPGA chip using JTAG in Xilinx Integrated Software Environment (ISE) tool. The simulation results of VHDL based ROM with address generator is shown in the form timing diagram obtained using ModelSim software. Experimental result of generation of sinusoidal waveform is also presented. FPGA development board has 100MHz on board clock generator. Since we are using FPGA as a hardware part, in future easily upgrade the signal generator by altering the VHDL program for FPGA design. Estimated power consumption of the FPGA based design excluding the DAC is found to be 240mW.

Keywords: DDS; FPGA Implementation; Phase Accumulator; ROM; Xilinx14.1; VHDL; LUT

I. INTRODUCTION

The hybrid model of Direct Digital Synthesizer (DDS) is a multiple signals like generating sinusoidal, Triangular, Sawtooth as analogue waveforms and Square waveform with predefined frequency. DDS has a various application in the advanced communication era such as mobile telephones, radiotelephones, CB radios, radio receivers, walkie-talkies, satellite receivers and none the less GPS system etc. The focus of this paper is on the design, analysis and simulation of DDS using ModelSim and Anvyl Sparten-6 FPGA board.DDS provides many significant advantages such as sub-Hertz frequency resolution, continuous-phase switching response, fast settling time and low phase noise. One important design constraint of the DDS is a Look up Table (LUT). The size of the LUT affected by factors that depend on response time, the power consumption and which affect the size of the DDS. The resolution and the size of DDS are also dependable on the size of the phase accumulator. In this method, the phase or amplitude of an analogue signals wave cycle is sampled at the equal phase intervals to obtain a discrete sequence for continuous wave period thus computing its analog amplitude. Consequently, a single period of a continuous wave is converted into a binary sequence using MATLAB. The sequence of binary stream represents the quantized amplitude of the continuous wave to be stored in a ROM memory. The full complete cycle of continuous wave is divided into four parts; hence quarter part of complete one cycle is inverted and repeated. Therefore, the content of the ROM memory matches the phase sampling value for a single cycle of continuous wave. So the implementations of a quarter part of the continuous waveform those results in the size reduction of the LUT unit. The design and the implementation of DDS systems performed by VHDL are becomes simple and efficient trend towards DDS design. Xilinx ISE 14.1 suit, an appropriate platform for VHDL compilation, synthesis and implementation, which offers a strong simulation tool. Therefore, it is simplify and enhances the overall design procedure [1].In architecture of DDS the main designs includes phase accumulator and phase to amplitude converter which implemented using VHDL on FPGA Sparten-6. Hence DDS will be reconfigurable and resizable.

Concept of LUT is constructed using ROM memory, the discrete samples of a continuous wave saved in LUT [2]. The block diagram of a phase accumulator system is shown in Figure 2. The phase accumulator produces continues signals at a certain frequency selective word (FSW) which determines the phase. Also, FSW determines the frequencies of a signal to be produced. Phase accumulator output continuously produces proper binary words representing the instant linear phase value for the look-up table function. The phase to amplitude converter is nothing but Look up Table which converts phase values into amplitude. The output signal frequency for DDS system is represented in 16-bits, that determined by following equation $Fout = W\ Fclk\ /2^N$ Where W is the FSW, N=16 is the number of bits, that can phase accumulator handles and Fclk is system clock [3].

II. DIRECT DIGITAL SYNTHESIZER

This DDS system is produces wide range of output frequency. The block diagram of Direct Digital Synthesizer is as shown in Figure 1.

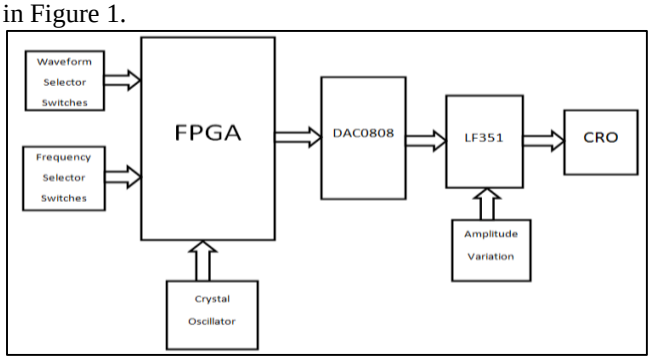

Fig. 1: Block diagram of DDS System

It is composed of reference clock, a frequency control register with 16 bits binary word, a Phase Accumulator, phase to amplitude converter is nothing but Look up Table, Digital to analog converter (DAC) and Low pass filter. Phase Accumulator and phase to amplitude converter is implemented into FPGA Sparten-6, which generates digital sine wave and it will convert into analog by DAC. The design is simulated by Xilinx ISE tool and MODELSIM software which would be used to see the analog waveforms.

III. Performance Parameter of DDS

A. Frequency Tuning:

The frequency of the DDS can be controlled using the FSW (Frequency Selective Word) or FCW (Frequency controlled word).The output frequency will be determined by the FSW [4]. Fdds= FSW * $Fclk$ /2^N Where, Fclk = Clock Frequency, The output frequency can be changed by changing the FSW.

B. Frequency Resolution

The frequency resolution of the direct digital synthesizer is a function of the applied referenced clock frequency of FPGA board and number of bits (N) employed in phase accumulator. The frequency resolution can be calculated using the formula given below $\Delta f = Fref / 2^N$, Where Δf = frequency resolution in Hz. In order to obtain improved frequency resolution, numbers of bits entered in the phase accumulators are increase the resolution [1].

C. Signal-to-Noise Ratio

Signal-to-noise ratio used to characterize the spectral quality of a signal waveform and it will determine by the formula: SNR (dB) = 6.02 AW + 1.8 [4][5]. By considering errors, the SNR for aw = 16 is 92 dB.

IV. Design of Sub modules of DDS

A. Design of Phase Accumulator

A full adder with a control word length of 16 bits is necessary to produce the phase address for the analog sine or cosine signal in ROMs. The block diagram of phase accumulator as shown in Figure 2.The phase Accumulator uses register having length: N-bit, that also called as digital Frequency-to-Phase Converter (FPC), or digital phase wheel (phase pointer: digital representation of instantaneous phase), as shown in Figure3[5].For linear phase samples, overflowing phase accumulator formed by an full adder and phase accumulator register integrates at a clock rate, so the frequency tuning data in phase increment register. The frequency control value added to phase accumulator that controls the average frequency of the "overflowing event". Note: The phase accumulator width (N) determines the frequency resolution of the DDS.

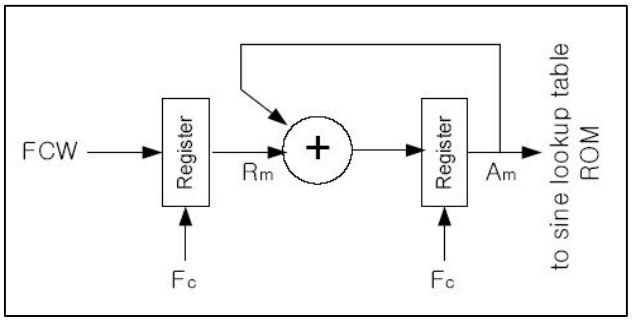

Fig. 2: Phase accumulator

B. The phase increment (W)

The phase increment (W) is achieved by the formula: Phase_in (W) = $fout\ Fclk * 2\text{^}16$[4].

The block diagram represents in phase accumulator on each clock tick event the phase increment value(W) will added by adder with the results of previous clock event as feedback.

This process helps to gives slope of the quantized level of the waveform.

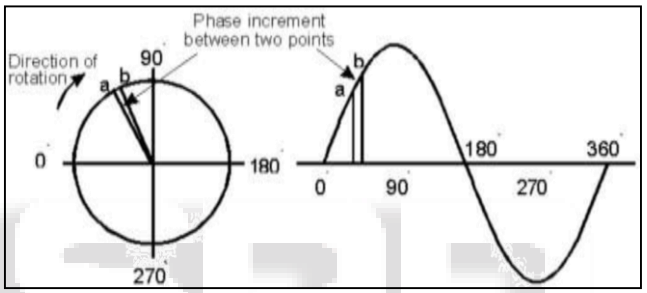

Fig. 3: Digital Phase wheel

As shown in Figure 3[5], the phase accumulator function is represented as a digital phase wheel which gives increment in phase value from 0^0 to 360^0 cycle. The complete sine wave oscillation can be supposed as a point moving around the circle. Each designated point like a, b as shown in Figure 3[5] which corresponds to equivalent point on the cycle of the sine waveform. One complete rotation gives one complete oscillation of the sine wave. If one cycle is completed then rotation starts over again [6]. The number of points on the cycle is generally determined by N which is 16 here i.e. 2^{16} points. But due to phase truncation the number of points equals to 2^{12}. So the address "000000000000" corresponds to 0º and the address "111111111111" is equal to 359.98º. The distance between two points a and b can determined by the value of W which is the phase increment. Hence the output frequency can be changed by changing the value of W. For higher frequency, W should be large and vice versa [4].

C. Design of Phase to Amplitude Converter

This section of DDS contains a Look up table in a read only memory (ROM). This LUT is used to convert the phase accumulator's output value which is linear amplitude information of waveforms [4]. It is basically a memory which stores sampled 10 bit binary values which are stored in hexadecimal format. These values act as amplitudes which are taken into account as integer values. The phase accumulator gives output in 16 bit binary value. If we use all the 16 bits as address, we would require large memory space

for the look up table. Hence it gives phase truncation [6]. So we use only the top 12 bits of phase accumulator to address the LUT. Therefore the total required memory locations to store the amplitude values are only 2^{12} = 4096[5].

The Figure 4 shows RTL view of Phase Accumulator with LUT. Consist of four inputs like clock, enable, reset and phase_increment as FSW with four waveforms as output. It generates Analog signal output values for sawtooth, triangular, sine wave and square wave. These outputs are fed externally to DAC.

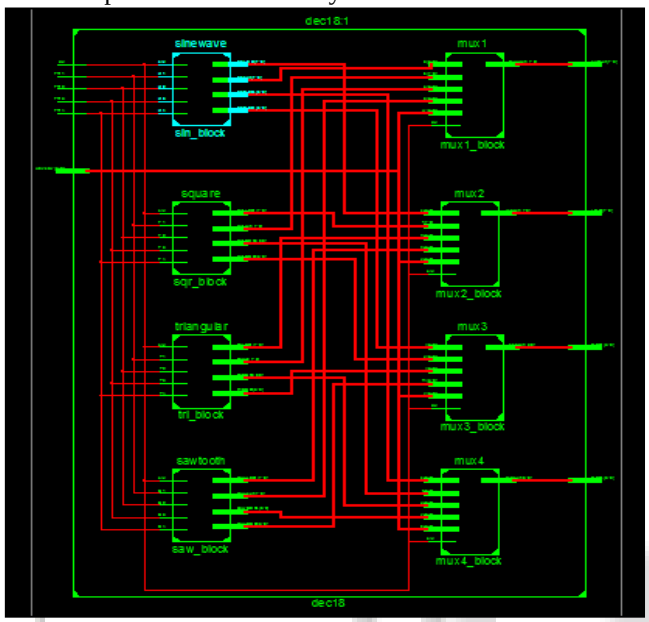

Fig. 4: RTL Structure view of DDS

D. Reconstruction of Analog Wave:

Extracting the analog signal from its discrete samples using digital to Analog converter(DAC).The DAC has data length N-bits, It is also called discrete binary values-to-voltage(current) converter, it realizes a hybrid multiplication (the DAC function). Usually the NRZ (non-return-to-zero) format is used to avoid a roll-off effect of ZOH (zero-order-hold) amplitude in discrete binary sequence (the output of LUT) is fed to DAC [7][8]. Spectral envelope is generated at DAC output.

E. Anti-Imaging Filter:

It is used as images-to-information (base) converter, or analog smoothing of quantized output values (reconstruction of signal) using low pass filter [6].

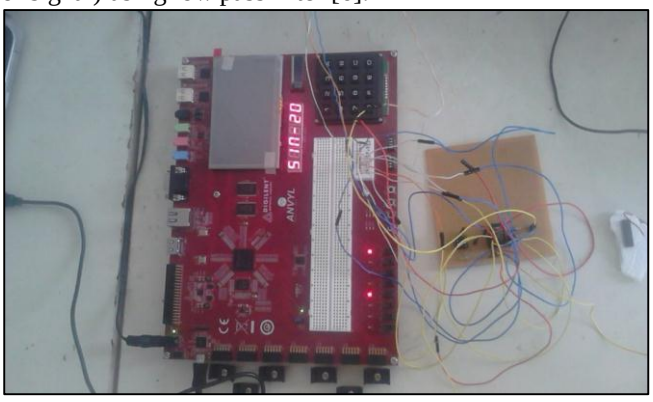

Fig. 5: Hardware Implementation of DDS

F. Simulation Results:

The above discussed modules are simulated and synthesized by Xilinx ISE Design Suite 12.3_1.

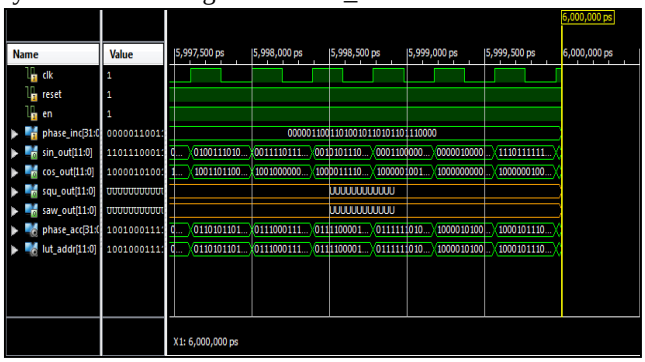

Fig. 6: Simulation Result of Phase Accumulator with LUT

The above Figure 6 shows simulation result of Phase Accumulator with LUT. Which receives Phase_increment value as Frequency Selective Word (FSW) are 20 and keeping the reference frequency (clock) of 100 MHz will generates output frequency of DDS as 30517.57Hz.

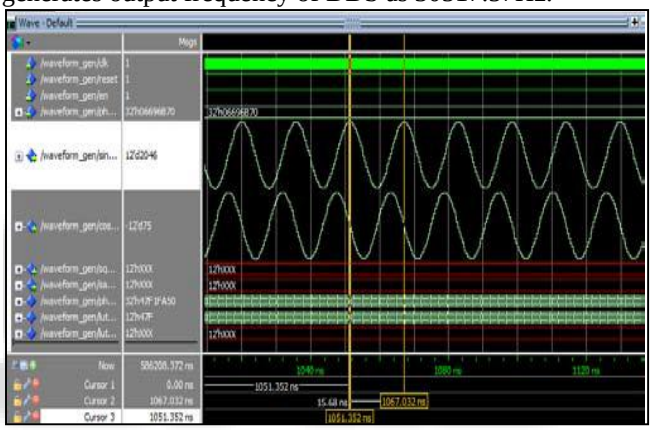

Fig. 7: Simulation Result of DDS using ModelSim Simulator

The Figure 7 shows Simulation result of Direct Digital Synthesizer using ModelSim Simulator. This simulation represents sine and cosine wave with frequency 30517.57Hz. By using this technique we can calculate following parameters: Below Table shows signal parameter that is calculated by generated signal and formulae.

G. Calculated Signal Parameters:

Reference Clock 50 MHz, Frequency Selective Word W=20, Desired Output Frequency 30517.57Hz, Frequency Resolution 1.5937 Hz and Signal-to-Noise Ratio 92 dB.

V. CONCLUSIONS

In the hybrid model of Direct Digital Synthesizer (DDS) using LUT is implemented in reconfigurable Spartan-6 FPGA chip. We have designed a 16 bit Phase Accumulator and look up table for phase to amplitude conversion. Multiple waveforms that are sine, cosine, square and saw tooth are generated, which increases the area of application. Since these waveforms are of 12 bit each, the result will also have greater accuracy. The phase accumulator and look-up table are the main reconfigurable block in hardware to set various frequencies of DDS. This complete design has been capable to produce waveforms up to MHz range.

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